Micromegas for the Muon System upgrade

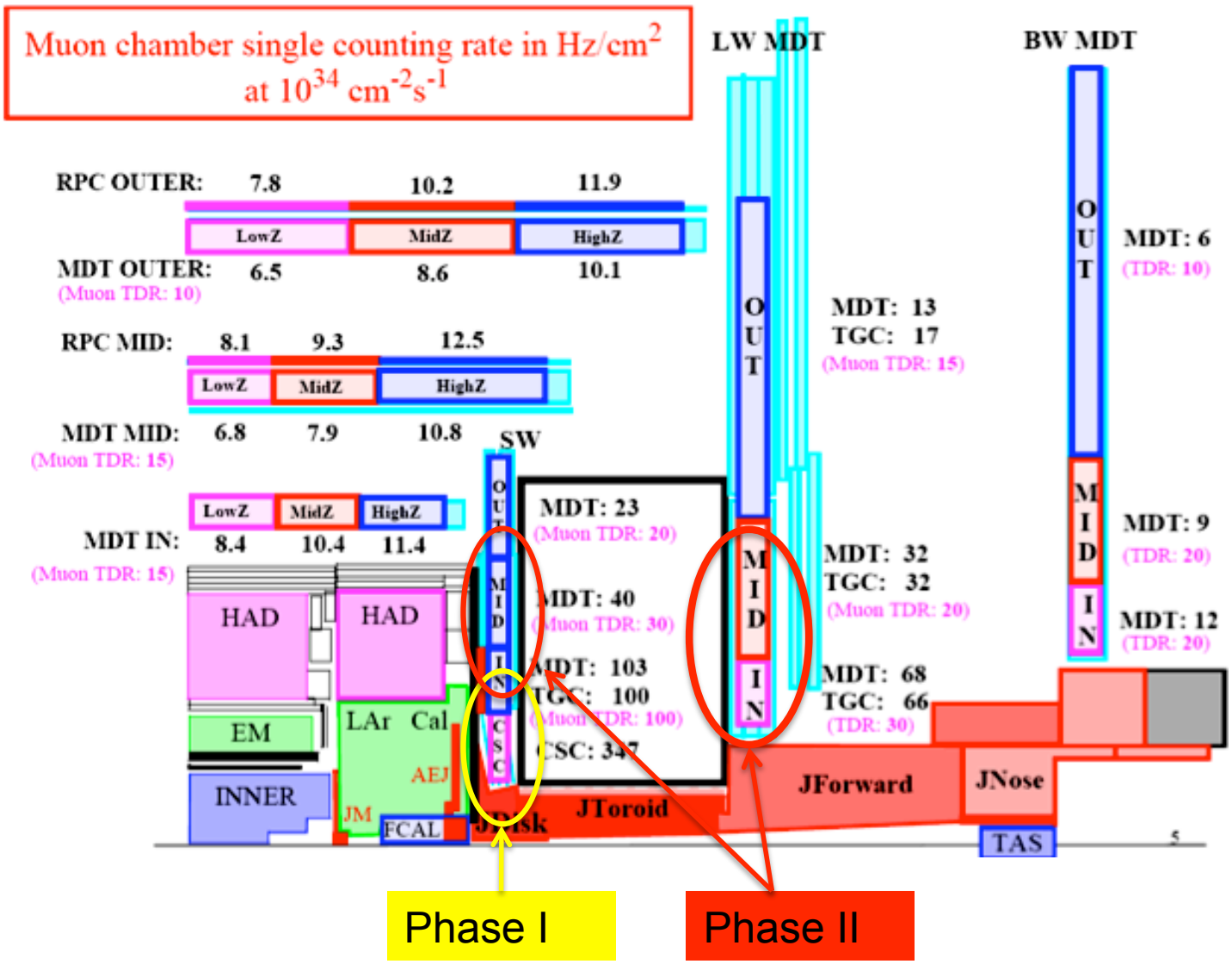
Arizona, Athens (U, NTU, Demokritos), Brookhaven, CERN, Harvard, Istanbul (Bogaziçi, Doğuş), Naples, CEA Saclay, Seattle, USTC Hefei, South Carolina, St. Petersburg, Shandong, Stony Brook,Thessaloniki

https://twiki.cern.ch/twiki/bin/view/Atlas/MuonMicromegas

Scope

Upgrade of the forward region of the ATLAS muon system for the luminosity increase of the LHC

- Phase I: 10^{34} cm^{-2} s^{-1} –> 2–3 x 10^{34} cm^{-2} s^{-1}
  - Complement the present Cathode Strip Chambers
  - 32 thin chambers of 1 m^2
  - Time-scale: installation ≥ 2014
- Phase II: L = 10^{35} cm^{-2} s^{-1}
  - Replace all Small Wheel chambers (MDTs + TGCs)
  - Replace Big Wheel chambers (MDTs + TGCs) for $\eta > 2$
  - 400 chambers of 1–2 m^2
  - Time-scale: ≥ 2018


Muon chamber single counting rate in Hz/cm^2 at 10^{34} cm^{-2}s^{-1}
LW MDT
BW MDT
RPC OUTER: 7.8 10.2 11.9
LowZ MidZ HighZ
MDT OUTER: 6.5 8.6 10.1
(Muon TDR: 10)
RPC MID: 8.1 9.3 12.5
LowZ MidZ HighZ
MDT MID: 6.8 7.9 10.8
(Muon TDR: 15)
SW
LowZ MidZ HighZ
MDT IN: 8.4 10.4 11.4
(Muon TDR: 15)
MDT: 23
(Muon TDR: 20)
MDT: 40
(Muon TDR: 30)
MDT: 103
TGC: 100
(Muon TDR: 100)
CSC: 347
MDT: 13
TGC: 17
(Muon TDR: 15)
MDT: 32
TGC: 32
(Muon TDR: 20)
MDT: 68
TGC: 66
(TDR: 30)
MDT: 6
(TDR: 10)
MDT: 9
(TDR: 20)
MDT: 12
(TDR: 20)
HAD
HAD
EM
LAr Cal
INNER
AEJ
JM
FCAL
JToroid
JForward
JNose
TAS
Phase I
Phase II

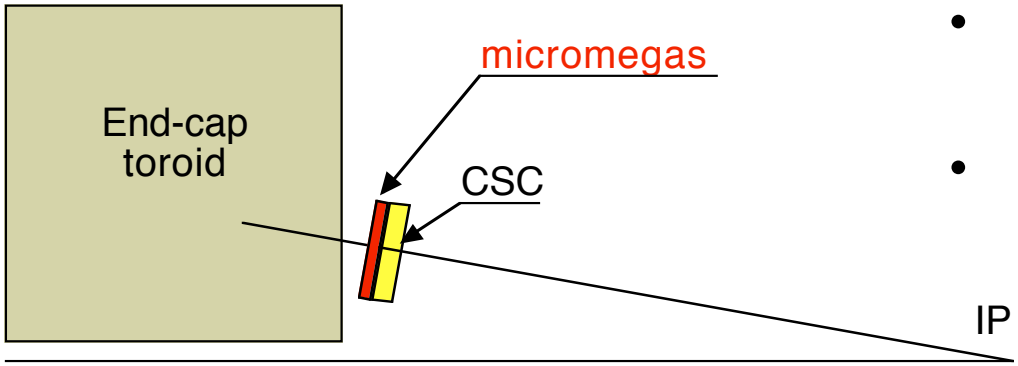
Why micromegas technology

- Robust detector that can be industrially produced
- Excellent performance (see MPGD2009, K. Nikolopoulos)
  - Very good spatial resolution
  - Timing performance sufficient for triggering
  - Potential to deliver track vectors in a single plane for track reconstruction and LV1 trigger
- Flexibility in the readout segmentation
- Excellent rate capability & ageing properties

The competitors

- Small (15 mm) diameter drift tube chambers
  - Similar to existing MDT chambers
  - Need extra 2nd coordinate measurement
  - Not obvious to stand rate at Phase II
- TGCs with smaller cathode strips and pad readout
  - Proven technology (used in ATLAS as trigger chambers), existing production facilities
  - Labour-intensive to construct, no good spatial resolution for larger track impact angles, not obvious that they can stand the high rates …

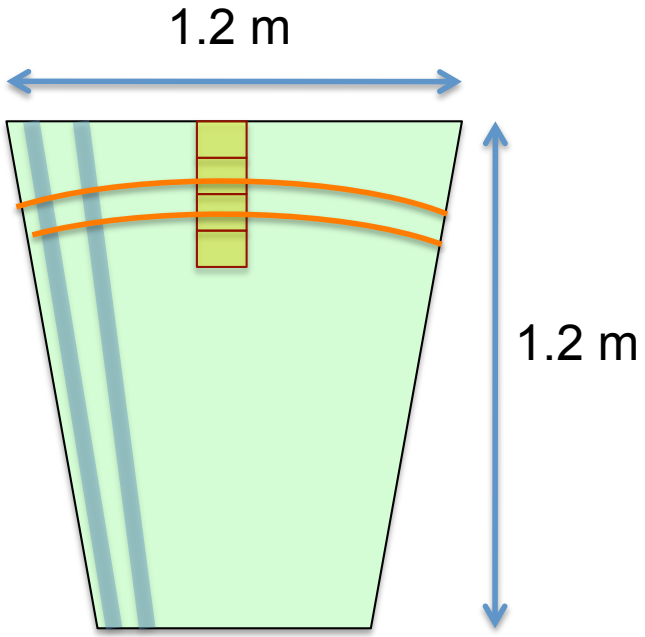
ATLAS upgrade – Phase I



- Strips for precision co-ordinate can be arranged circular
- 2nd co-ordinate strips and/or pads of any shape

- Thin chambers to be added to CSCs
- Number of channels/module for 500 µm pitch:
  - 2400 x 2 = 4.8 k (precision strips)
  - O(200) strips for 2nd coordinate
  - O(1000) pads for space points

  Total/module: 6 k channels
- 32 chambers of 1 m^2 with 4 active layers each (total MM area 100 m^2)
- Total # of channels : 200 k

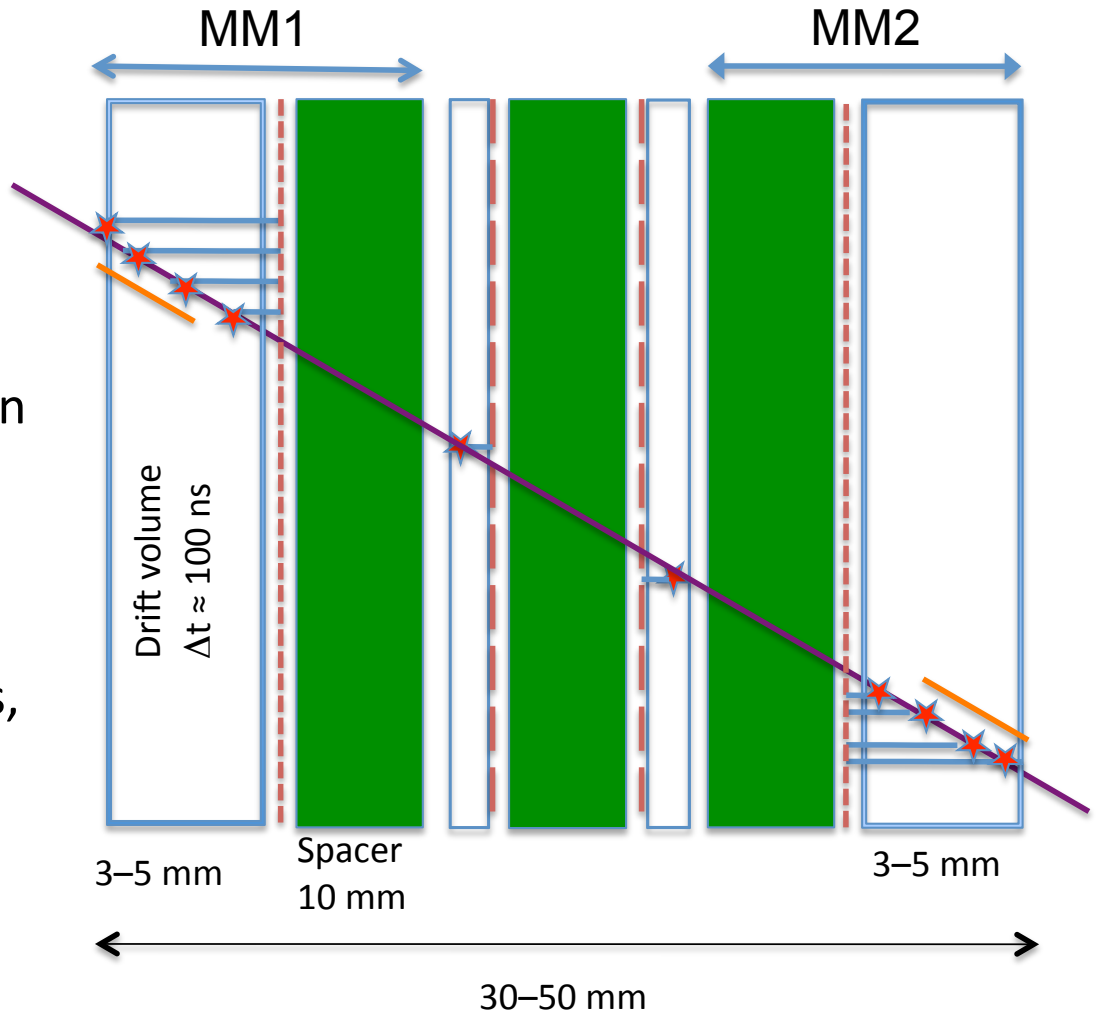


Module (schematic)

- Self-supported units of double MMs (back to back)
- Space points along tracks by operating MM as µTPC

  Number of space points is function of track angle and strip pitch

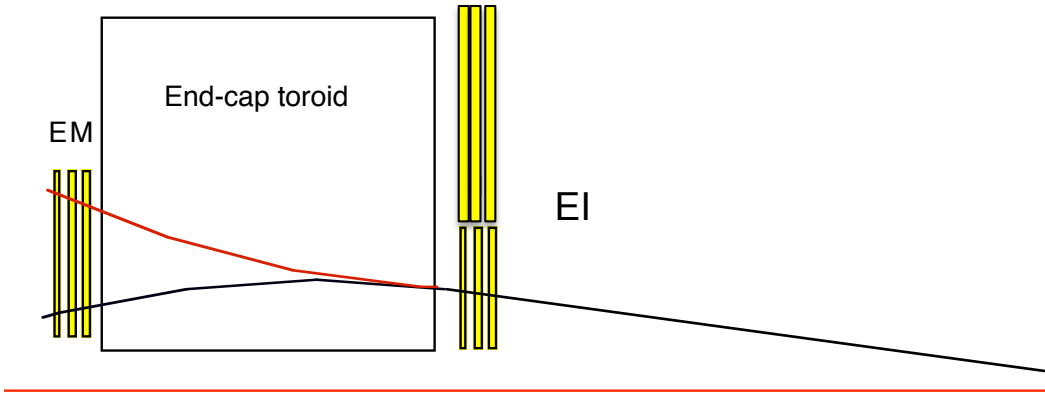
  Out-of-time tracks not aligned
- Trigger and/or 2nd coordinate by thinner separate double-gap units, wider strips and/or pads, … or 2-dimensional readout pattern



ATLAS upgrade - Phase II

- Three multigap chambers to replace all EI MDTs and CSCs
  - 288 chambers of $\Delta r \approx 1100$ mm
  - Strip pitch: 500 (or 250) µm
  - Max strip length: 1 m
  - 5–10k channels/chamber
- Three multigap chambers to replace EM MDTs + TGCs for $\eta > 2$
  - 96 chambers of $\Delta r \approx 1700$ mm
  - 7–15 k channels/chamber
- All chambers vertically installed
- Total MM area close to 2000 m^2
- Total # of channels : 2.25 M
  (4.5 M for 250 µm strip pitch)

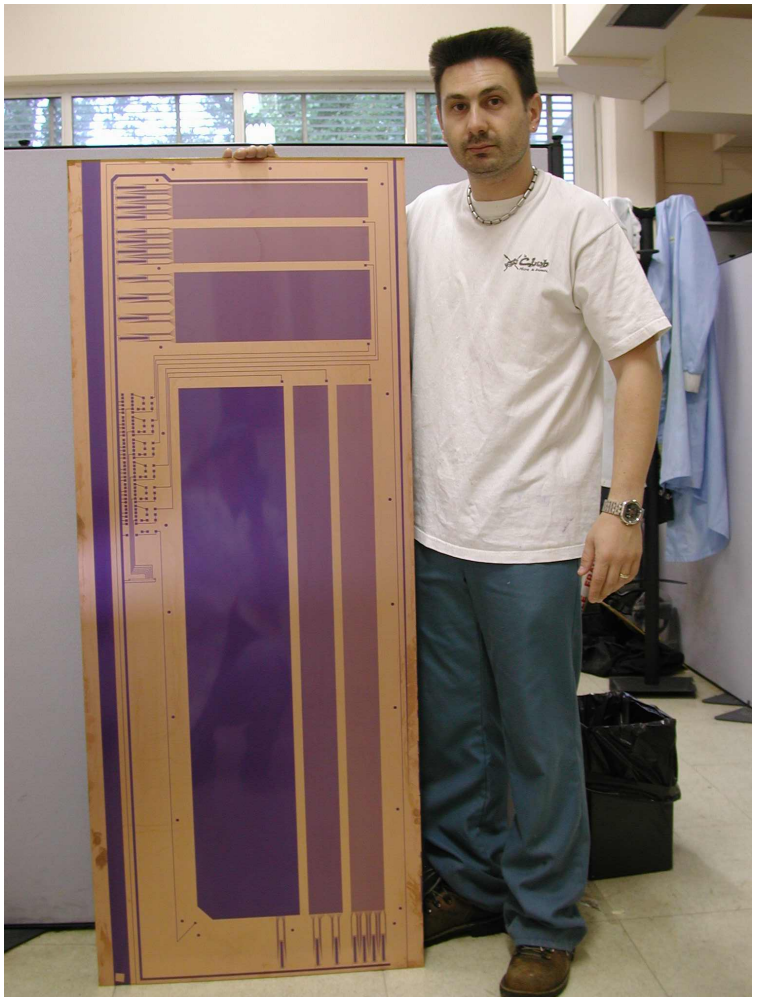
- Trigger:
  - Bunch ID from thin gaps (pads) from first time signals (<5 ns)
  - Fast-or for LV1 decision
  - Track angle (LV1) from time measurement on precision strips



What needs to be done

- Full-size prototype for Phase I as basis for the ATLAS upgrade LoI
  1. Show that MMs with the required performance and size can be constructed (in industry)
  2. Come up with a convincing concept for spark reduction
  3. Define readout plane segmentation, precision and trigger
  4. Specify electronics and readout system

On the road to large area detectors



New in prototype chambers 2009

- 100 x 100 mm^2 chambers with 250 µm strip pitch & better mesh (450 lpi, 18 µm wires, pre-stretched) compared to P1 prototype

  T2K connectors, read out with T2K electronics or other

  Detector performance and resistive coating studies
- 1500 x 500 mm^2 prototype (half-size)

  Segmented mesh, 250 and 500 µm strip pitches, longer strips (350 & 850 mm)

Mamma Pilot run 4-9 June 2009

- Saclay/Irfu joined the H6 beam test with 2 main goals:

1. Comparative study of standard bulk and resistive anode bulks (2 techniques : resistive ink and carbon-loaded kapton, several strip pitches). Several aspects : spark rate, spark tolerance, high hadron rate behaviour, space resolution.

2. Adaptation of T2K electronics to a standard bulk detector (216 strips, 250 µm)

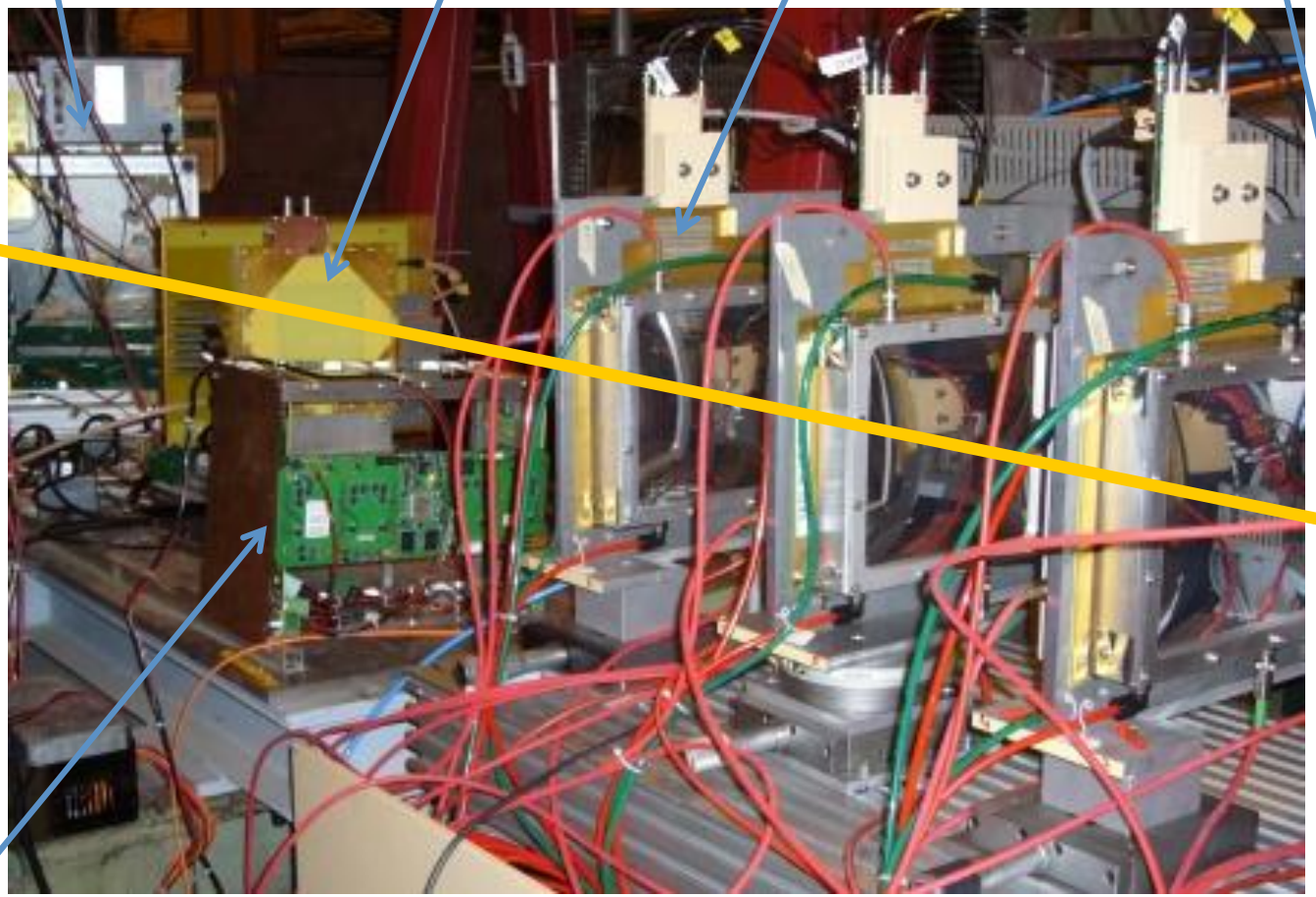
- « pilot run » in all respects: first time the detectors were in a hadron beam, first collaborative action in MAMMA, new (Gassiplex and AFTER – based) DAQs.

Transparencies by P. Colas

‘Old’ CERN detector

New CERN detector
with T2K connectors

Micromegas telescope (3 xy stations)
+ résistive detector + (standard)
probe detectors.
Gassiplex readout



Beam

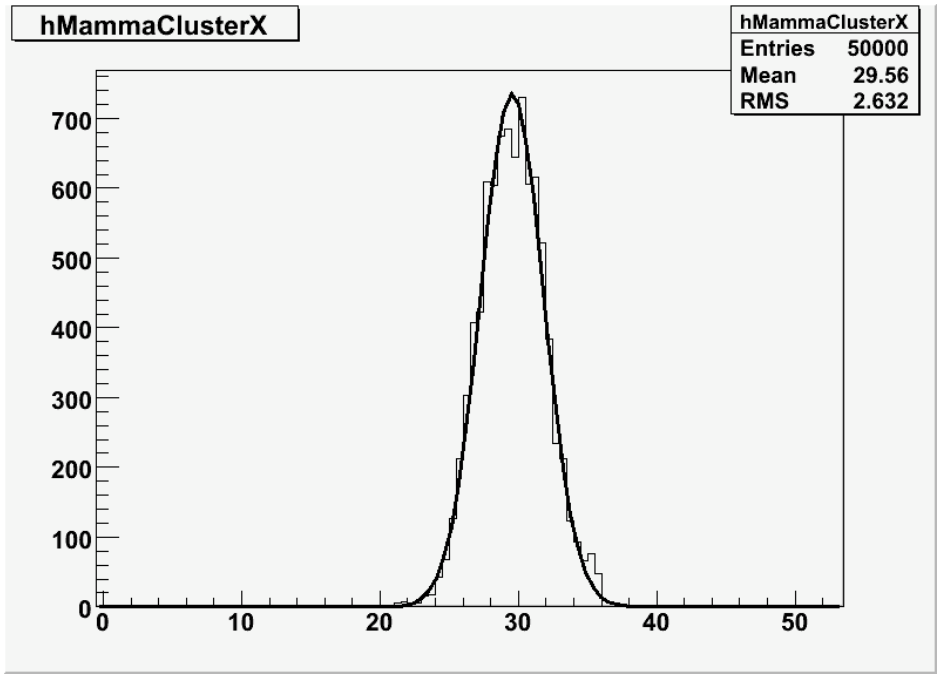
T2K electronics

SETUP

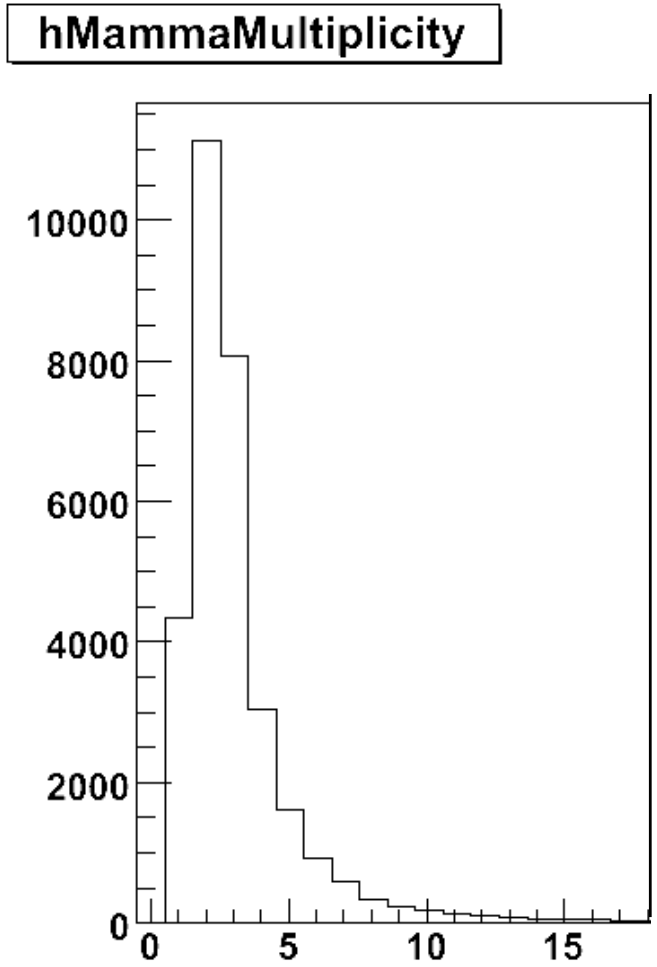
Transparencies by P. Colas

RESULTS

Much less and very different sparks on resistive detectors.
It is very difficult to measure and count sparks.
Continuous sparking above 425 V.



Beam profile by the 250 µm – pitch detector

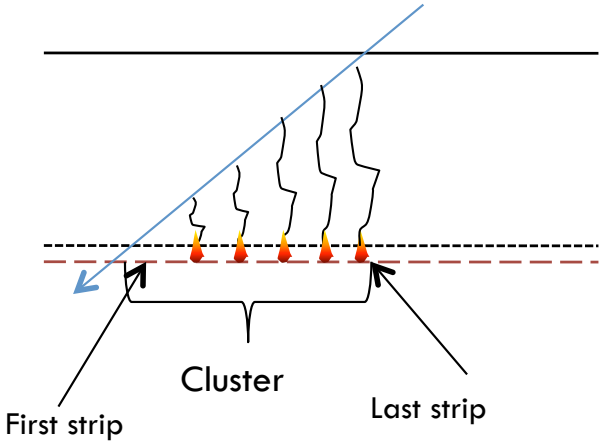


Number of strips
(mean : 3.3)

Transparencies by P. Colas

μ-TPC principle

Reconstruct track coordinates in the drift volume
Needs measurement of signal arrival time for each strip/pad



- track vectors to help pattern recognition and track reconstruction

- solves the problem of the degradation of the spatial resolution for inclined tracks

- potentially powerful tool for background rejection (track not coming from IP)

- if it can be used in the LV1 trigger (requires on-chip local track reconstruction) it will solve the problem of muon trigger rate at SLHC

Typical parameters

- Track angles for CSC coverage: 10–20°, if MM vertical
- Drift gap: 7 mm => footprint: 1–2 mm
- Strip pitch: 250 µm => 4–8 strips see signal
- Average number of primary electrons (Ar): 15–20
- Max drift time: 100–200 ns (v_{drift} = 7–3.5 cm/µs)
- Drift time range 'per strip': 20–35 ns

$\Rightarrow$ Requirements on readout electronics

  - Time resolution of a few ns
  - Charge measurement is needed but can be coarse (8–10 bit ADC), integration time 20–100 ns, to be optimized

Electronics

- Many chips available that have some of the desired functionality, but none has all
- New schedule allows for development of new electronics
- BNL are ready to undertake a preliminary design effort
- Estimated time for the production/availability of a new chip: 3 yrs

Chip specifications (preliminary)

- 128 channels/chip (preamplifier, shaper, peak amplitude detector, ADC)
- Peaking time >20 ns; dynamic range: 80 fC
- Fast trigger of all and/or group of channels on chip
- Rate: 100 kHz
- Input capacitance: up to 250 pF
- On-chip zero suppression
- SEU tolerant logic

A similar chip (but much longer integration time and smaller rate capability) exists at BNL; we will try to have some readout electronics based on this for the test beam at the end of 2009

Next steps

- Try different front-end electronics and readout (T2K, CSC, BNL, …)
- Final specifications for readout electronics by end 2009
- Study of spark reduction/protection (Saclay)
- Evaluate 1.5 x 0.5 m^2 prototype during summer and fall 2009
- Design of CSC-size prototype in fall of 2009; to be constructed in 2010 (in industry, in collaboration with BNL and CERN)
  - Size: 1.2 x 1.2 m^2
  - Chamber with several bulk micromegas for precision/trigger/2nd co-ordinate planes
- Start work on integration in ATLAS …
  - Aim to have a realistic layout for the ATLAS upgrade LoI in 2010