

# Huazhong Normal University (Wuhan) activities within RD51 scalable readout project



FEE card produced in Huazhong Normal University for ALICE/PHOS project



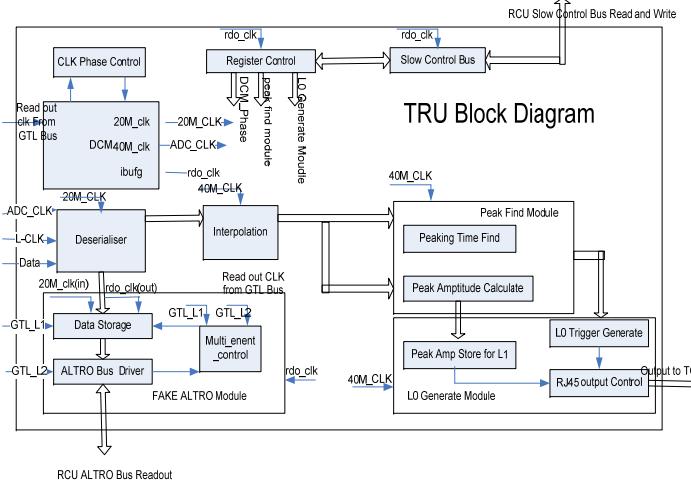
Readout Electronics Test Setup

6/16/2009

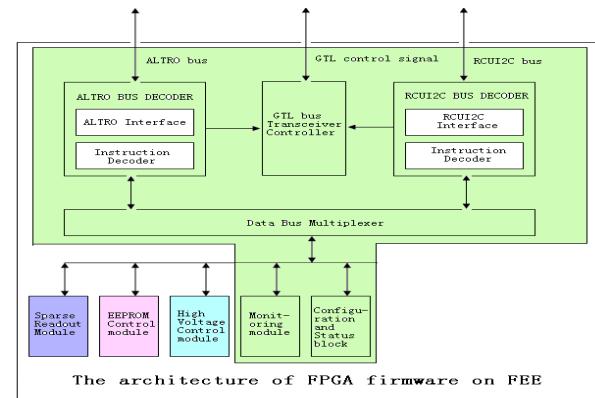


Altro-based FEE card for APD readout

Dong Wang , CCNU Wuhan

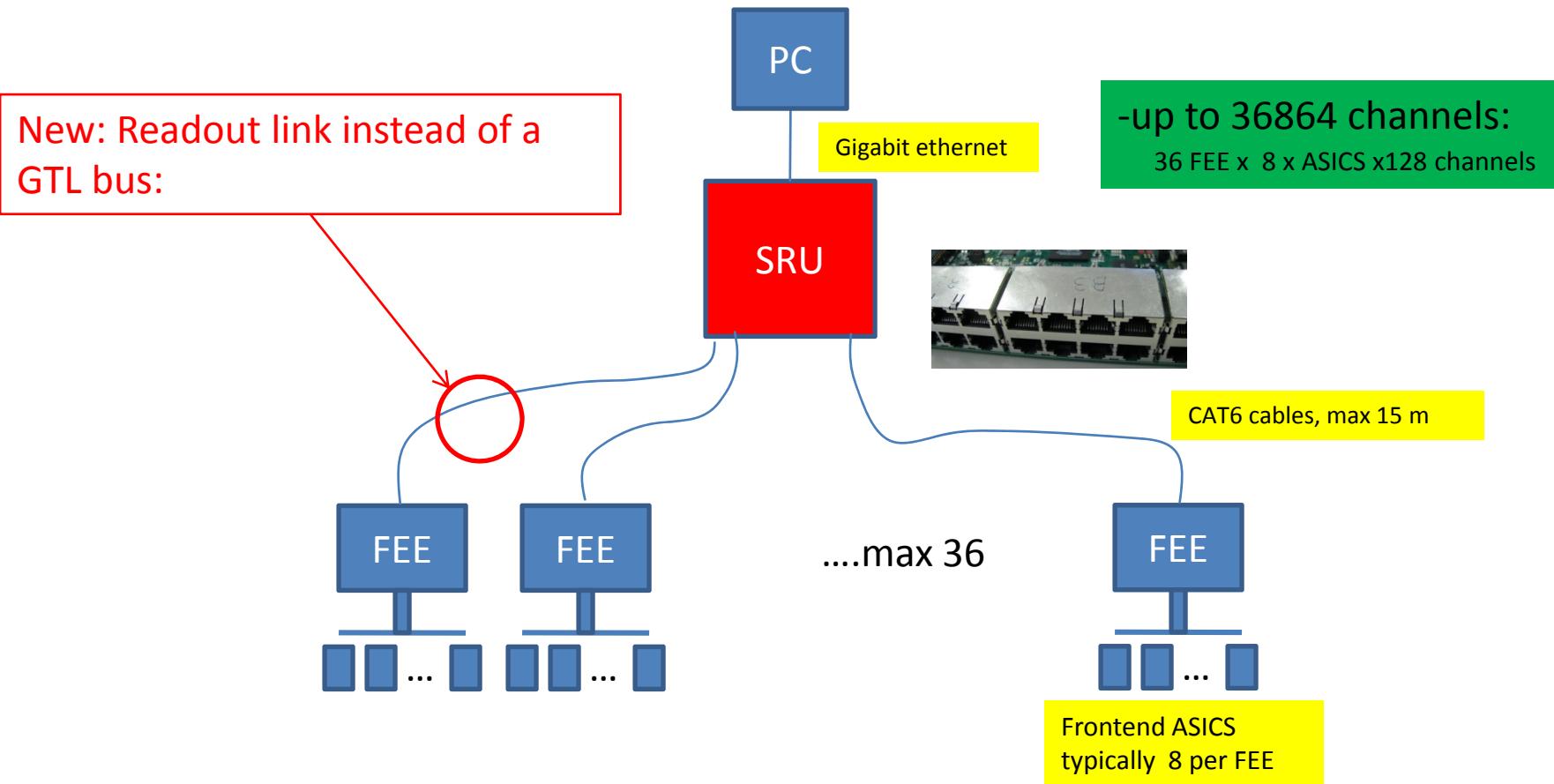


Firmware of PHOS/TRU trigger cards



Board Controller Firmware of FEE & Participation in ALICE RCU firmware

# Simple SRU system



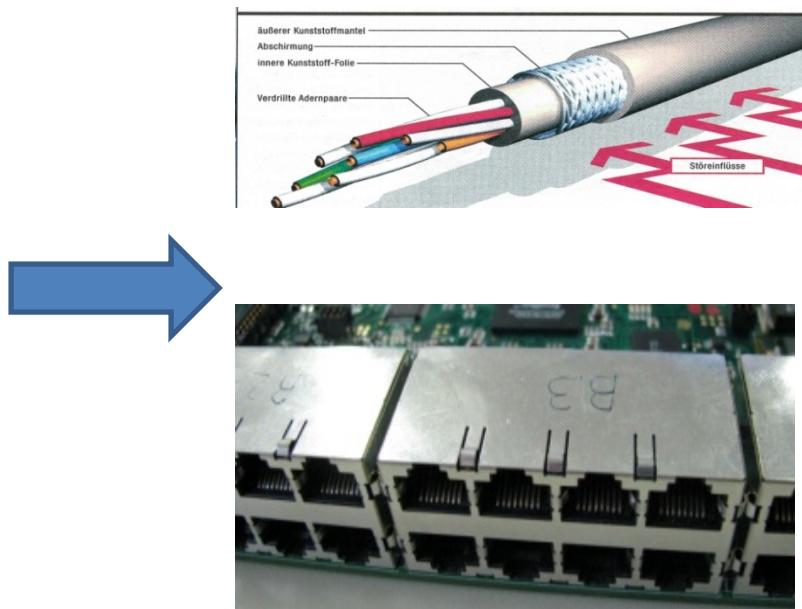
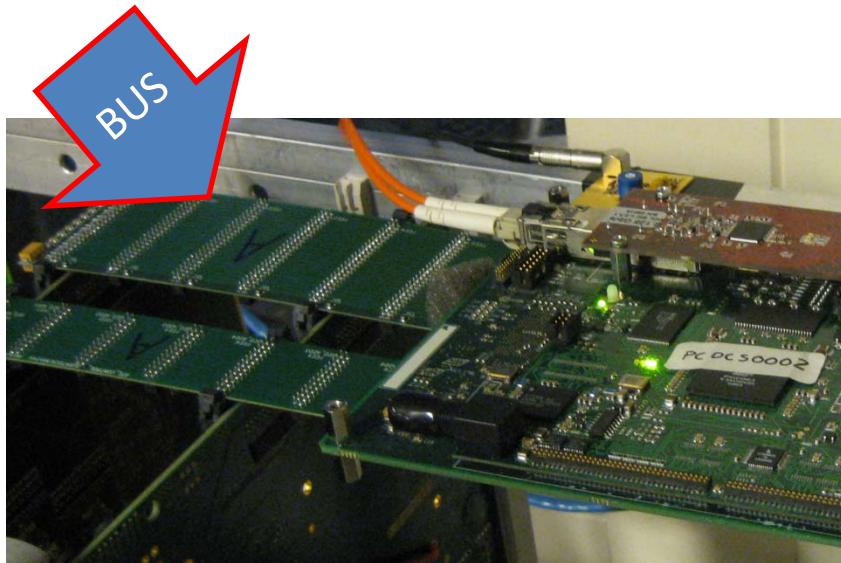
# From readout bus to readout link

Point to Point link architecture:

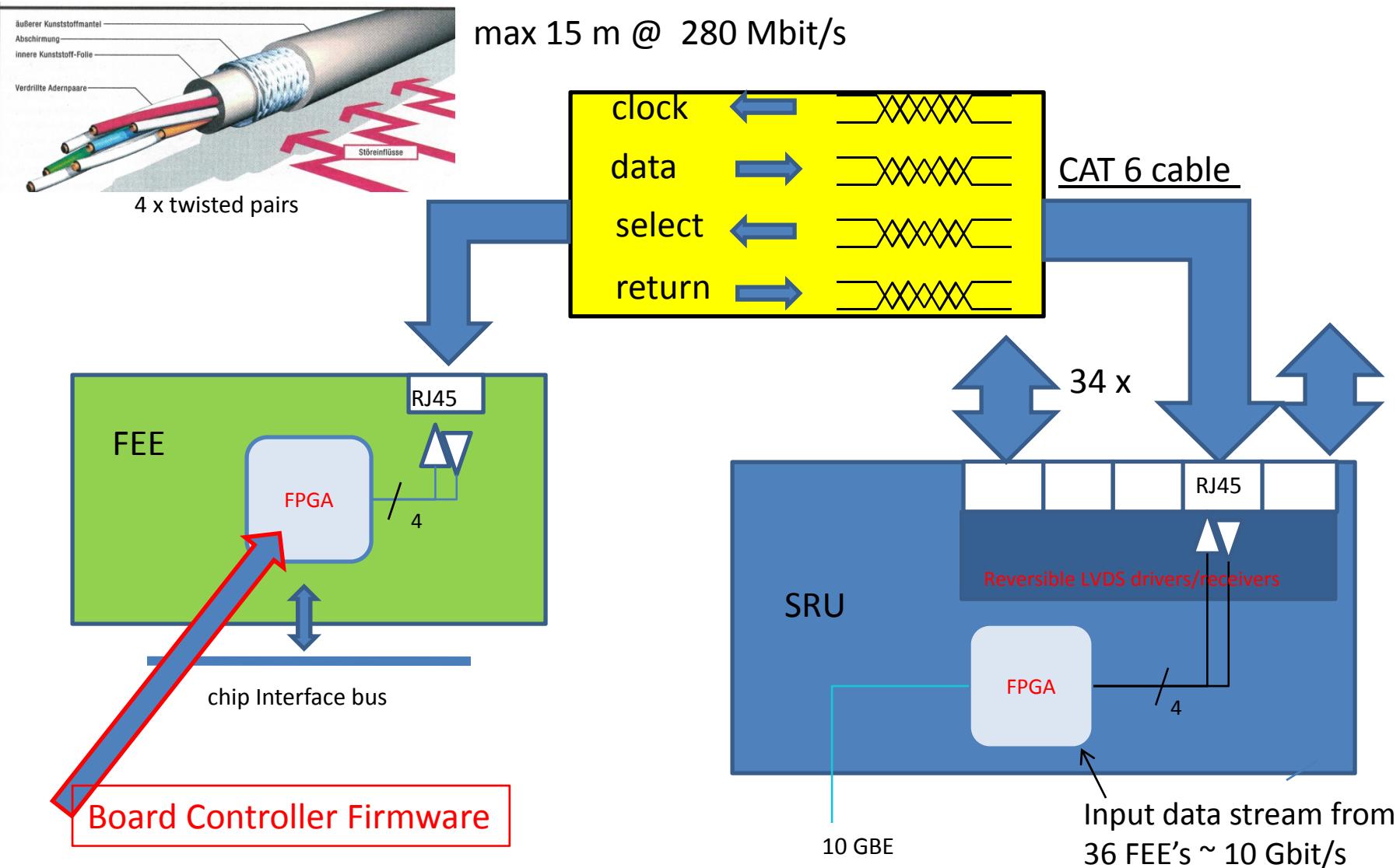
- well defined impedance both ends, longer distance than bus
- single node failure does not influence other nodes
- parallel transfers on all links, i.e. higher total BW
- cheaper by using off the shelf cables
- Much less contacts , longer life

Status so far:

- tested with 280MHz clk and 15 Meter over CAT6 cable
- use simple packet protocol



# SRU<->FEE: serial LVDS



# Serial readout/control modes

2 modes of operation defined by SCU clock  
Board controller senses clock to switch mode

Readout mode: **clock = 40 MHz ( or other )**

data = 200 Mbit/s

select = readout-trigger to FEE

return = local trigger from FEE

Control mode: **clock <= 4 MHz**

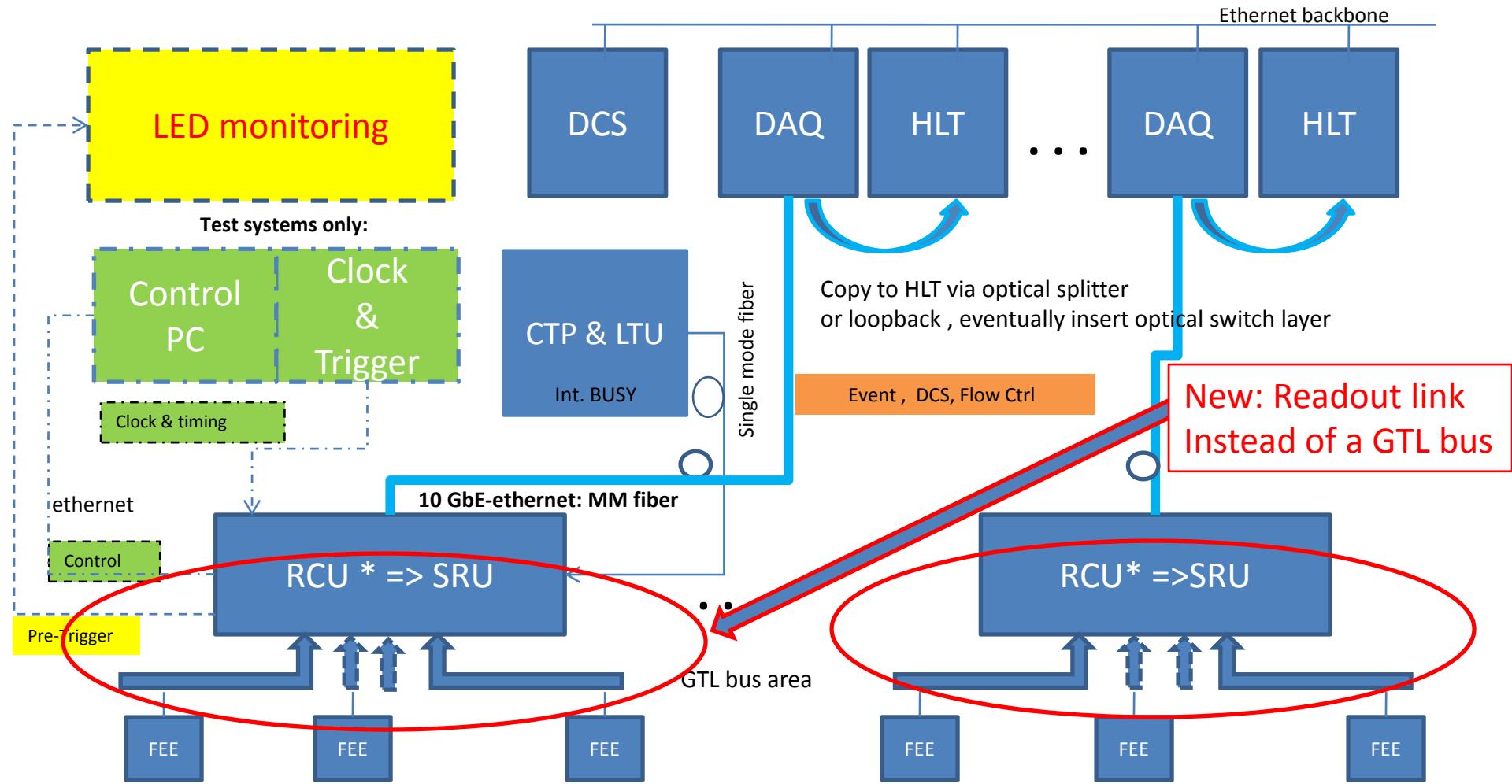
data = Serial data out

select = Serial data in

return = coded status

# =>ALICE case study\*

## for PHOS, EMCal, etc.



# Upgrade Board Controller FPGA firmware

- New feature of ALTRO CHIP read and serial data push out will be added in the FEE Board controller
- The deserialiser and decoding part will be revised from the PHOS/TRU firmware

