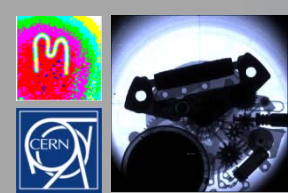




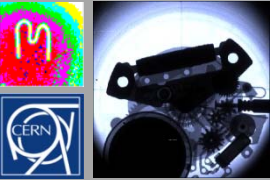
MEDIPIX3 TESTING STATUS

R. Ballabriga and X. Llopart



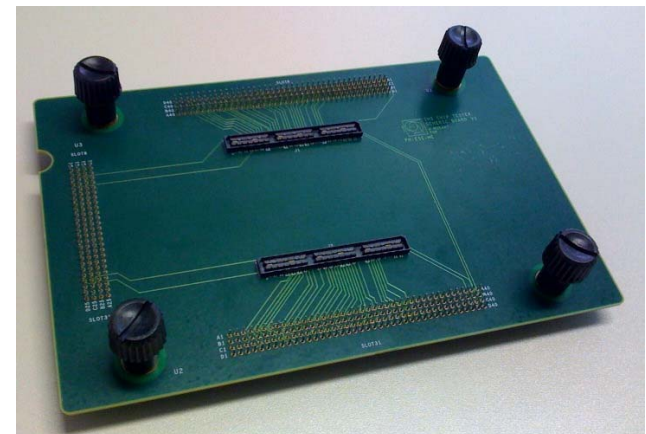
Medipix3

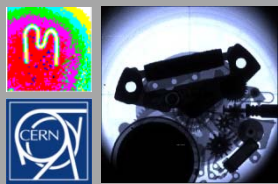
- Pixel functionality:
 - Single pixel mode or charge summing mode:
 - 55 x 55 μm pixels with 2 thresholds
 - 110 x 110 μm pixels with 8 thresholds
- Counting:
 - 2 programmable counters with overflow (1, 4 or 12 bits) or 1-24bit.
 - Full-Sequential , Semi-Sequential or Continuous Read Write modes.
- Readout:
 - Configurable LVDS readout link: 1 (250 Mbps) to 8 lines (2Gbps)
 - Matrix readout by blocks (ROI):
 - Selectable Column Block Readout (32, 64, 128 or 256)
 - Selectable Row Block Readout (1, 2, 4, 8, 16, 32, 64, 128 or 256)
 - Fast pixel Reset: MatrixFastClear : 192ns @ 250MHz
- Connectivity:
 - On-chip test pulse generator
 - E-fuses for chip identification
 - TVS (Through Via Silicon) connection possible



The IC tester

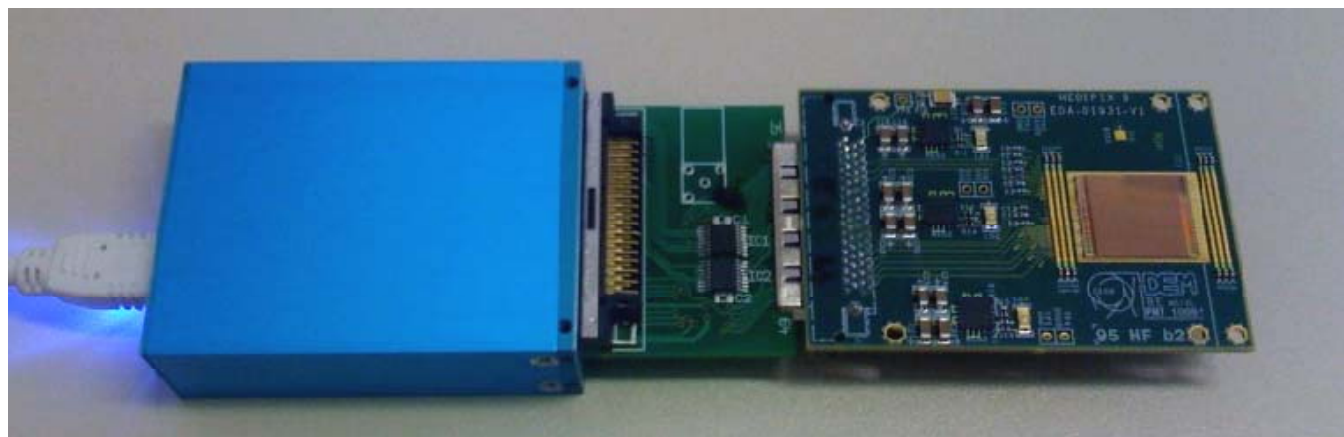
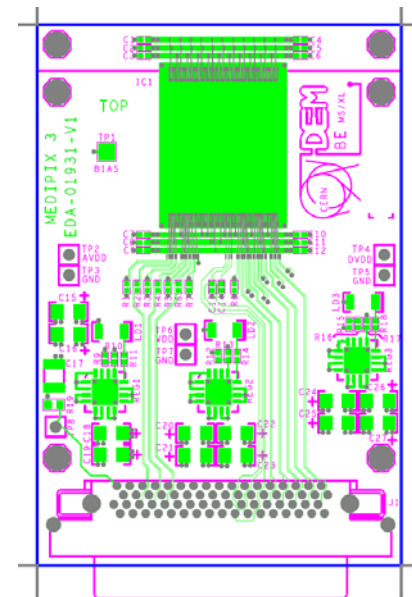
- 2 boards have being produced to interface the CERN IC tester with the Medipix3 chip:
 - IMS generic board
 - Medipix3 mezzanine

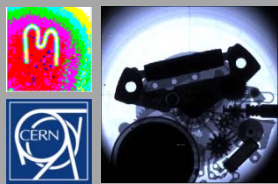




USB Interface

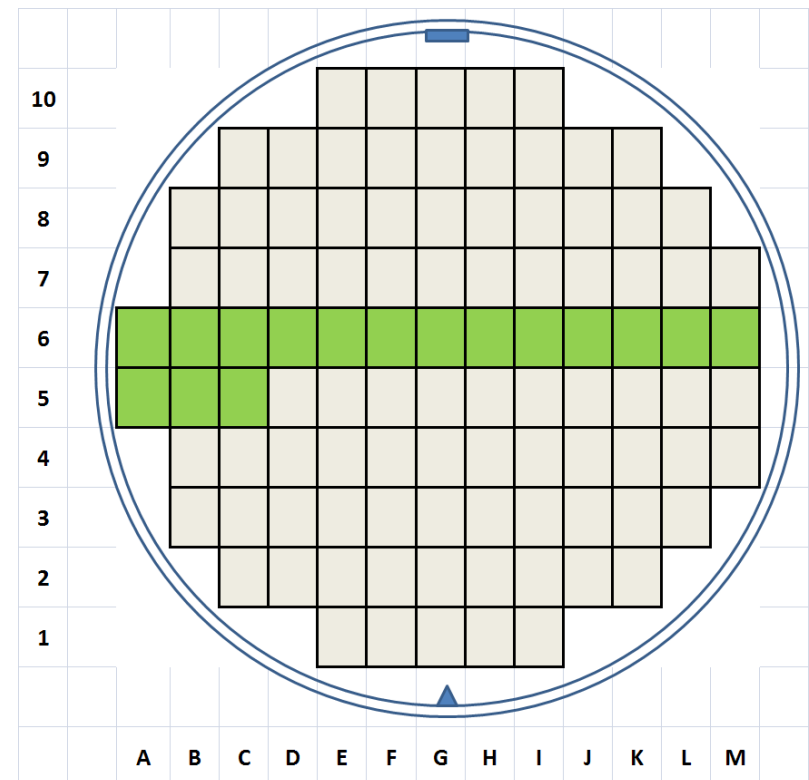
- USB v.122 used by the Medipix2 & Timepix
- Software and USB μ C firmware has been updated
- Readout clock frequency $\sim 5\text{MHz}$
- Very versatile
- New chip carrier PCB design using the same VHDCI interface

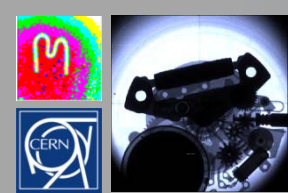




Medipix3 Testing

- Half-diced Medipix3 wafer came back on 2nd February.
- Testing started the 5th February in the IC Tester
- We mounted in total 16 chips :
 - 6 for the IC tester
 - 4 bonded in both sides
 - 2 with the top WB pads diced off
 - 10 for the USB interface
 - 7 bonded in both sides
 - 3 with the top WB pads diced off



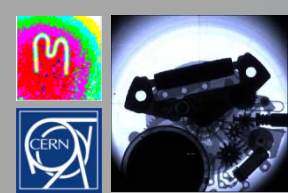


Measure ID (VDDA, VDD and DVDD) after Reset

- **Test flow is: Reset + SetDACs + Fast Matrix Reset + Measure power supply currents in static mode**

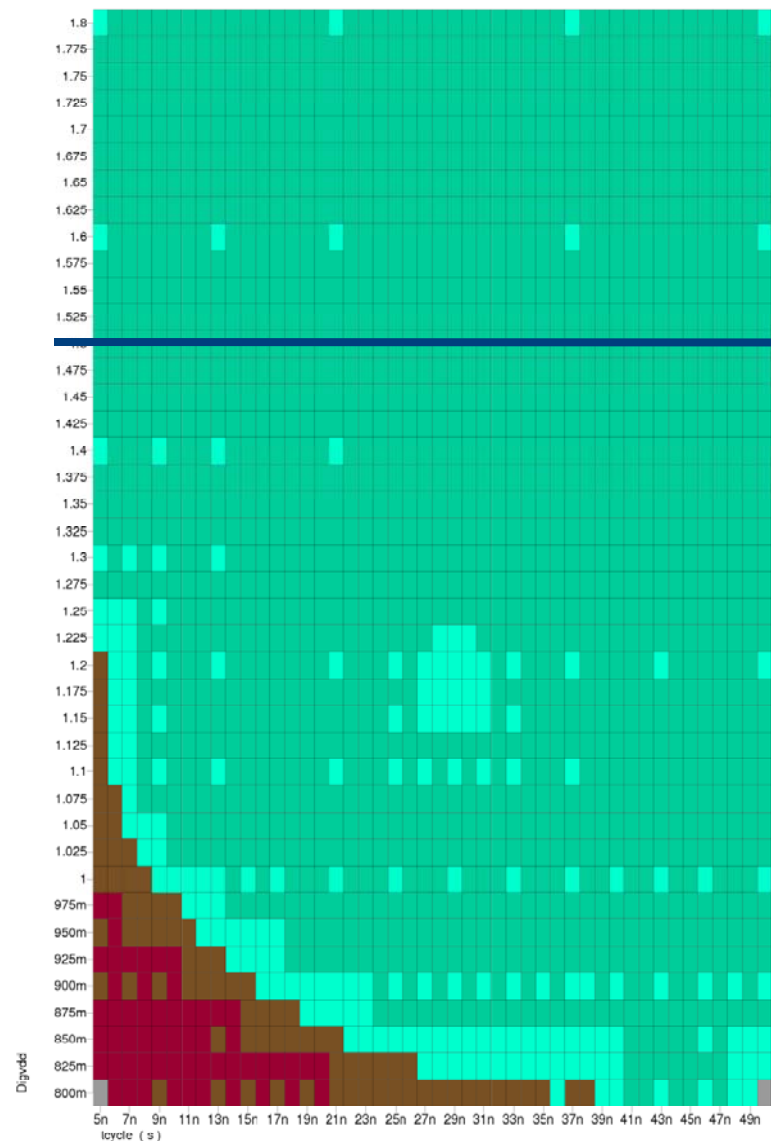
	Mode	Manual	A6	B6	C6	D6	NPT1	NPT2
AVDD [mA]	CS	600	540	536	498	558	496	850
VDD [mA]	CS		7.8	12.7	13.3	95	32.6	40.8
AVDD [mA]	SP	400	388	384	364	437	385	510
VDD [mA]	SP		4.4	7.2	9.2	91.6	26	24.1
DVDD=2.5V [mA]	SP/CS	51.4	51.1	50	50.8	50.3	51.3	51

- **All chips show similar (not NPT2) total analog current for the same DAC settings in SP and CS mode.**
- **The DVDD (LVDS driver/receiver) fits very nicely for all chips.**
- **We have still to measure the VDD current consumption versus frequency**



Write and Read DACs

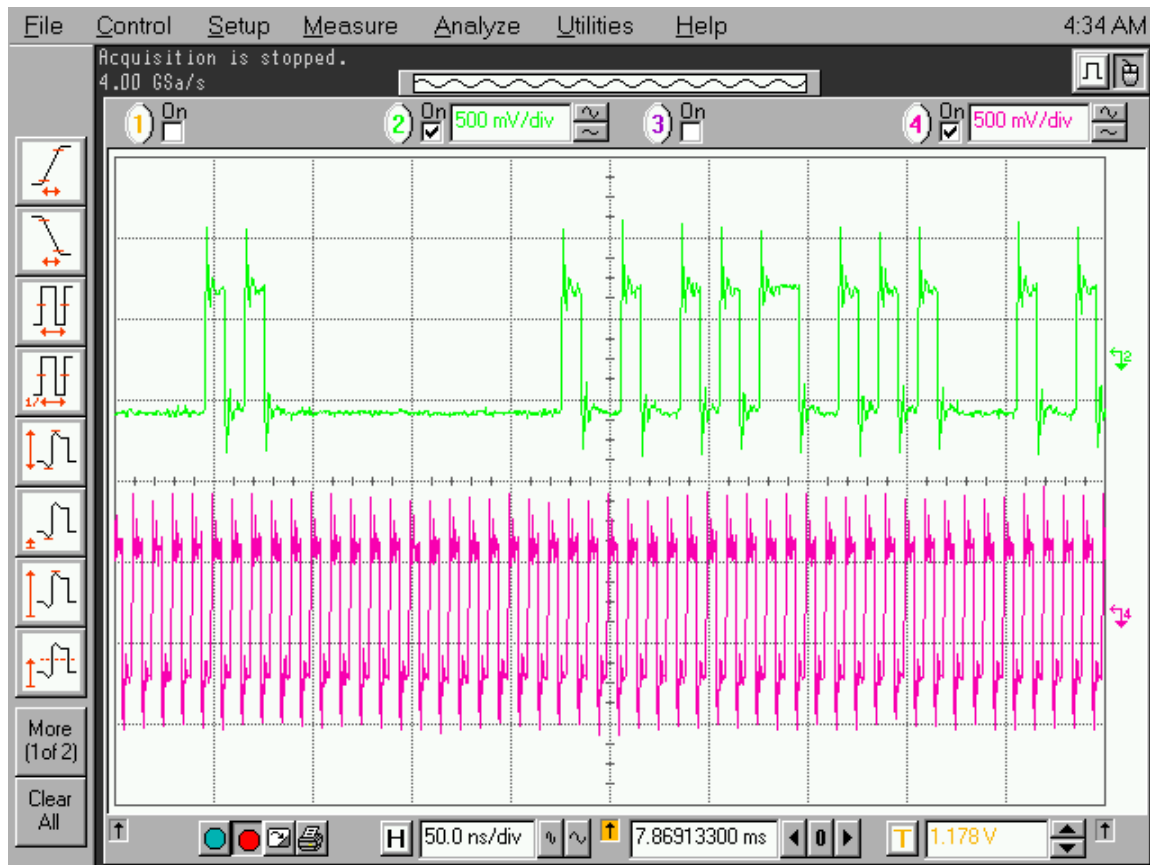
- Digital test that compares the DAC register contents written to chip and read out.
- Shmoo plot: “is a graphical display of the response of a component or system varying over a range of conditions and inputs”
- VDD [0.8 to 1.8V] and clock frequency [20 to 200 MHz] are scanned
- All 6 tested chips pass this test



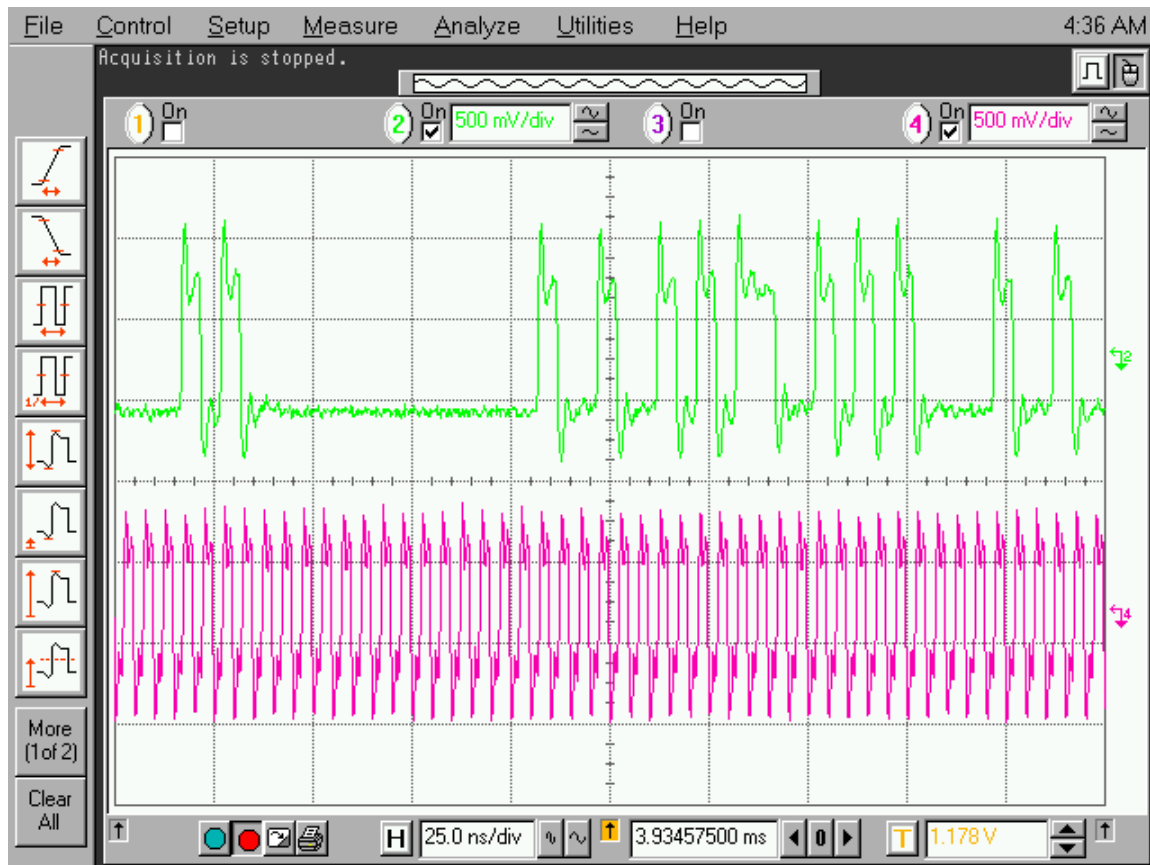
Data and clock from the chip (10 Mbps)

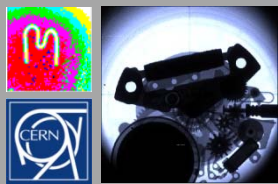


Data and clock from the chip (100 Mbps)



Data and clock from the chip (200 Mbps)

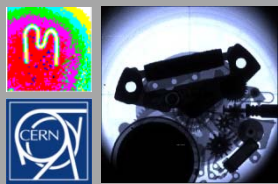




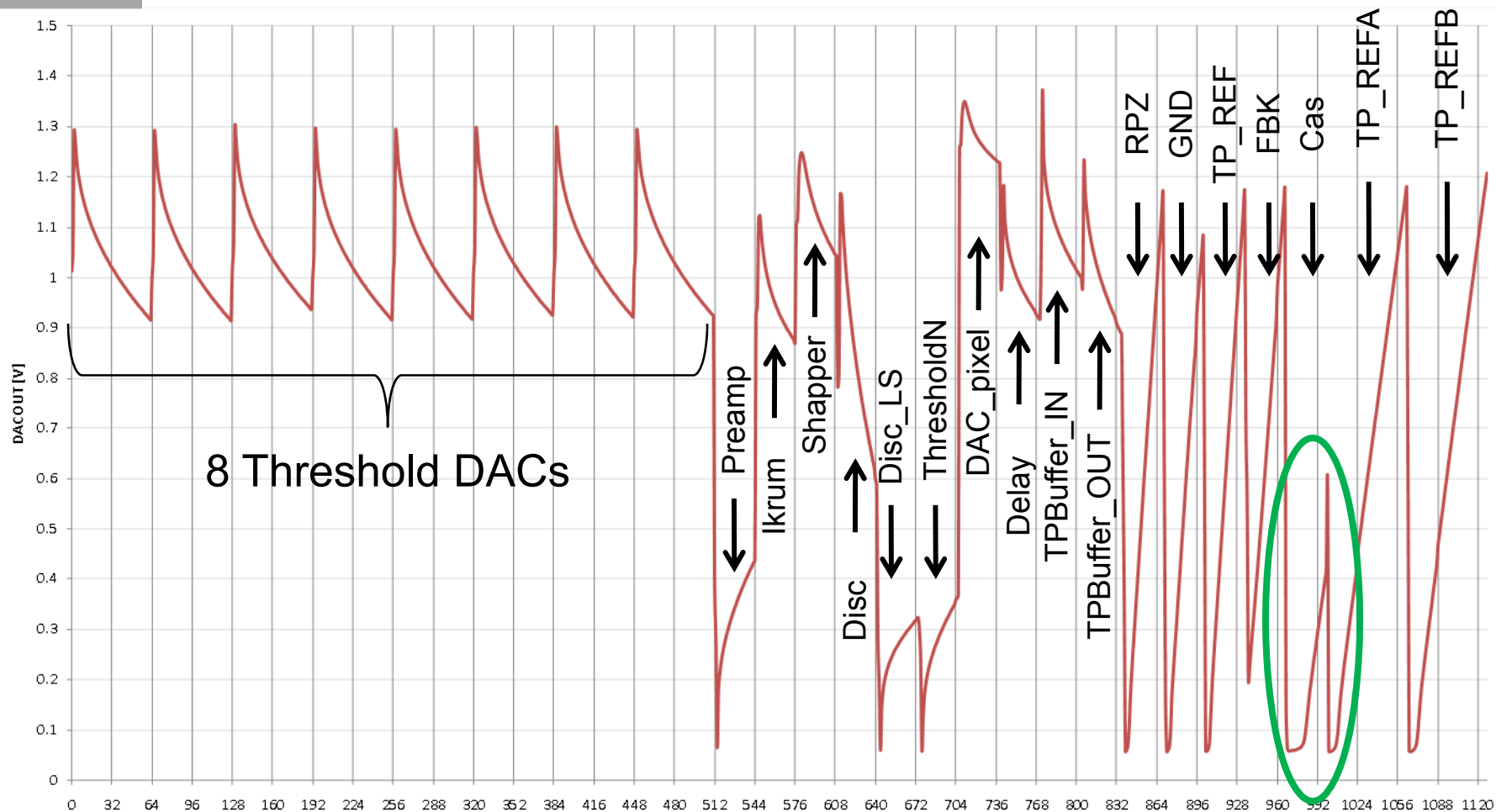
ClockOut DataOut delay

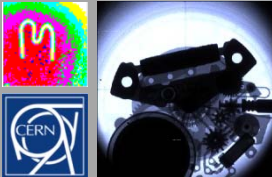
- Delay of $\sim 2\text{ns}$ between ClockOut and DataOut. Can be corrected in the readout system?
- The DataOut[0:7] skew is well below $<1\text{ns}$. To be measured...





DACs SCAN

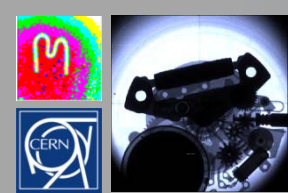




DACs Scans (II)

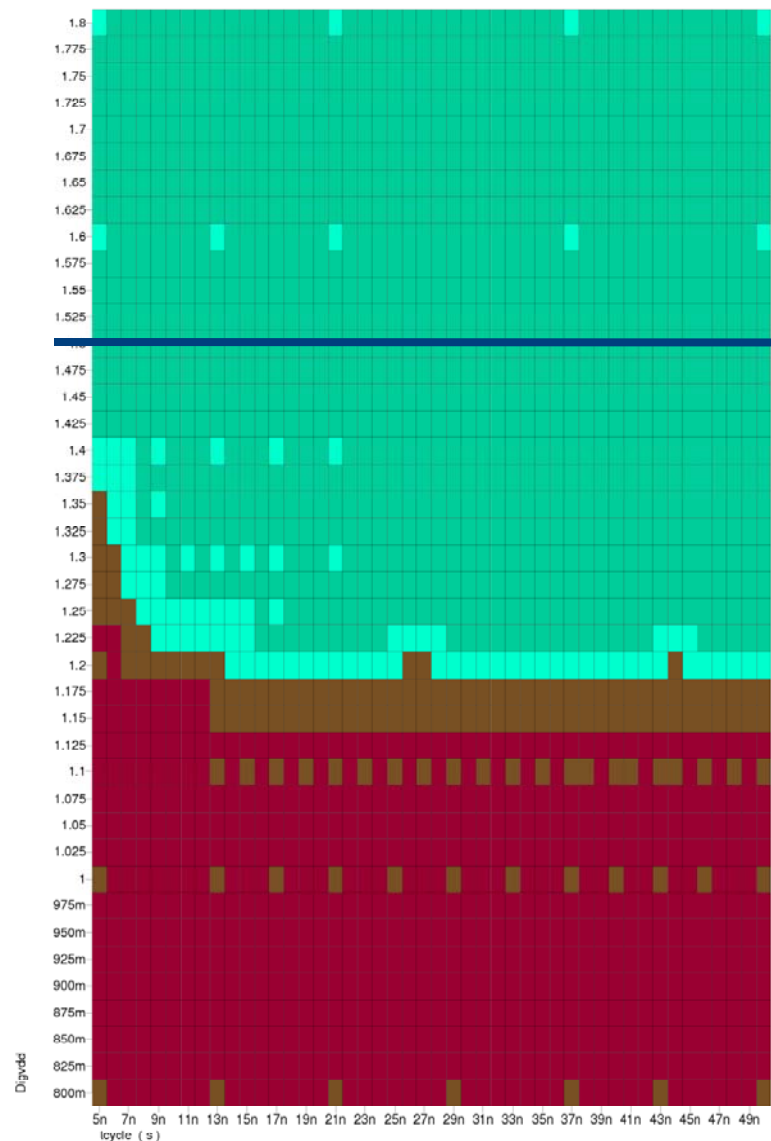
- All tested chips show similar DAC curves
- Very good agreement with simulated values
- Also the Temperature sensor seems to work but it should be properly calibrated
- Cas DAC will need to be imposed externally using the EXT_DAC input.

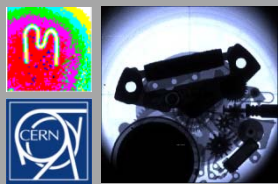
	Simulated values (After Reset)	Measured A6 DACs (After Reset)
Threshold[0]	255 nA (1.05 V)	1.027 V
Threshold[1]		1.027 V
Threshold[2]		1.036 V
Threshold[3]		1.028 V
Threshold[4]		1.025 V
Threshold[5]		1.023 V
Threshold[6]		1.03 V
Threshold[7]		1.025 V
Preamp	2.56 μ A (355 mV)	355 mV
lkrum	25.6 nA (970 mV)	970 mV
Shapper	512 nA (1.03 V)	1.115 mV
Disc	1.024 μ A (0.84 V)	794 mV
Disc_LS	512 nA (270 mV)	265 mV
ThresholdN	512 nA (320 mV)	303 mV
DAC_pixel	17 nA (1.25 V)	1.289 V
Delay	102.4 nA (1.02 V)	982 mV
TP_BufferIn	5.12 μ A (1.12 V)	1.08 V
TP_BufferOut	128 μ A (1.04 V)	983 mV
RPZ	640 mV	607 mV
GND	640 mV	602 mV
TP_REF	640 mV	583 mV
FBK	640 mV	688 mV
Cas	640 mV	78m V
TP_REFA	640 mV	609 mV
TP_REFB	640 mV	615 mV



Write & Read to pixel matrix

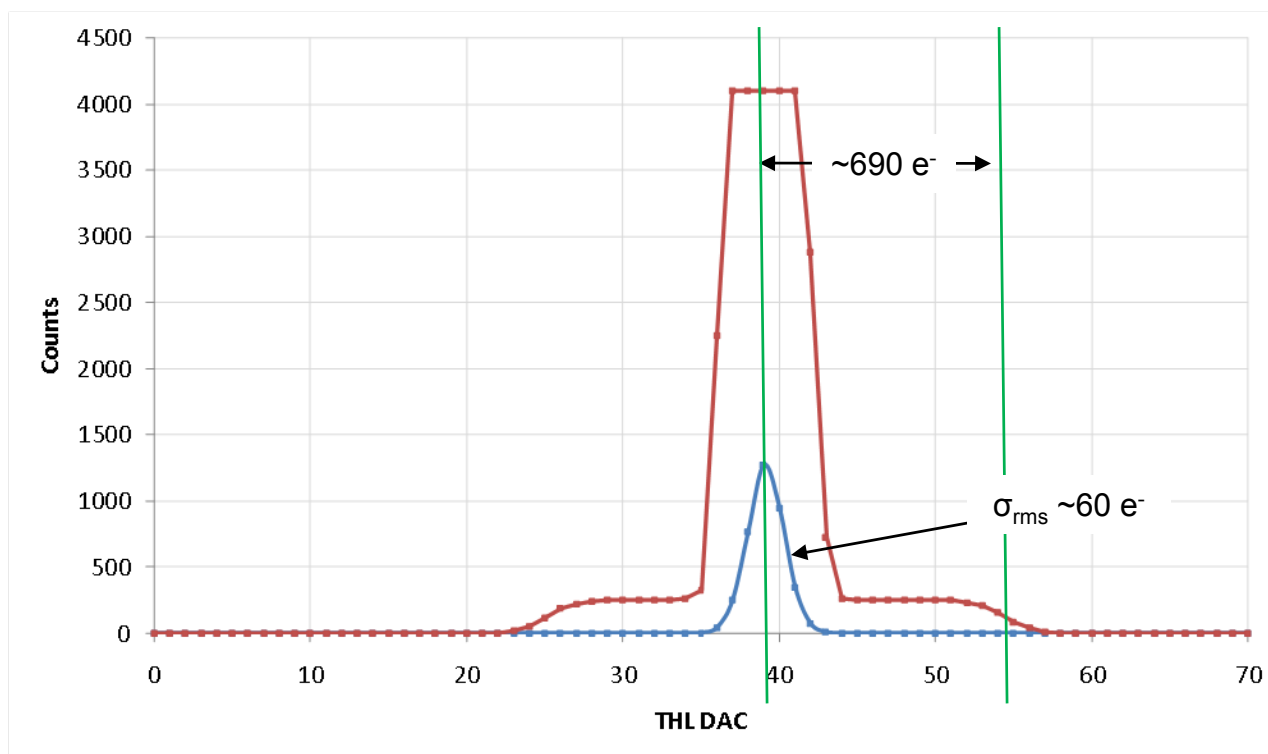
- Communication (write/read) to the pixel matrix has been tested successfully up to 1.6 Gbps (IC tester limit is 200 MHz)
- Chips only powered from the bottom or top.
- Region of interest readout works well
- From the 6 tested chips in the IC tester we have:
 - 2 class AA (all columns working)
 - 1 class AB (counter1 has 1 dead column)
 - 3 class CC (1 or 2 dead columns)

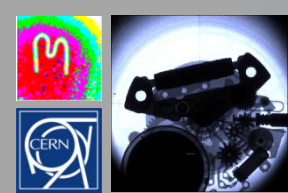




Pixel s-curve

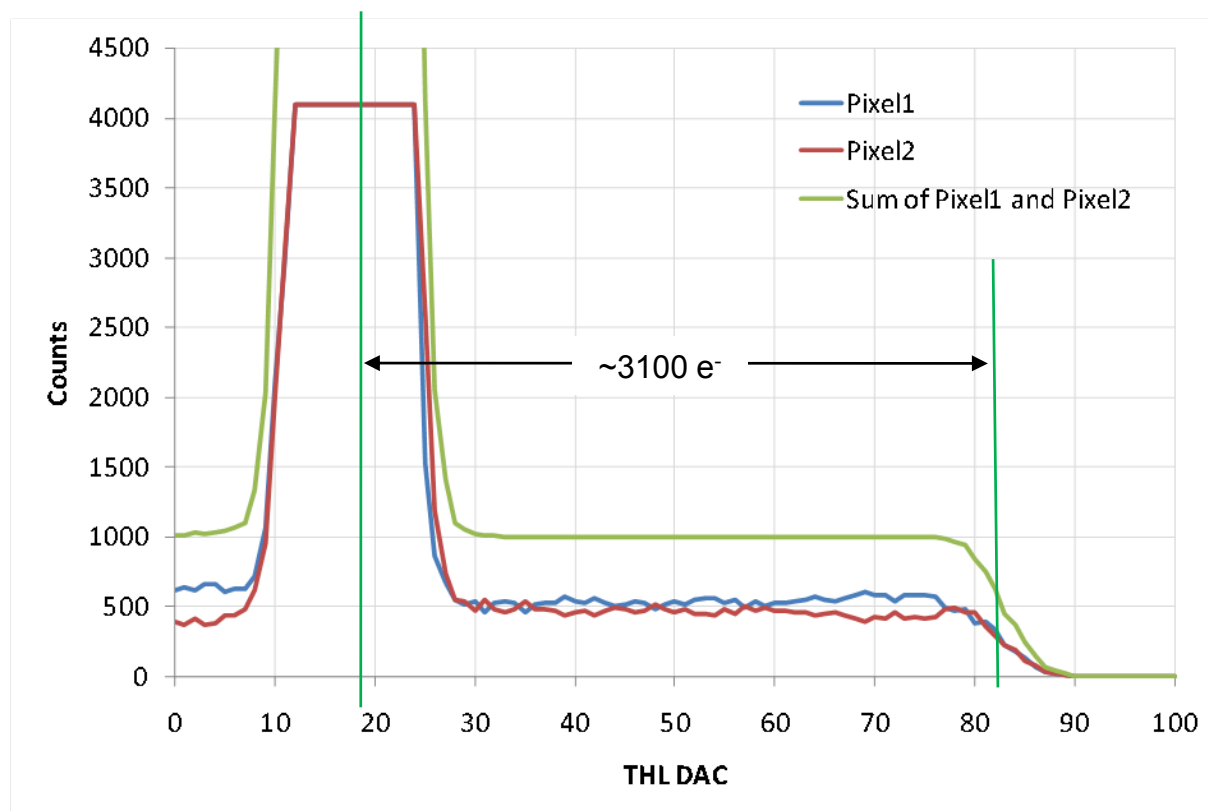
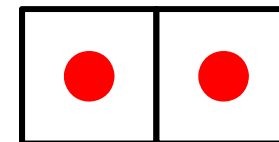
- Using the USB interface
- Using the S-curve method in a single pixel the ENC and gain can be extracted

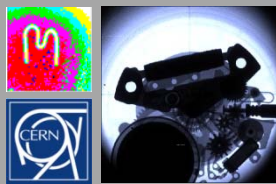




Charge summing

- Early measurements shows that the charge summing architecture works as expected





Conclusions

- **Medipix3 is operational**
- **Periphery:**
 - LVDS drivers/receivers, 24 DACs, e-fuses, IO logic, EndOfColumn, DAC registers, CTPR registers work as expected.
 - The Cas DAC must be external imposed to ~800 mV to bias the pixel front-end properly.
- **Pixel Matrix:**
 - Set Matrix, Readout in serial or parallel or ROI works as expected
 - In Full sequential mode the first s-curve show expected/simulated pixel noise (~60 e⁻)
 - No systematic top-down effect seems visible when powering the chip from only one side. First indications show a threshold variation after tuning of ~80 e⁻ in single pixel mode.
 - Charge summing mode looks very promising.
 - CRW mode has not been fully tested yet.
- **Several fast readout systems will soon be ready and compatible with Medipix3 (Relaxed board, MARS, RUIN, Prague and USB2.0)**