Time Projection Chamber with Triple GEM and Pixel Readout

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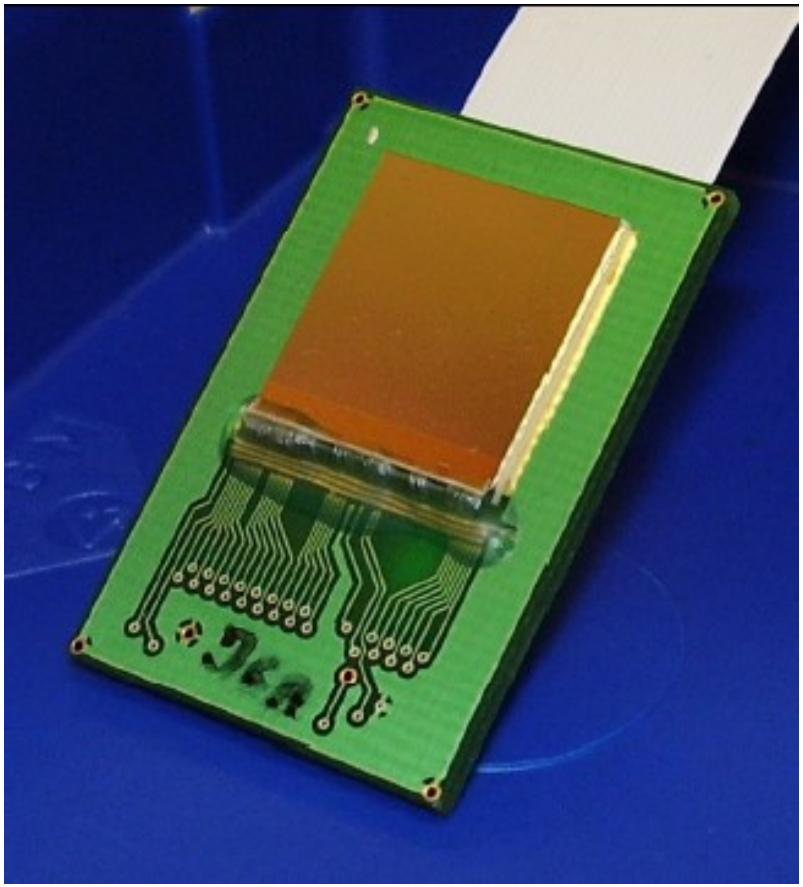
Timepix



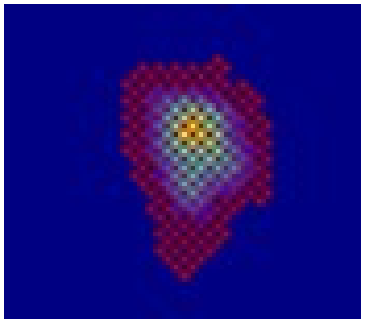
256 * 256 pixel

pixel size: 55 * 55 µm²

chip dimensions: 1.4 * 1.4 cm²

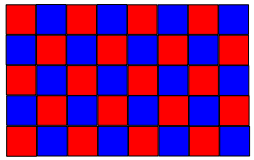
Each pixel can be set to one of these modes:

- hit counting
- TOT = time over threshold
  gives integrated charge
- time between hit and shutter end
- hit/no-hit

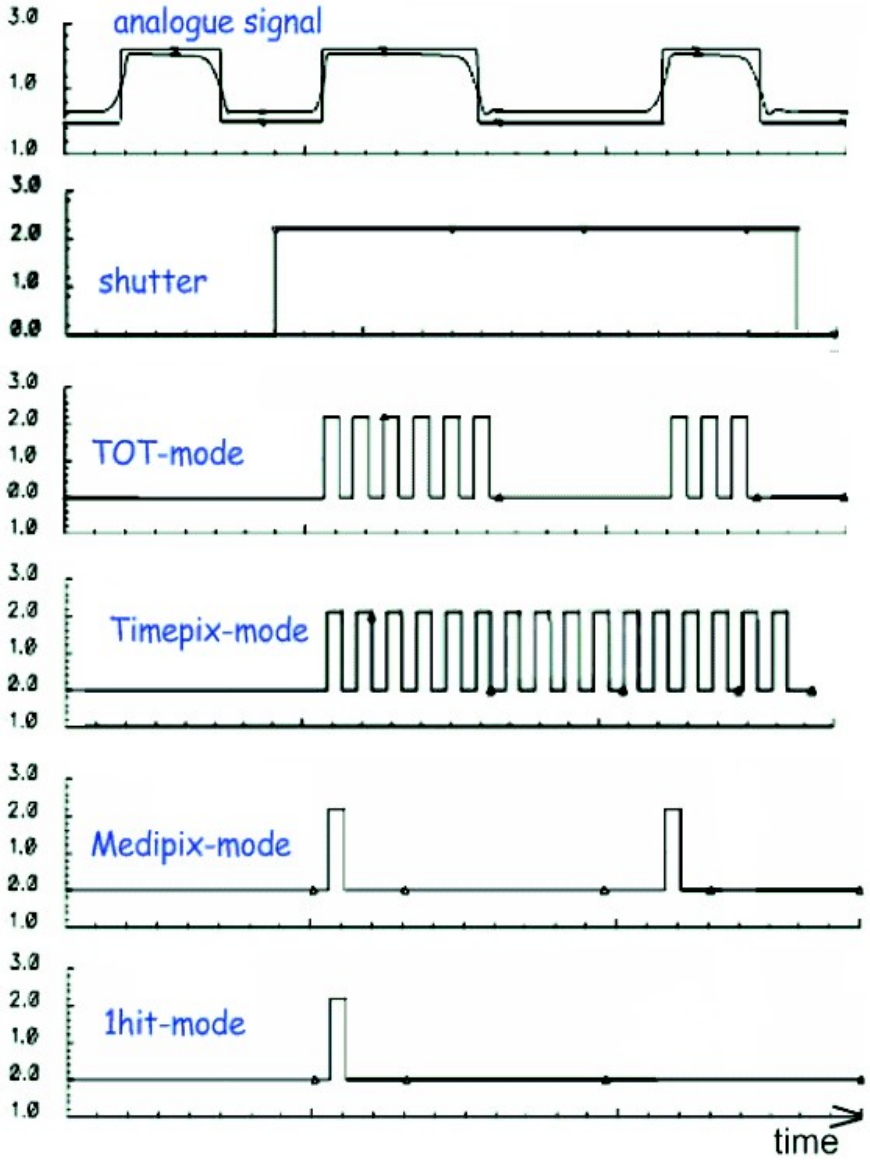


current running condition:

checker-board pattern of TOT and Time



Timepix modes



exit analog part

Shutter

ToT: charge integration

Timepix mode: measures time from signal to end of shutter

Medipix mode: counts hits

1-hit-Mode
binary

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Current readout options

single Chips and Quadboards have been built sofar:

MUROS: work good with single chips + Quadboards,
built by NIKHEF, not available/supported anymore

USB-device: built and supported by University of Prague
USB-device 1.1 could be made to work with single chips
USB-device 1.22 make Timepix Chip forget its DAC
Setting after 1 event, workaround exists
→ possibly the layout with flatband cable introduces delay or signal decay

Readout software: Pixelman 1.7.2, 1.9.1,
newest version does not support external shutter
Runs under Windows –
communication with rest of DAQ (Linux) is problematic

Many hardware bricolage-solutions were necessary for the testbeam

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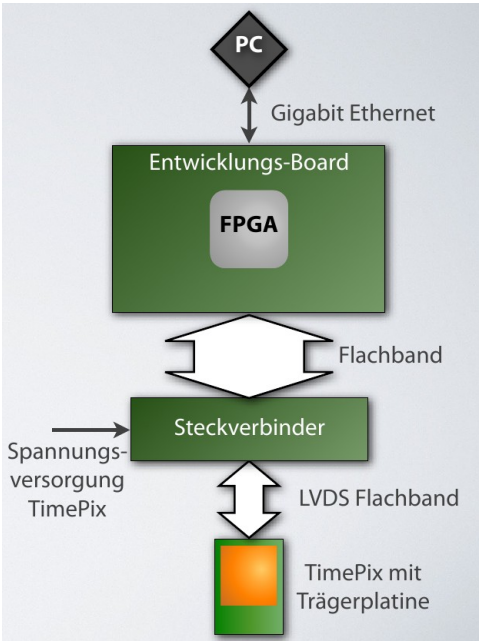
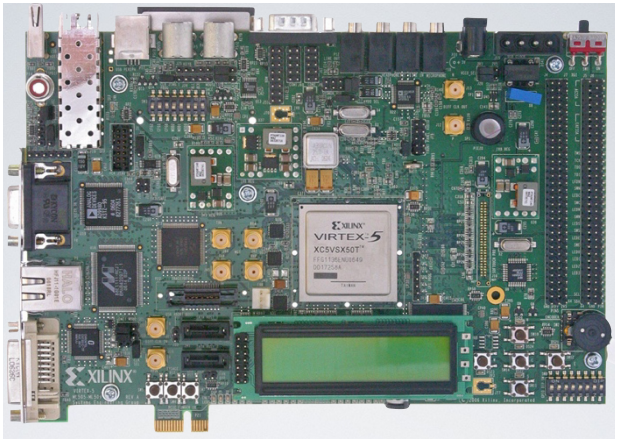
New FPGA-based Readoutsystem by University of Mainz

Mainz is designing and building a new FPGA-based readout for Timepix chips.

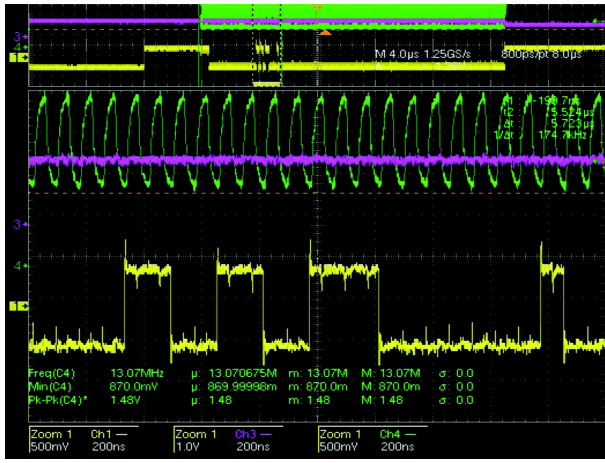


- Readout with maximum speed (100MHz)
- Connection to PC with Gigabit Ethernet
- FPGA:
  - De-/serialization of data streams
  - Conversion CMOS – LVDS
  - Firmware in VHDL



XYLINX–development board

- Software and firmware are in good shape but some missing functionality until now
- Serialization and ethernet communication are correct
- Not at full speed yet (needs matching of clock to delayed data stream in Timepix)
- Chip can be read out, test with detector at Bonn soon



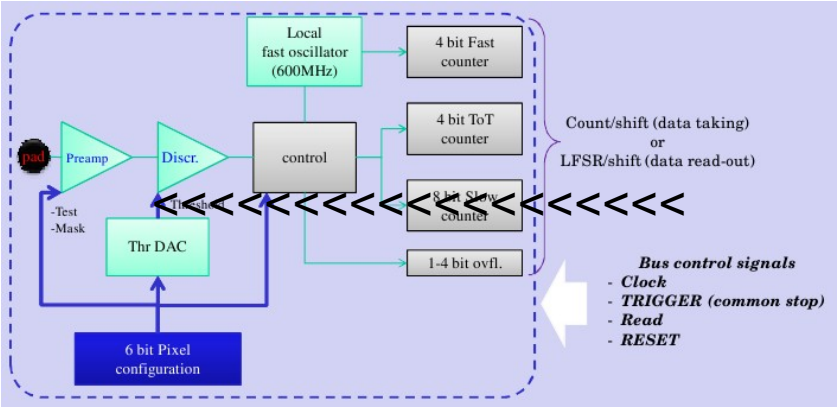
GOSSIPO-3

Test chip to evaluate:

- a preamp-shaper-discriminator circuitry
- the performance of a low-power TDC-per-pixel circuit with a resolution sub 1 ns.
- an on-chip temperature sensor is being designed.

Specifications

Front-end: - input parasitic capacitance < 10 fF
- input noise 70 e-
- threshold 350 e-
- fast response 10ns (rise-time)



drift time measurements: - event clock 40MHz
- accuracy (bin size) 1.8ns (4-bit @ 25ns)
- range 6.4 s (8-bit @ 25ns)

ToT measurements: - accuracy 25ns
- range 400ns (4-bit @ 25ns)

power consumption: goal 100mW/cm2 (3 W/pixel)

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