# New service board

## THE LHCB MUON I2C LONG-LINE PROTOCOL USING GBT-SCA AND IGLOO2
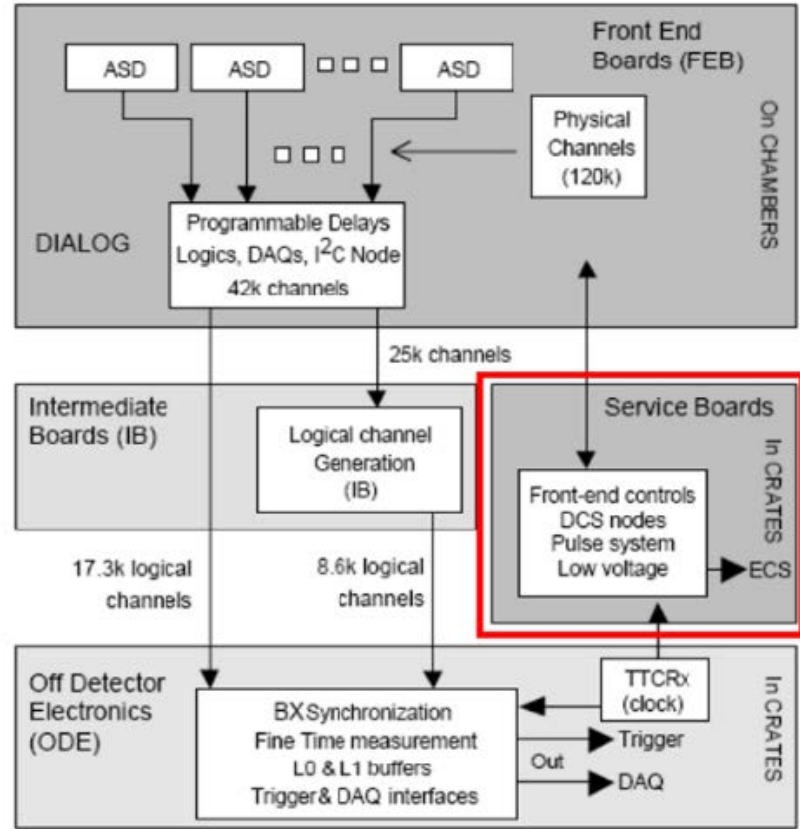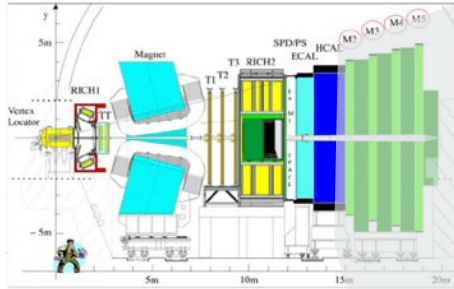
LHCb Upgrade Electronics

P. Fresch, V. Bocci

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# Introduction to the muon ECS



- 1000 chambers
- 100'000 physical channel
- 7000 Front-End boards

The front-end boards have control registers that can be set for tuning and monitoring purposes. A Service Boards System is in charge of proving to the ECS the access of these configuration map.

*V. Bocci* - Architecture of the LHCb muon Frontend control system upgrade

# The Front-End boards control link



- The tuning and debugging operations are carried out by the DIALOG chip
- 93 memory-mapped registers are used to set the operation mode of this chip
- The registers are accessed following the protocol of standard I2C RAM device (e.g. writing frame below)

| S | Slave Address | 0 | A | Word Address | A | DATA | A | P |
|---|---------------|---|---|--------------|---|------|---|---|
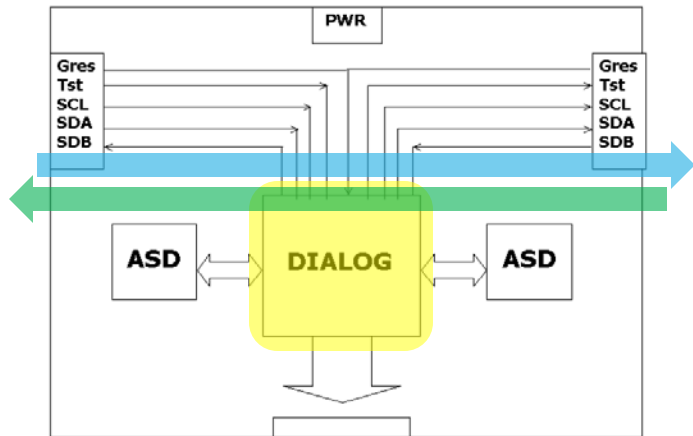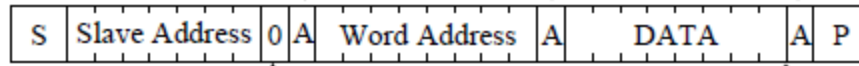


- The Front-End boards are positioned at >10m away from the Service Boards system crates, a standard I2C bus is not the best solution
- To overcome signal degradation commercial I2C bus-extender were available but not possible to use in a radiation environment
- On other hands LVDS rad-tolerant chips and IP were present
- It has been chose to split the bidirectional Serial Data wire in two LVDS-based unidirectional lanes

*V. Bocci, G. Chiodi, F. Iacoangeli, F. Messi, and R. A. Nobrega - The Muon Front-End Control Electronics of the LHCb Experiment*
*S. Cadeddu, V. De Leo, C. Deplano and A. Lai - Dialog 1.0 Datasheet*

# The Front-End boards control link
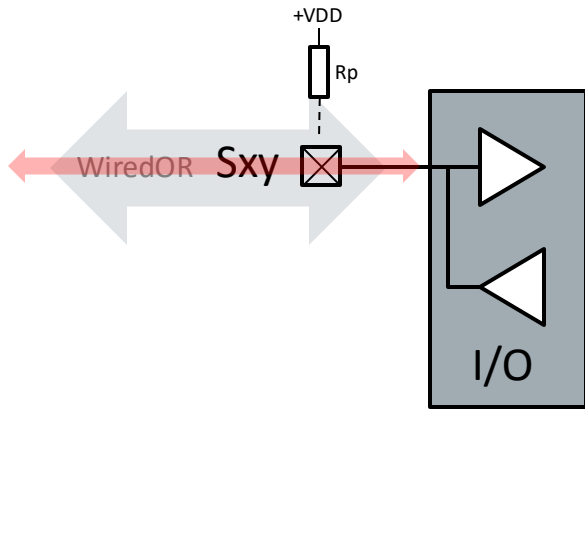


The standard I2C requires the bus wires to be in a wired-or configuration. Thus an interface write and read on the same wire and all the slaves share and senses the same physical wire.

Splitting the single wire (Sxy) on two different lanes (Txy and Rxy) allowed the use of the LVDS standard. It requires an end-to-end connection (avoiding Multipoint LVDS). The serial clock line requires one lane only because is a single master configuration
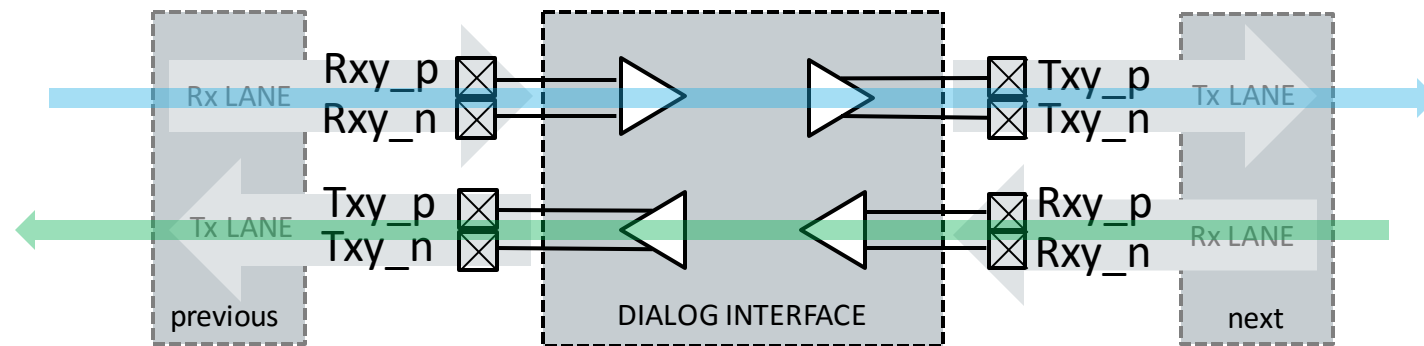
Thus the slaves are connected in a daisy chain fashion and do not share and sense the same physical lane. This requires a particular management (at the moment carried out by a dedicated uP-based rad-tol board)

# The GBT link implementation in the ECS upgrade

The GBT link project provide 16 I2C master in the Slow Control Chip whose aim is exactly providing an interface between the custom Front-End of the experiments and the custom GigaBit Transmission link for monitoring and debug purposes.
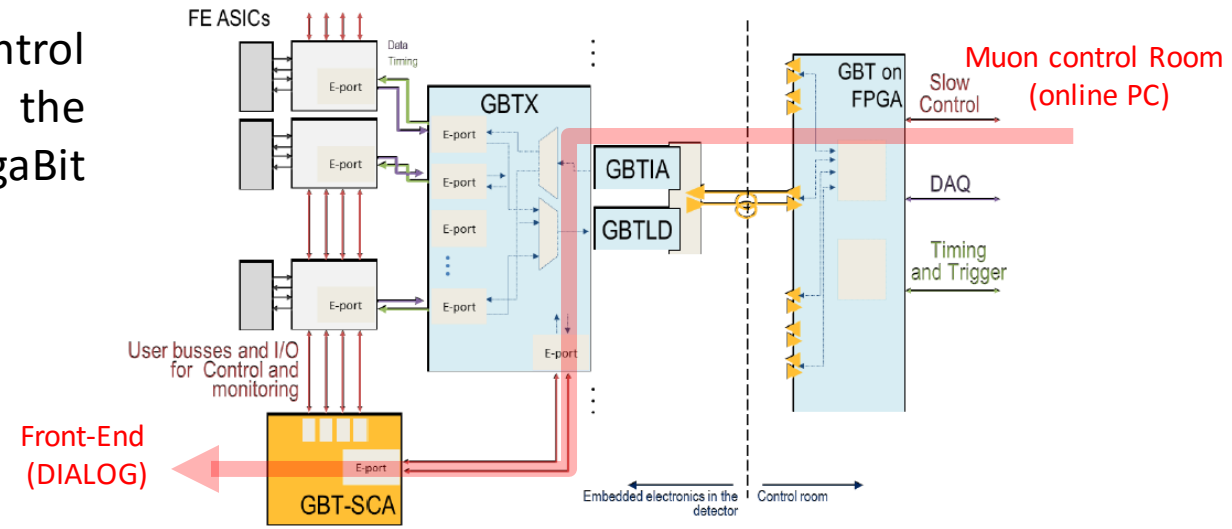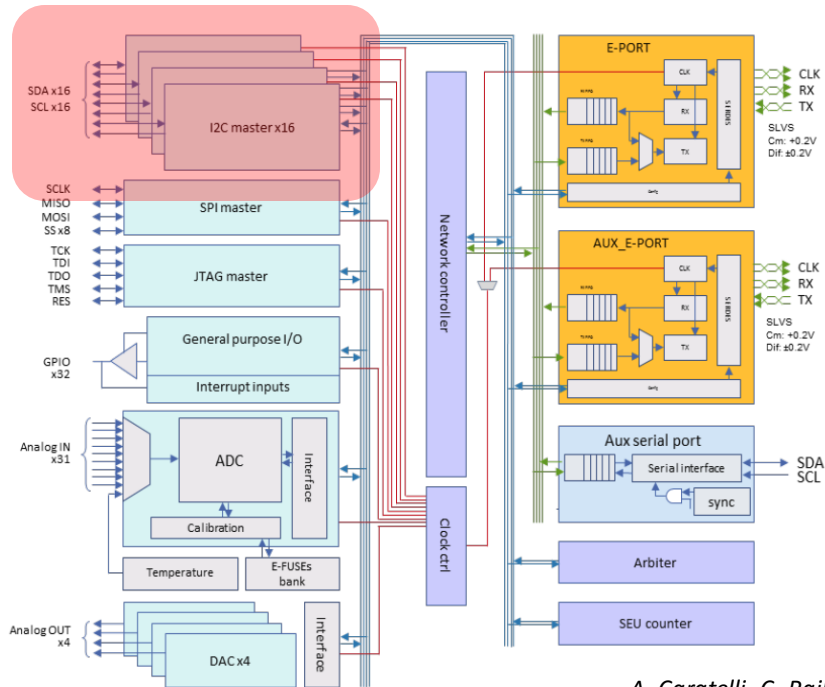




At logical level, the LVDS-based link is exactly equal to the I2C. A standard I2C master might be able to drive the bus. **The idea is to provide to the GBT-SCA I2C interface the possibility to communicate on the custom bus and provide the access to the DIALOG chip on Front-End boards by the means of the GBT link.**

*A. Caratelli, C. Paillard, K. Kloukinas, S. Bonacini, A. Marchioro, P. Moreira, R.De Oliveira* – The Slow Control Adapter for the GBT system USER MANUAL

# The I2C Protocol Converter

Considering this property of the bus, an FSM is required for a partial parsing of the messages on the I2C bus that acts on the hardware and permit the communication in both directions:
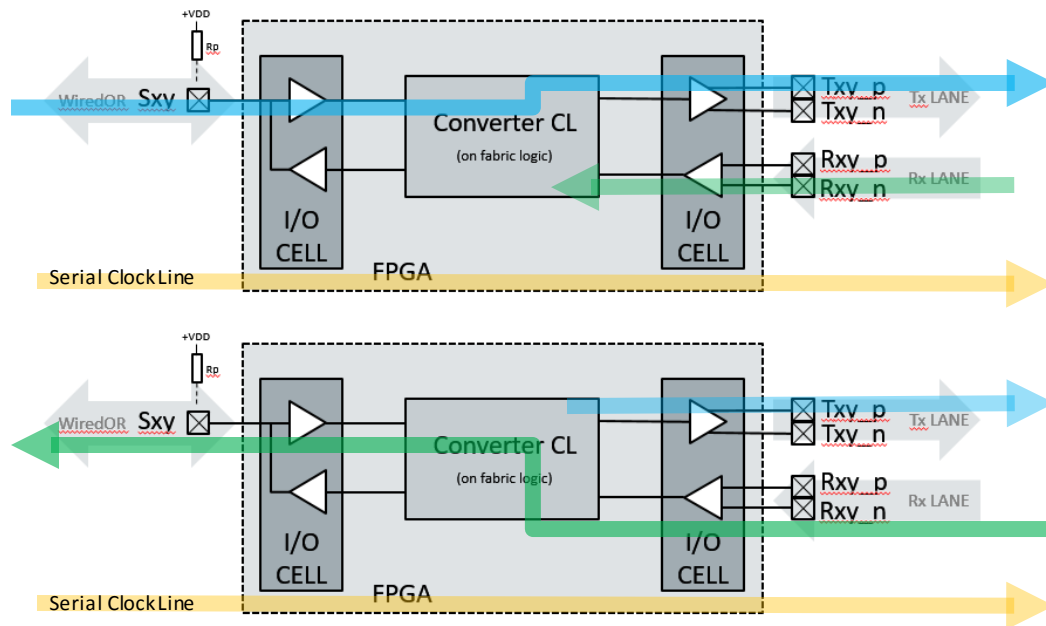


When the master has the control of the bus, the data flow is from the master to the slave(s) (from left to right in the picture above). After the 8th bit it release the bus and wait for the slave to acknowledge the transaction



When the slave as the control the data are flowing from the slave(s) to the master (from right to left in the picture above). After the 8th bit it release the bus and wait for the master to acknowledge the transaction

If the sense of the data flow is not correctly managed the communication fails. The Converter Combinatory Logic senses the actual frame and acts correspondingly. It is synchronized with the I2C Serial Clock Line that is then buffered on the dedicated LVDS lane to reach the slaves.

# The I2C Protocol Converter
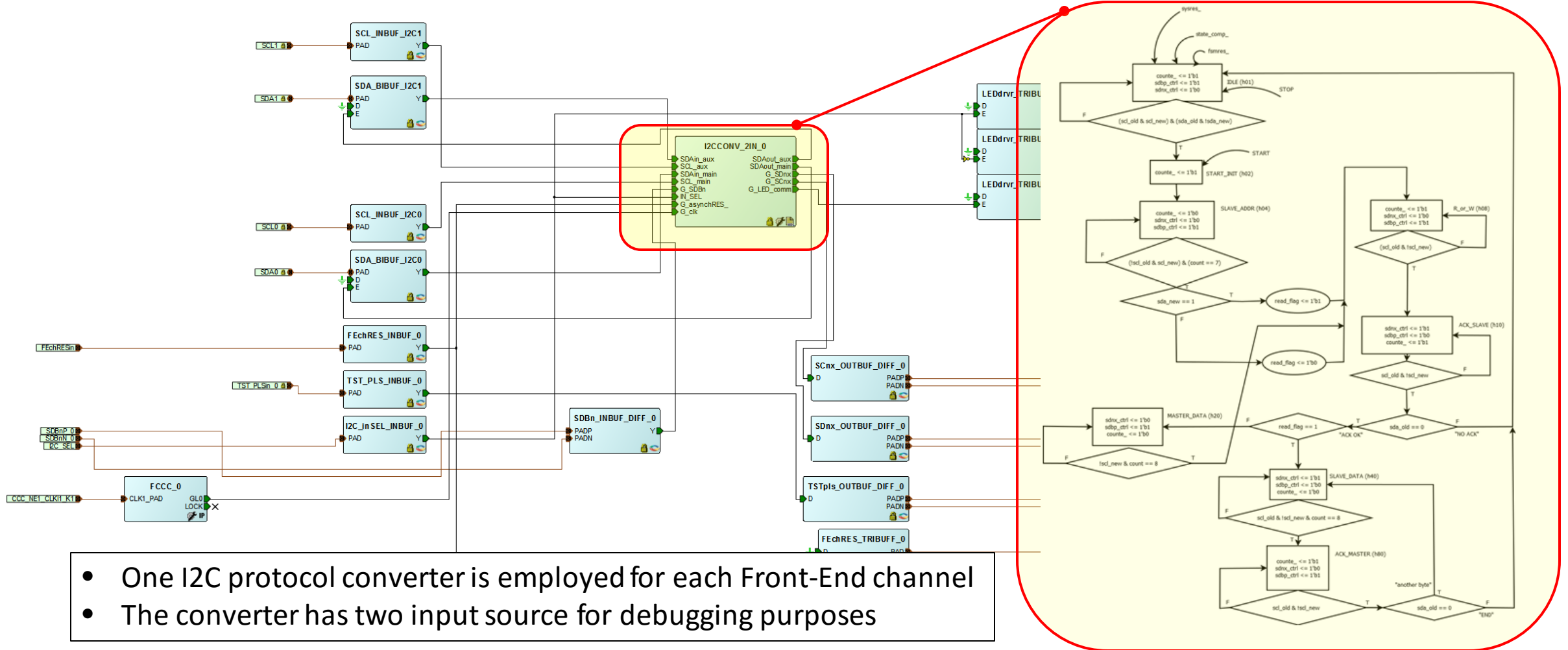


- One I2C protocol converter is employed for each Front-End channel
- The converter has two input source for debugging purposes

# The I2C Protocol Converter
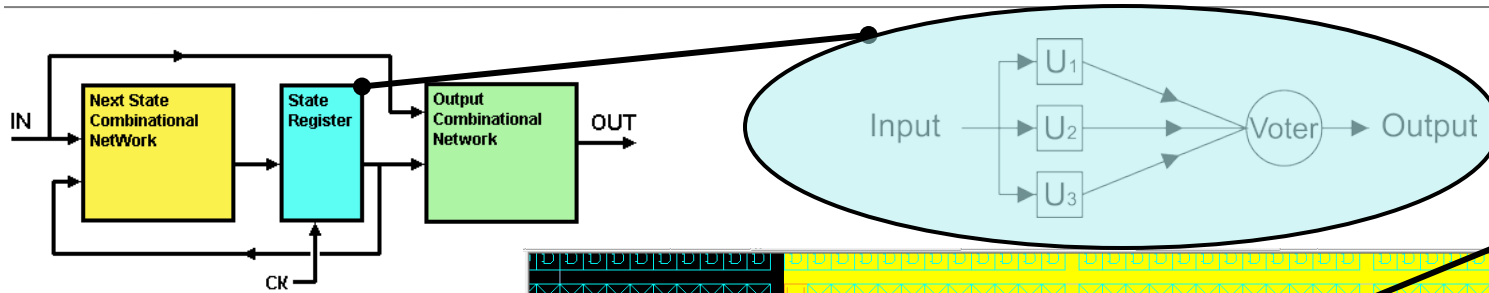


- The FSM has a Mealy architecture
- The state register (and all te other register of the FSM) are TMR protected
- The TMR is implemented by a synthesis directive
- The total usage is <140 cells (4 input LUT + 1 FF)
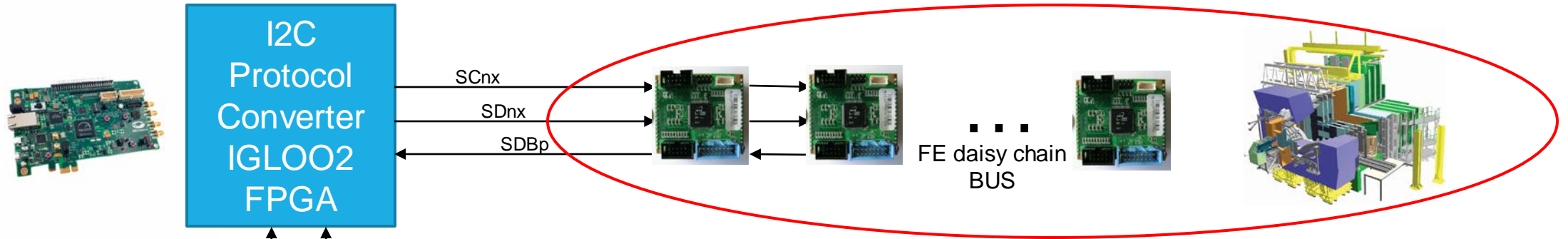- We expect to fit all the 12 FSM required in 10% of the chip
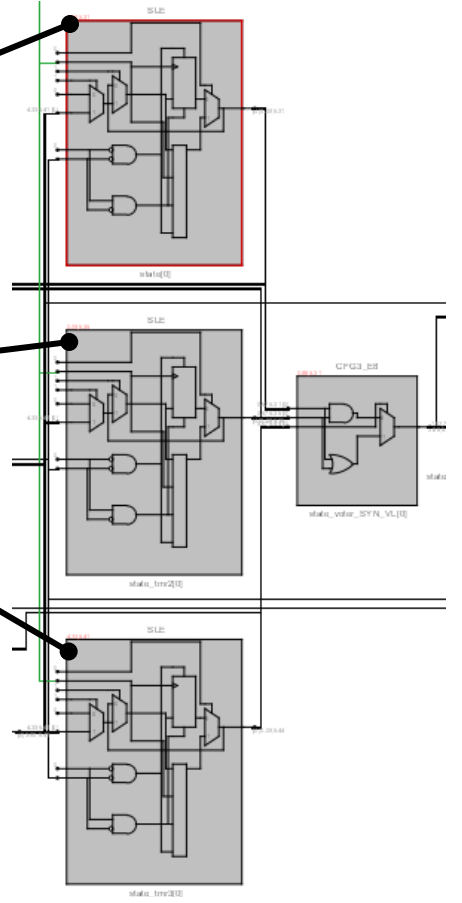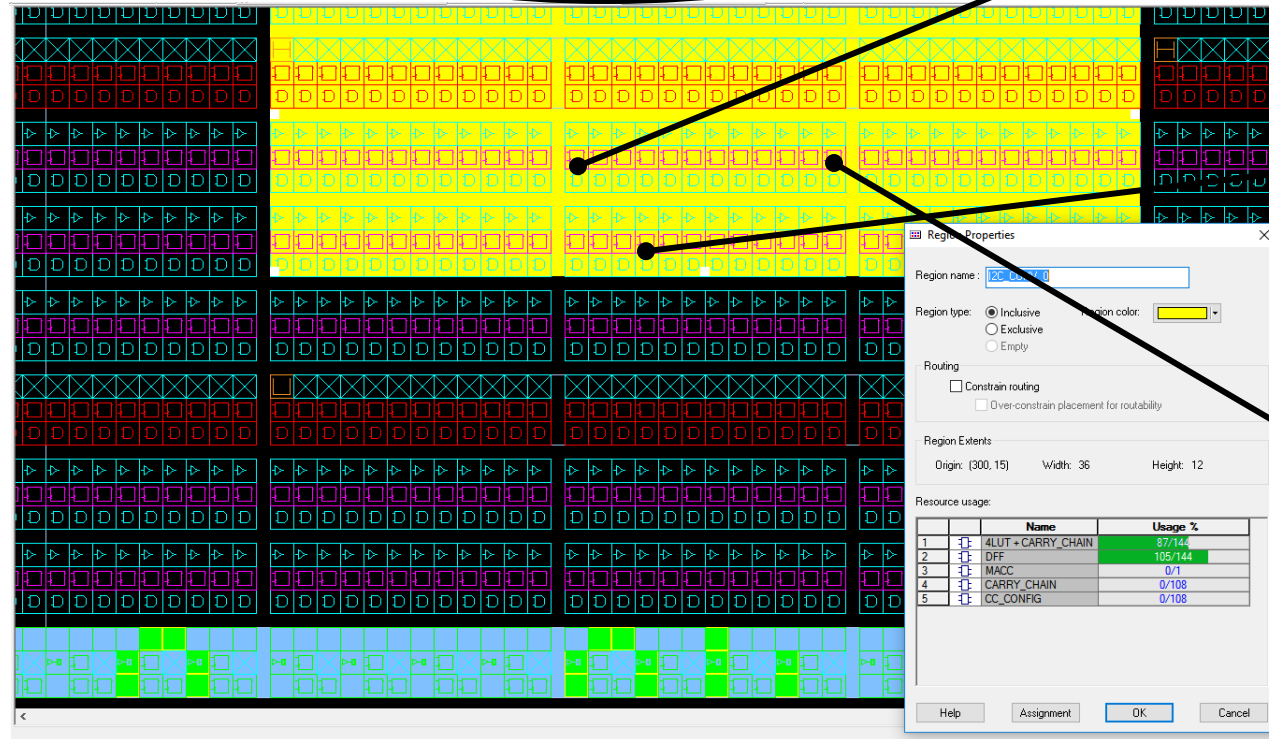
```
module CORE_I2CCONV_TMR( SDA, SDnx, SDBn, SCL, SCnx, LED_comm, asynchRES_, clk) /* synthesis syn_safe_case =1 */   /* synthesis syn_radhardlevel = "tmr" */;
```
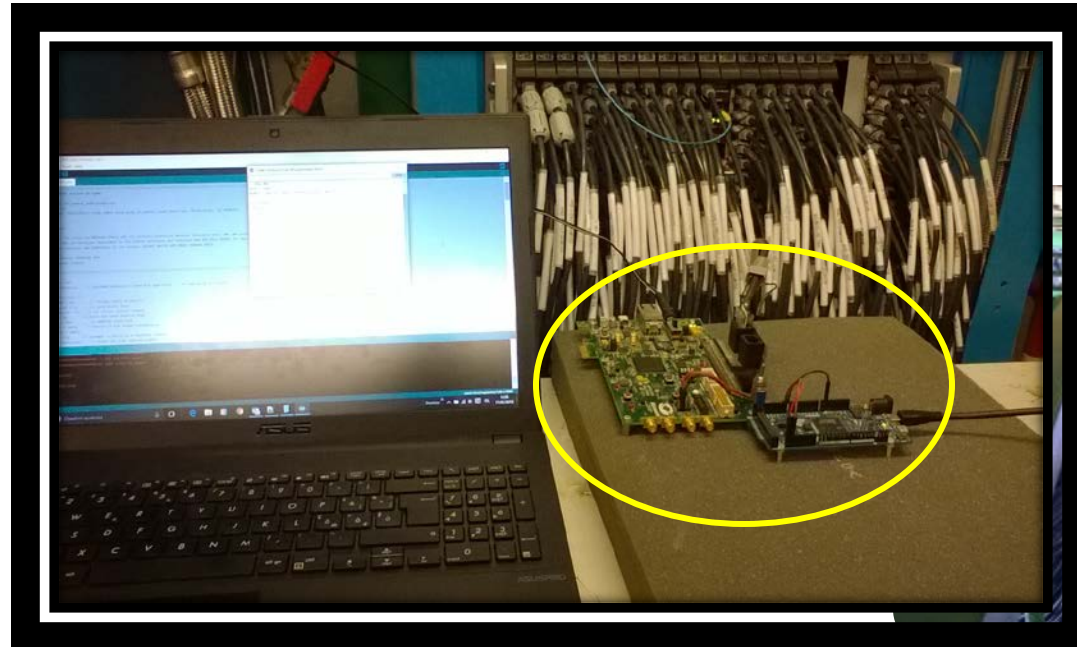
# Microsemi® IGLOO2® HW description and features
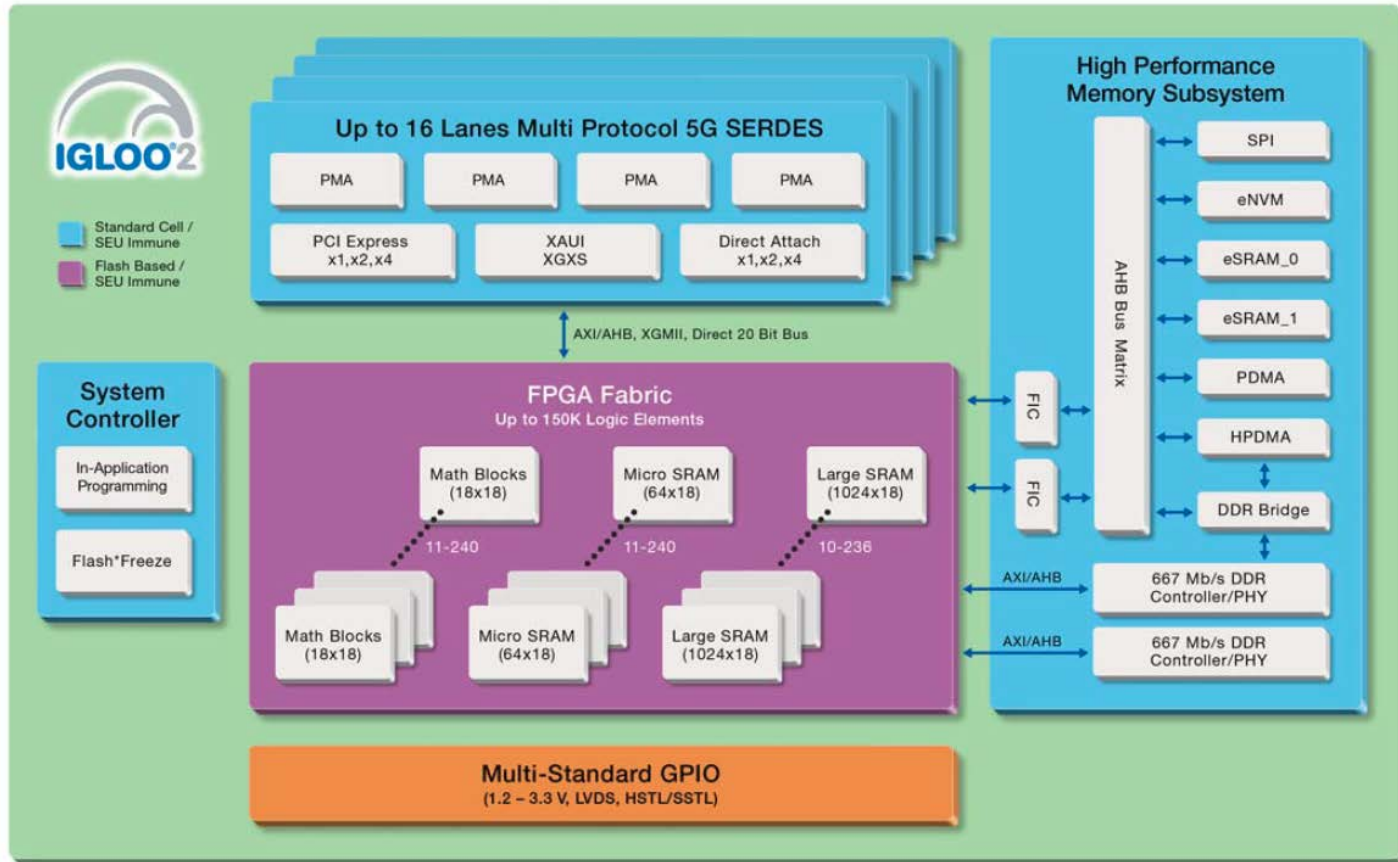


- 4 input Look-Up Table (LUT) Single Event Upset (SEU) Immune implemented with Zero FIT FPGA Configuration Cells
- High Performance Memory Subsystem on AHB with SECDEC enable/disable feature to protect eSRAM and eNVM data
- Multi-Standard GPIO with native LVDS
- The FSM registers are protected by Triple Mode Redundancy automatically implemented using Symplify compiling directives
- Versatile and reliable platform for further logic development

*Microsemi® - IGLOO2 FPGAs Product Brief*

# Test on the LHCb muon detector



I2C Protocol Converter IGLOO2 FPGA

SCnx
SDnx
SDBp

FE daisy chain BUS

SCL | SDA

Standard I2C Master Arduino Due

IT IS WORKING!!

# Test on the LHCb muon detector

```
I2C Scanner
Scanning...
I2C device found at address 0x30  <- OK
I2C device found at address 0x31  <- OK
I2C device found at address 0x32  <- OK
I2C device found at address 0x33  <- OK
I2C device found at address 0x34  <- OK
I2C device found at address 0x35  <- OK
done


Move the switch to start the test!

Communication with slave @ address:  30
started @(us):  2747538

ended @(us):  53354617
# of W&R attempts: 100000000    NACK_couter: 0 0    Comm_err counter: 0


Communication with slave @ address:  31
started @(us):  53385947

ended @(us):  103182974
# of W&R attempts: 100000000    NACK_couter: 0 0    Comm_err counter: 0


Communication with slave @ address:  32
started @(us):  103215371

ended @(us):  153003654
# of W&R attempts: 100000000    NACK_couter: 0 0    Comm_err counter: 0


Communication with slave @ address:  33
started @(us):  153036059

ended @(us):  203005555
# of W&R attempts: 100000000    NACK_couter: 0 0    Comm_err counter: 0
```

- Communication test have been done on a bus of FE connected through a 26m-long cable (the longest, worst condition)

- The same register has been written and read at full speed (1 Mbps) for 100'000'000 times. Two known sample byte have been used alternatively and checked at each iteration, looking for errors on communication/elaboration on each FE (DIALOG chip) belonging to the bus (6 devices)

- In the end a total amount of about 1,2GB of data have been exchanged (>13 hours) without any error (do not refer to the @(us) time stamp!). To completely reconfigure and check the entire system less than 2.5 MB are required

# Test on the LHCb muon detector

- The SCA I2C transmission buffer max size is 16 Byte:



[*] "**GBT-SCA**: THE SLOW CONTROL ADAPTER ASIC FOR THE GBT SYSTEM - User Manual" v.7

- A maximum of 16 byte can be exchanged in a single write or read I2C frame

- Let's test if the DIALOG can do that:



- All the DIALOG on the I2C LVDS bus were tested with success. All the possible frame size have been used. Data varied from 0x41 to 0x50 (ASCII "A"to"P")

# Quick check test with the MiniDAQ
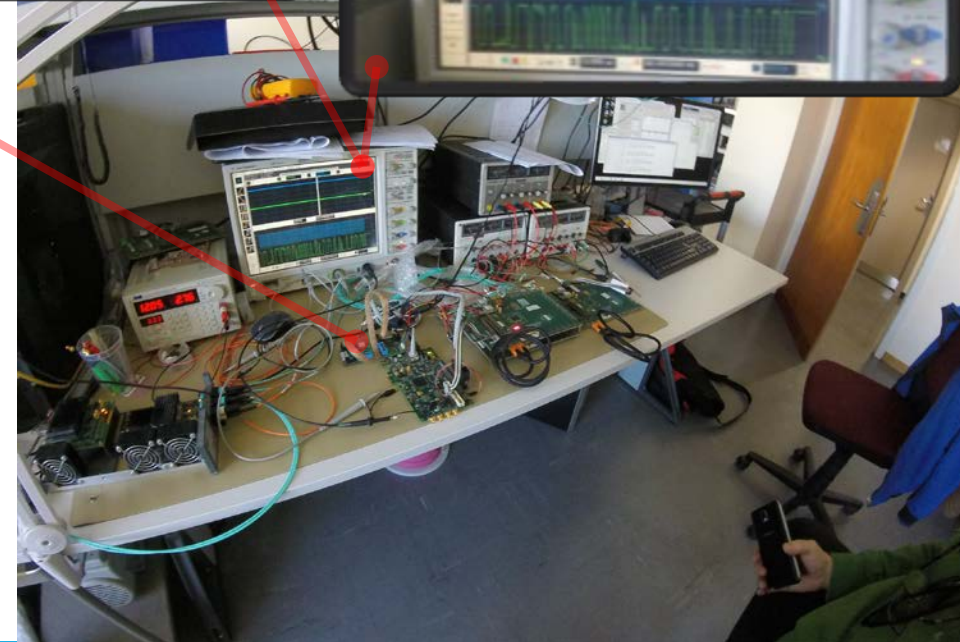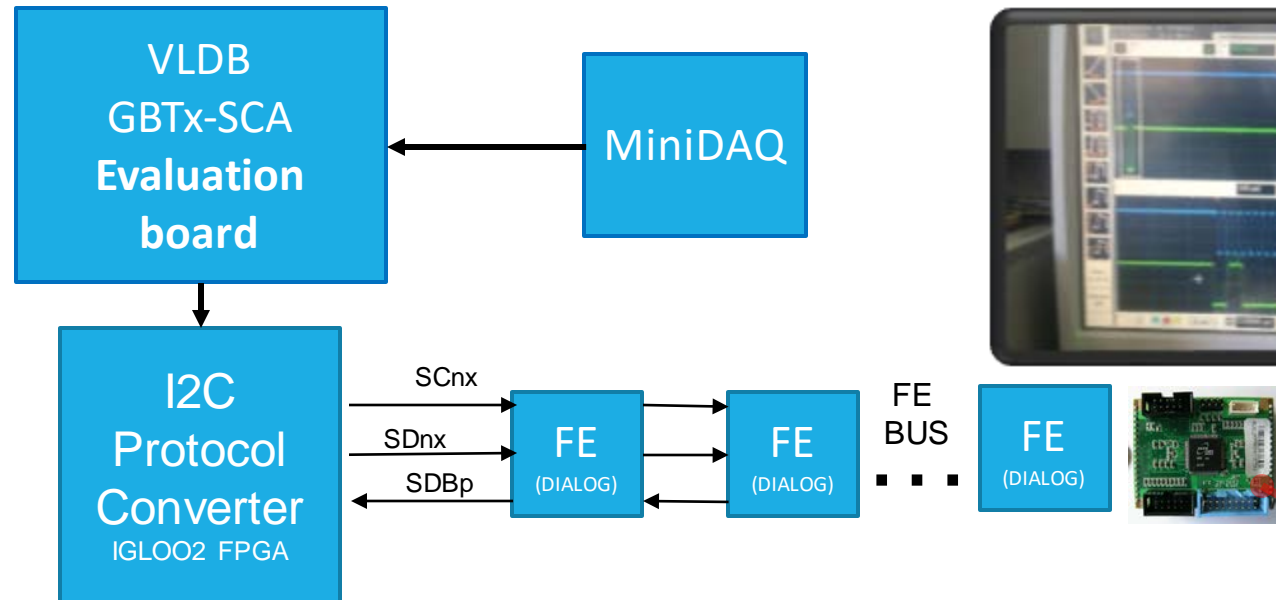


- The logic showed to work correctly since the first test but because of analogic signal misalignments due to a different power source module used on the CERN VLDB we initially had poor performances in terms of BER
- Fixing the issue with a small modification of the IGLOO2 Evaluation Kit we solve the problem and the test bench started working correctly

# Final version of the nSB prototypes



TOP

| In1 | GND1 | Alim |
| In2 | Bottom | GND2 |
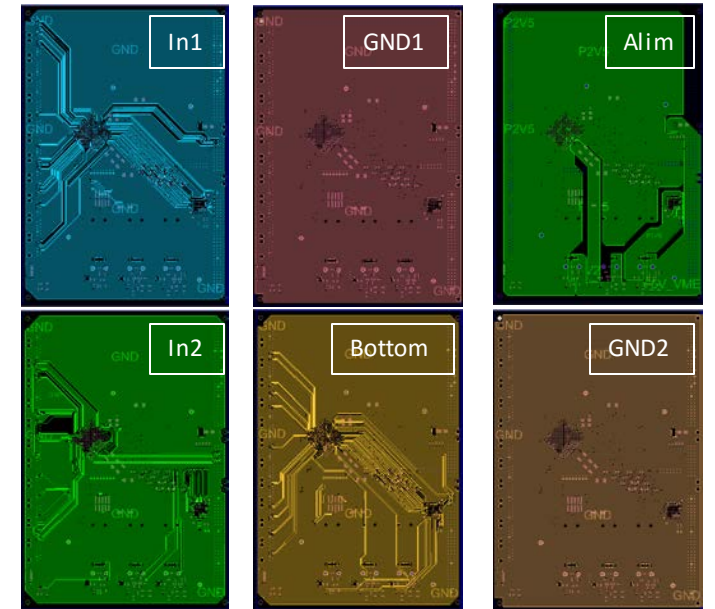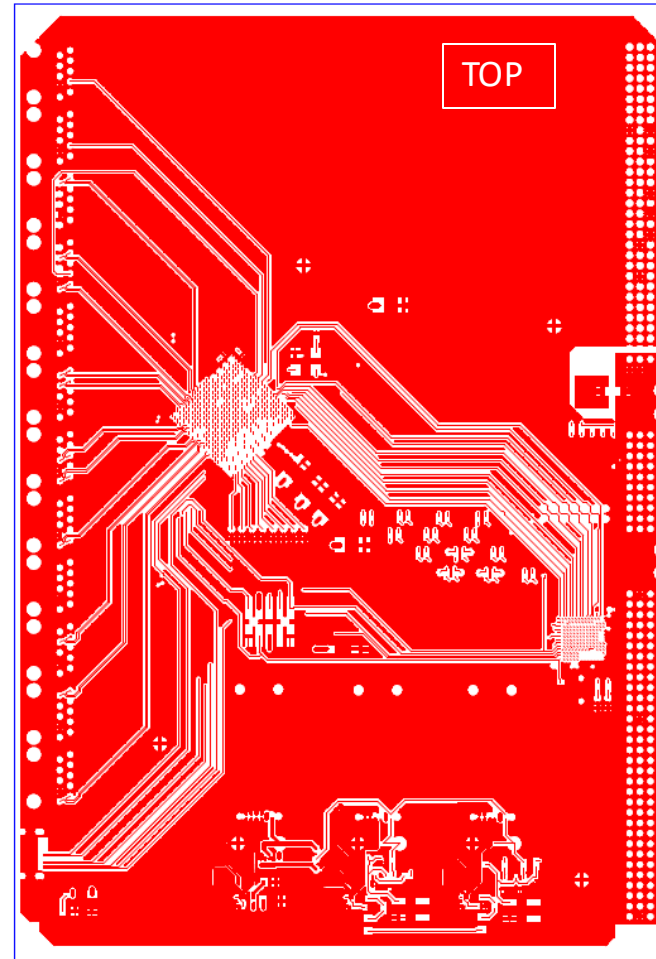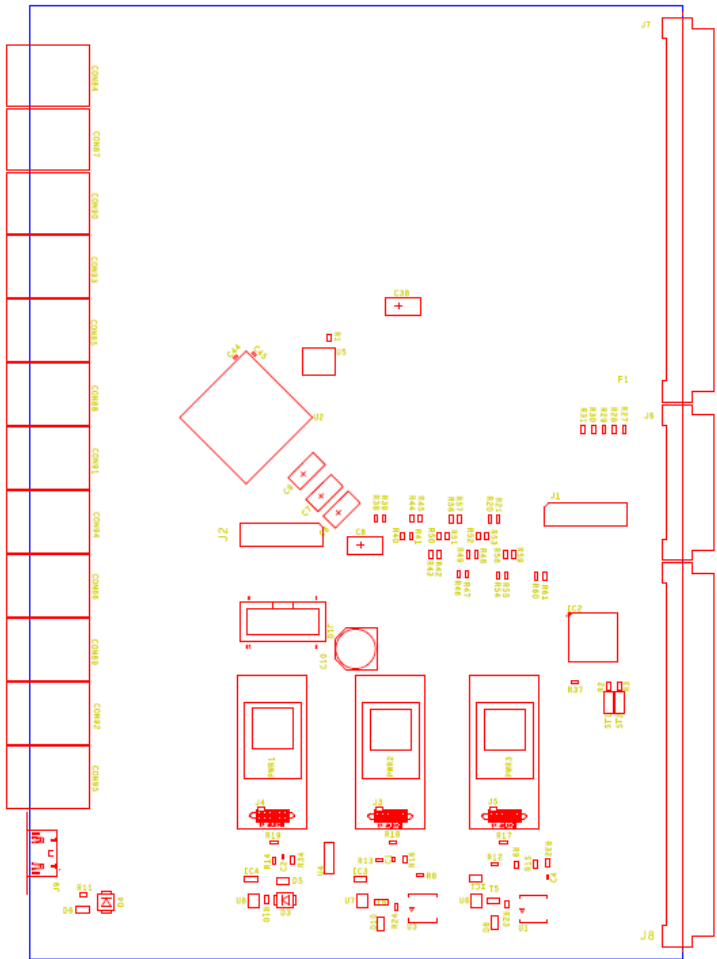
- We are waiting for the production of the prototypes of the nSB
- The manufacturing request order has been submitted

Credit to: Giacomo Chiodi

# Conclusions

- The protocol converter combined with the LVDS-based I2C bus forms a long-line link that can be driven by the GBT-SCA chip, suitable for environment with presence of radiations

- Each configuration/debug register is seen by the GBT system as a standard I2C RAM memory register

- Moreover the link developed for this special application can be extended to any application where a long-line I2C link is needed

- The logic of the converter showed to be robust during the first test session on the apparatus but more test will be done (probably directly on the nSB prototypes)

# Thank you

FOR YOUR ATTENTION!