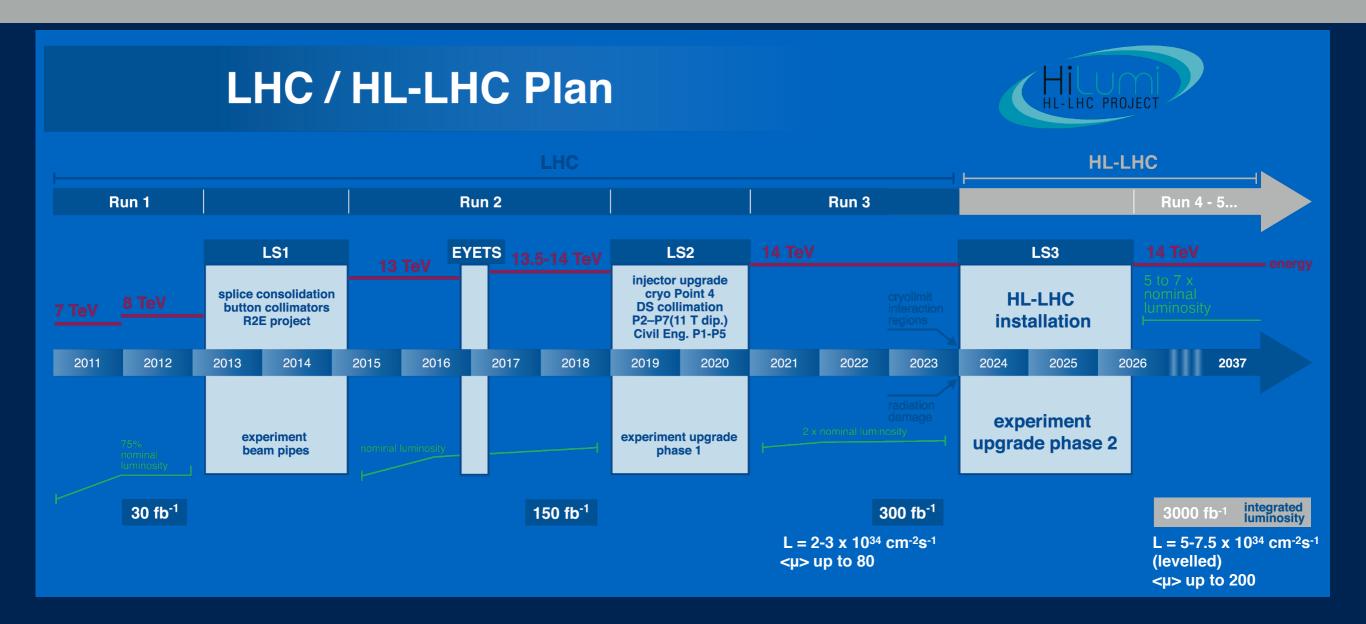
ATLAS UPGRADE

THE FIFTH ANNUAL LARGE HADRON COLLIDER PHYSICS CONFERENCE 20 May 2017

RICCARDO VARI - INFN ROMA
ON BEHALF OF THE ATLAS COLLABORATION

ATLAS AND LHC UPGRADES



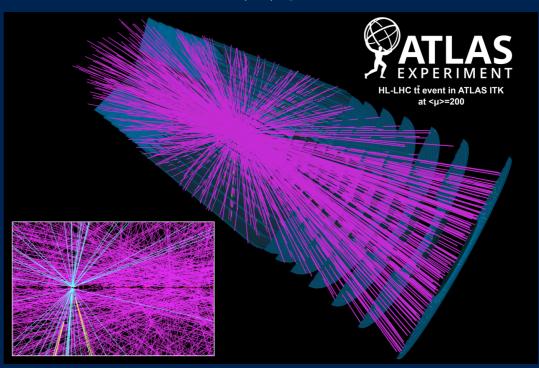
+ ATLAS UPGRADES:

- Long Shutdown 1 (LS1): RPC in barrel feet region, MDT at $|\eta| \sim (1.1-1.3)$, pixel IBL, HLT
- Long Shutdown 2 (LS2): New Small Wheel, Muon, LAR electronics, L1 Calo, FTK, TDAQ
- Long Shutdown 3 (LS3): Many New Systems, R&D activities and TDR preparation ongoing

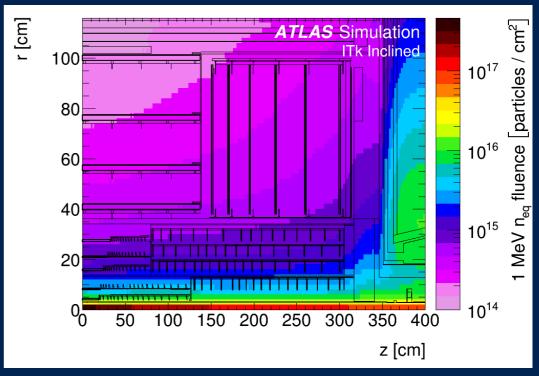
HIGH LUMINOSITY IMPACT ON THE EXPERIMENT

- + HIGH LUMINOSITY IS NEEDED TO ACHIEVE PHYSICS GOALS
- + ALL PARTS OF THE EXPERIMENT HAVE TO STAND A PEAK LEVELLED LUMINOSITY OF 7.5x10³⁴ cm⁻² -1
- + DETECTOR CHALLENGES:
 - HIGH PILEUP ($<\mu>$ UP TO ~200 COLLISIONS/CROSSING)
 - HIGH RADIATION LEVELS (~10 NEQ/CM; 10 MGY)
- + REQUIREMENTS:
 - KEEP GOOD PHYSICS PERFORMANCES IN THIS CHALLENGING ENVIRONMENT, AT LEAST AS GOOD AS IN RUN 2 AND 3
 - KEEP ACCEPTABLE TRIGGER RATE WITH LOW P_T THRESHOLD
 - $^{ ext{-}}$ MITIGATE PILE-UP UP TO HIGH η

PILEUP

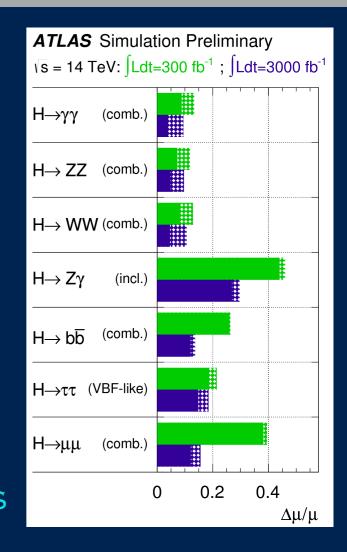


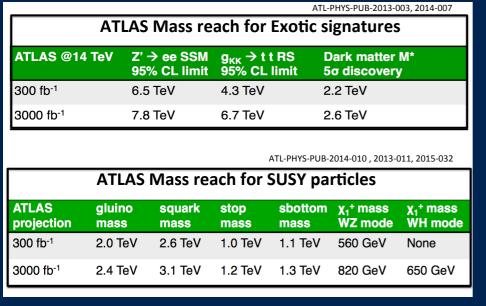
RADIATION LEVELS

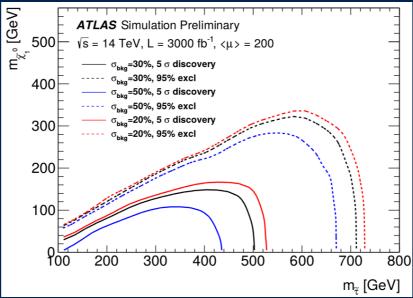


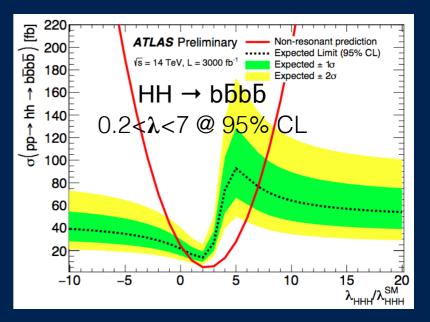
MOTIVATION FOR THE UPGRADES

- * MAXIMISE PHYSICS PERFORMANCE FOR:
 - PRECISION MEASUREMENTS OF HIGGS
 COUPLING AND OTHER SM PROCESSES
 - SEARCH OF SM RARE EFFECTS (LIKE H-> $\mu\mu$), IN PARTICULAR SELF-COUPLING HIGGS FROM DOUBLE HIGGS EVENTS
 - CONTINUE THE LHC SCIENTIFIC PROGRAMME
 WITH THE RESEARCH OF NEW PHYSICS SIGNALS

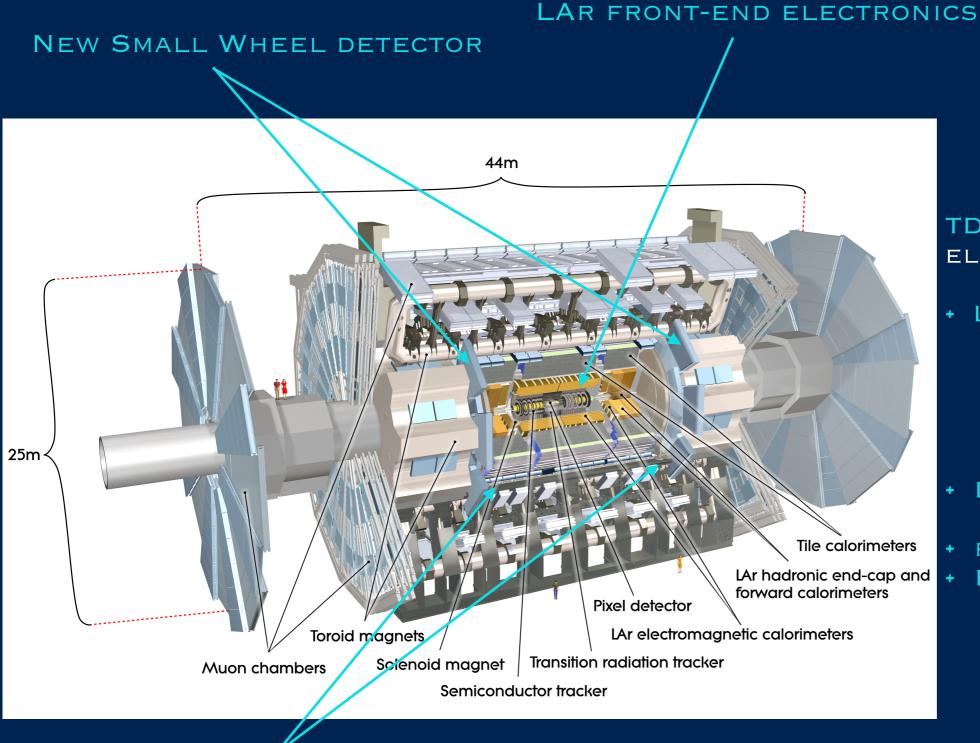








ATLAS PHASE-I UPGRADES



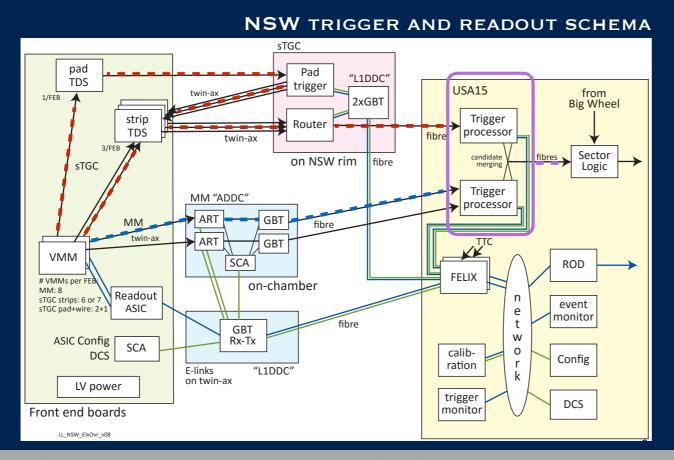
TDAQ OFF-DETECTOR ELECTRONICS:

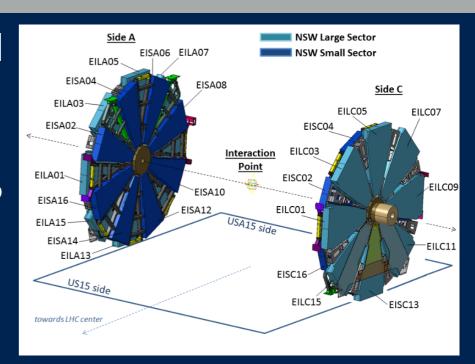
- + L1 HARDWARE TRIGGER:
 - L1 CALORIMETER
 - L1 TOPOLOGICAL
 - L1 NSW TRIGGER
 - L1 ENDCAP TRIGGER
 - L1 MUCTPI
- + L1.5 HARDWARE TRIGGER:
 - FAST TRACK TRIGGER
- * READOUT SYSTEM
- · HLT

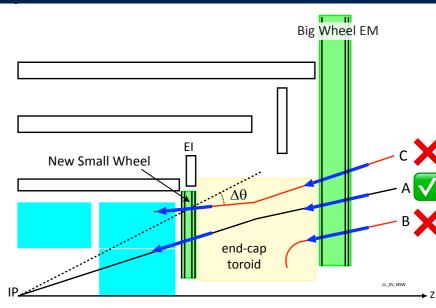
NEW MUON RPC DETECTOR (BIS78)

NEW SMALL WHEEL

- * TWO 5M RADIUS WHEELS IN THE INNER END-CAP REGION (1.3 < $|\eta|$ < 2.7)
- + EACH WHEEL IS FORMED BY:
 - 2 EXTERNAL STGC QUADRUPLETS (MAINLY TRIGGER, BUNCH ID IDENTIFICATION + VECTOR TRACKING WITH < 1 MRAD RESOLUTION)
 - 2 INTERNAL MICROMEGA QUADRUPLETS (MAINLY TRACKING, SPATIAL RESOLUTION < 100 μ M)
- * NEEDED TO REDUCE FAKE MUON TRIGGERS IN THE END-CAP REGION, THANKS TO THE COINCIDENCE ENDCAP-NSW





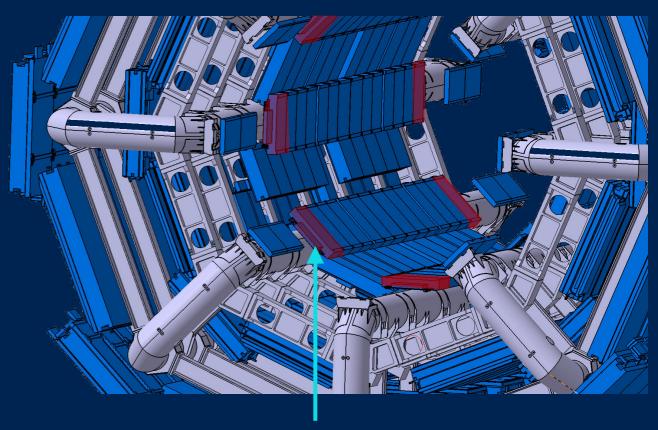


ATLAS-TDR-020-2013 EXPECTED L1 MUON RATE FOR L = 3×10^{34} cm⁻²s⁻¹

L1MU threshold (GeV)	Level-1 rate (kHz)
$p_{\mathrm{T}} > 20$	60 ± 11
$p_{\rm T} > 40$	29 ± 5
$p_{\rm T} > 20$ barrel only	7 ± 1
$p_{\rm T} > 20$ with NSW	22 ± 3
$p_{\rm T} > 20$ with NSW and EIL4	17 ± 2

BIS78

- + NSW covers the region (1.3 < $|\eta| <$ 2.7), while the Big wheel covers (1.0 < $|\eta| <$ 2.7)
- * HALF OF THE REGION 1.0 < |\eta| < 1.3 IS COVERED BY THE EXISTING EIL4 TGC END-CAP TRIGGER DETECTORS
- * NEW DETECTORS IN THE BARREL BIS REGION COVER THE OTHER HALF
- * 16 RPC TRIGGER CHAMBERS + REPLACEMENT OF 16 EXISTING MDT WITH SMDT
- + THE ADDITIONAL RPC CHAMBERS
 CAN SIGNIFICANTLY REDUCE THE
 FORESEEN FAKE RATE



BARREL INNER SMALL REGION BIS78 RPC+SMDT

* PHASE-II PILOT PROJECT:

SAME MDT AND RPC DETECTOR

TECHNOLOGY THAT WILL BE

USED FOR PHASE-II, WHEN THE

FULL BI LAYER WILL BE

EQUIPPED

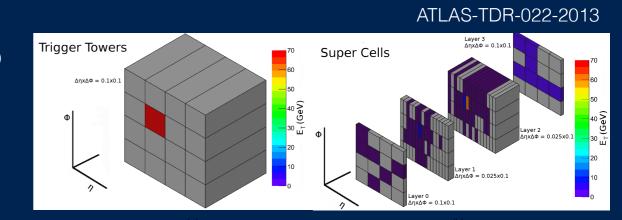
LAR CALORIMETER AND L1CALO NEW ELECTRONICS

+ LAR CALORIMETER:

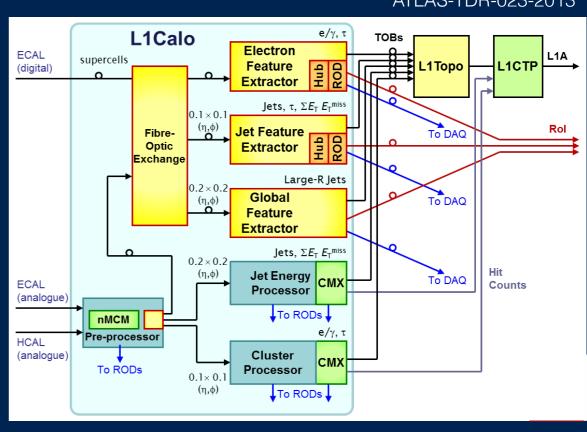
- + NEW FRONT-END (TRIGGER DIGITISER BOARD LTDB)
 AND BACK-END (DIGITAL PROCESSING SYSTEM LDPB)
 BOARDS
- * INCREASED TRIGGER TOWER GRANULARITY ($\Delta \eta x \Delta \phi = 0.025x0.1$)
- * GOOD TRIGGER PERFORMANCES WITH THE INCREASING LUMINOSITY AND PILE-UP:
 - + LOW TRIGGER RATE THANKS TO THE BACKGROUND REJECTION
 - + LOW THRESHOLDS AND BETTER TURN-ON CURVES
 THANKS TO THE HIGHER GEOMETRICAL RESOLUTION

+ L1CALO:

- NEW FEATURE EXTRACTOR BOARDS: EFEX, GFEX, JFEX
- MORE REFINED PROCESSING OF ELECTROMAGNETIC
 CALORIMETER INFORMATION AT HIGHER GRANULARITY
- BETTER DISCRIMINATION BETWEEN PHOTONS, ELECTRONS, TAUS AND JETS
- EFFICIENT SINGLE OBJECT TRIGGERS FOR ELECTROWEAK-SCALE PHYSICS

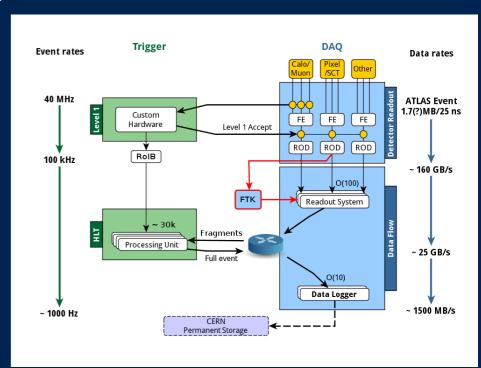


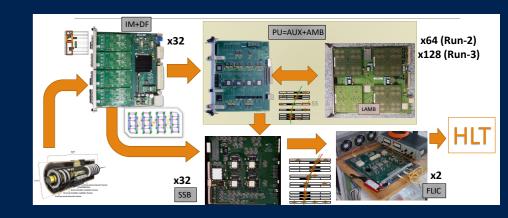
ATLAS-TDR-023-2013



FAST TRACKER (FTK)

- * PERFORMS REAL-TIME TRACKING FOR ALL EVENTS ACCEPTED BY THE LEVEL-1 TRIGGER (NO ROI), SUPPORTING HLT DECISION
- * EFFICIENCY > 90% FOR P_T>1GEV, $|\eta|$ <2.5, RATE UP TO 100 KHz, LATENCY < 100 μ s
- + Provides tracking information to Level-2 in ~25 μs
- + BASED ON PIPELINED CUSTOM HARDWARE:
 - FIRST STAGE (PATTERN RECOGNITION) + SECOND STAGE (TRACK FITTING)
 - 8192 ASSOCIATIVE MEMORY CUSTOM CHIPS, >1000 FPGAS
- * ABOUT 50% OF THE COMPUTING POWER WILL BE INSTALLED BY JULY 2017, THEN 100% FOR PHASE-I





TDAQ PHASE-I

+ L1 CALO:

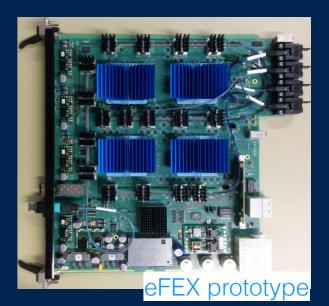
- NEW TRIGGER AND READOUT ELECTRONICS, NEW FIBRE OPTICS SYSTEM
- FINER GRANULARITY DATA, MORE EFFICIENT ALGORITHMS

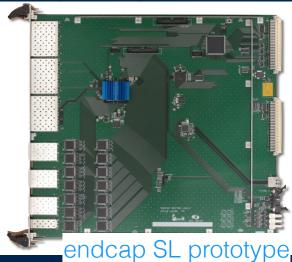
+ L1 TOPO:

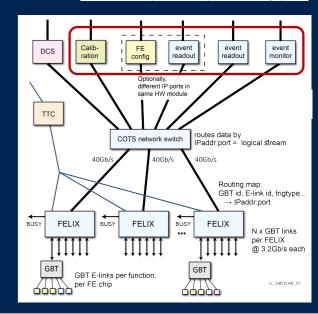
- NEW BOARD: TOPOLOGICAL ALGORITHMS, CALORIMETERS AND MUONS

+ L1 END-CAP:

- NEW MUON END-CAP SECTOR LOGIC BOARD WITH NEW INPUTS:
 - + NEW SMALL WHEEL MUON SYSTEM (TRIGGER PROCESSOR BOARDS)
 - + RPC NEW BIS78 TRIGGER BOARDS
 - + OUTER LAYER OF THE EXTENDED BARREL OF THE TILE CALORIMETER
 - + REDUCE THE FAKE TRIGGER RATE
- + L1 MUCTPI: NEW MUON TO CENTRAL TRIGGER PROCESSOR INTERFACE BOARD
- + FTK: NEW HARDWARE TRACK SYSTEM
- + HLT: OUTPUT RATE UP TO 1 KHZ
- + FELIX READOUT SYSTEM:
 - IT FUNCTIONS AS A ROUTER BETWEEN THE FE LINKS AND COMMERCIAL MULTI-GIGABIT NETWORK TECHNOLOGY, TRANSMITTING DATA TO THE APPROPRIATE DESTINATION NODE (READOUT, DCS, ...)
 - PREVIOUS HARDWARE RODS ARE REPLACED WITH SOFTWARE PROCESSES
 - IT INTERFACES WITH THE TTC AND BUSY SYSTEM
 - PHASE.-I: NSW, BIS78, L1CALO. IT WILL BE THE STANDARD SYSTEM FOR PHASE-II



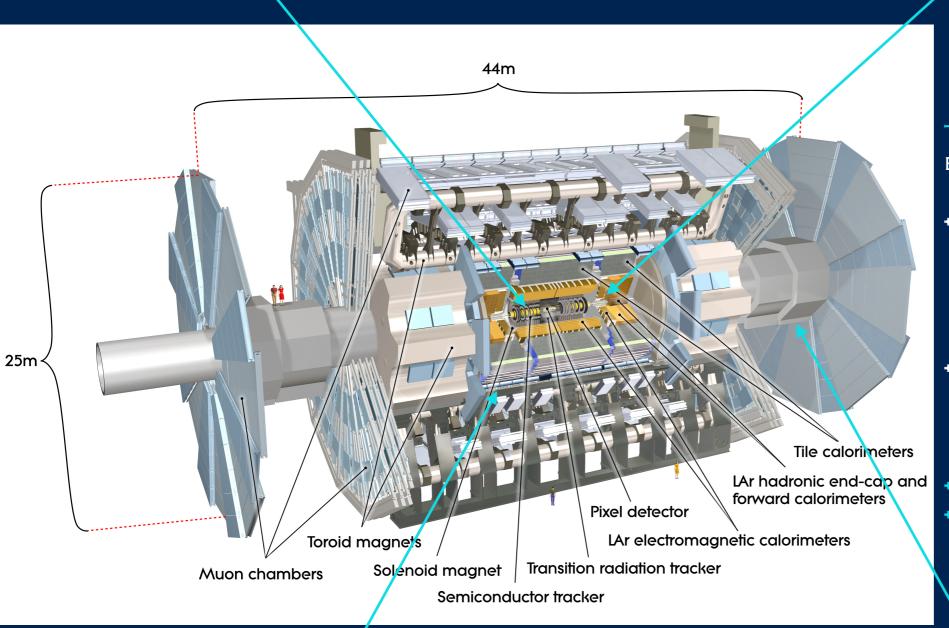




ATLAS UPGRADES FOR PHASE-II

NEW ALL-SILICON INNER TRACKER (ITK)
WITH ETA COVERAGE UP TO 4

HIGH GRANULARITY TIMING DETECTOR (HGTD)
IN FORWARD REGION (OPTION)



TDAQ OFF-DETECTOR ELECTRONICS:

- + LO HARDWARE TRIGGER:
 - + LO CALORIMETER
 - + LO TOPOLOGICAL
 - + LO MUON
 - + LO GLOBAL
- + L1 HARDWARE TRIGGER (OPTION):
 - + L1 GLOBAL
 - + L1 TRACK TRIGGER
- * READOUT SYSTEM
- + HLT

NEW MUON CHAMBERS IN THE INNER BARREL REGION

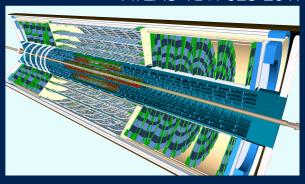
FORWARD MUON TAGGER (OPTION)

INNER TRACKER

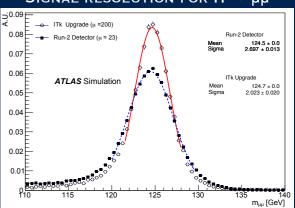
- + THE FIRST ATLAS PHASE-II TDR, COVERING THE OUTER PART OF THE TRACKER BASED ON SILICON STRIP DETECTOR, HAS BEEN SUBMITTED TO THE LHCC
- * NEW ALL-SILICON TRACKING SYSTEM
- * PIXEL DETECTOR AT SMALL RADIUS CLOSE TO THE BEAM LINE + LARGE AREA STRIP TRACKER SURROUNDING IT:
 - CENTRAL REGION: FIVE PIXEL LAYERS FOLLOWED BY TWO SHORT-STRIP LAYERS OF PAIRED STEREO MODULES, THEN TWO LONG-STRIP LAYERS OF PAIRED STEREO MODULES
 - FORWARD REGIONS: SIX STRIP DISKS AND A NUMBER OF PIXEL RINGS LEADING TO ONE OR MORE HITS DEPENDING ON THE RING LAYER AND η POSITION
- * EXTENSION UP TO $|\eta|=4$
- + NEARLY TEN TIMES MORE ELECTRONICS CHANNELS (60 MILLION)
- * EQUAL OR BETTER PERFORMANCES THAN THE EXISTING DETECTOR IN A MUCH MORE DIFFICULT TRACKING ENVIRONMENT
 - HIGH TRACK RECONSTRUCTION EFFICIENCY AND LOW RATE OF FAKE TRACKS
 - > 99% EFFICIENCY FOR MUONS WITH $P_T > 3 \text{ GeV}$; > 85% EFFICIENCY FOR PIONS AND ELECTRONS ABOVE 1 GEV, KEEPING FAKE RATES BELOW 1%



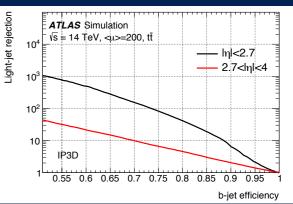
ATLAS-TDR-025-2017



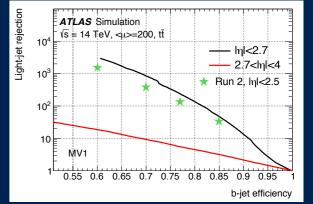
Signal resolution for $H \rightarrow JJJ$



PERF. OF THE IP3D B-TAGGING ALGORITHM



Perf. of the MV1 b-tagging algorithm



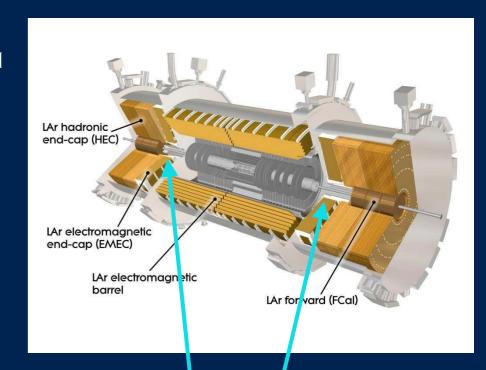
LIQUID ARGON CALORIMETER + HIGH-GRANULARITY TIMING DETECTOR (HGTD)

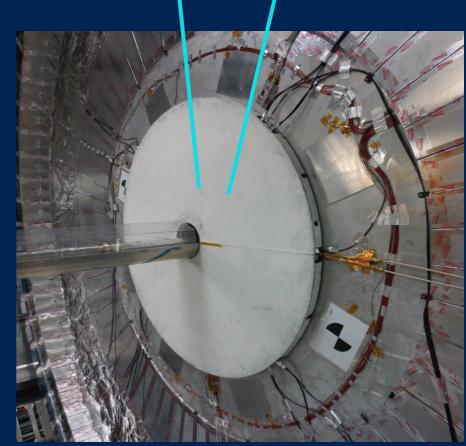
+ LAR:

- CURRENT ELECTRONICS IS NOT COMPATIBLE WITH PHASE-II REQUESTS (LATENCY AND TRIGGER RATE)
- RADIATION HARDNESS REQUIREMENTS ARE ABOVE ORIGINAL DESIGN (1 KGY AND 2.7 x 10¹³ NEQ/CM²)
- PHASE-I UPGRADED BOARDS WILL CONTINUE TO BE USED
- NEW FRONT-END AND BACK-END ELECTRONICS
- FULL GRANULARITY FE DIGITAL DATA SENT AT 40 MHz TO BACK-END

+ HGTD:

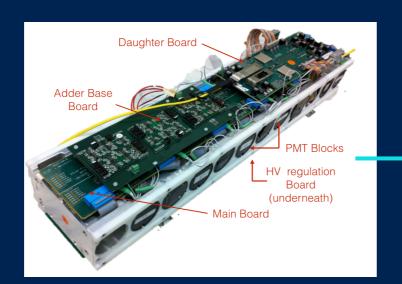
- MOTIVATION: PILE-UP MITIGATION, IMPROVE E/Y AND JET/E_T PERFORMANCE
- LOWER TRIGGER THRESHOLDS AND INCREASED PHYSICS ACCEPTANCE; VALIDATE ISOLATION FOR E/8
- SORT CHARGED TRACKS BY TIME TO REDUCE CONFUSION IN TRACKING AND PARTICLE FLOW
- $7 \cdot 2.4 < \eta < 4.2$; $R_{MIN} = 11 \text{ CM}$; $R_{MAX} = 65 \text{ CM}$; $\Delta Z \sim 6 \text{ CM}$; $\Delta T < 50 \text{ PS}$

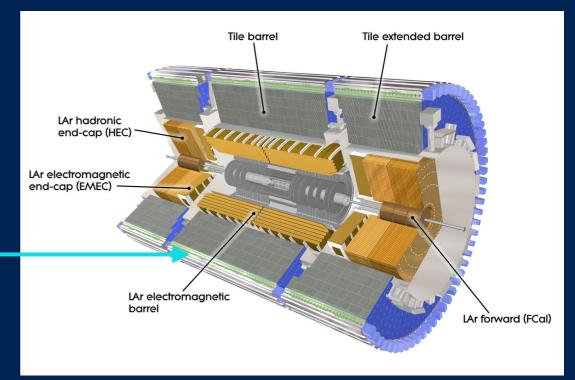




TILE CALORIMETER

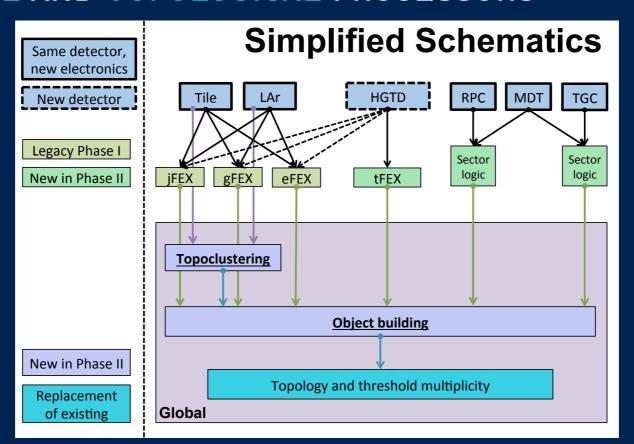
- + MOTIVATIONS FOR THE UPGRADE:
 - BETTER RADIATION TOLERANCE, BETTER PRECISION AND FINER TRIGGER GRANULARITY
 - INCREASED RATE AND LATENCY
 - AGEING OF COMPONENTS EXCEEDING THE DESIGN LIFETIME
- + NEW ELECTRONICS:
 - HIGH SPEED OPTICAL COMMUNICATION FOR FULL DATA TRANSMISSION AT 40 MHz TO OFF-DETECTOR ELECTRONICS
 - REDUCED MODULARITY
 - DIGITAL INFORMATION FOR THE LO/L1 TRIGGER SYSTEMS
 - FULL REDUNDANT DATA PATH AND POWERING





LEVEL-O CALORIMETER TRIGGER (LOCALO)

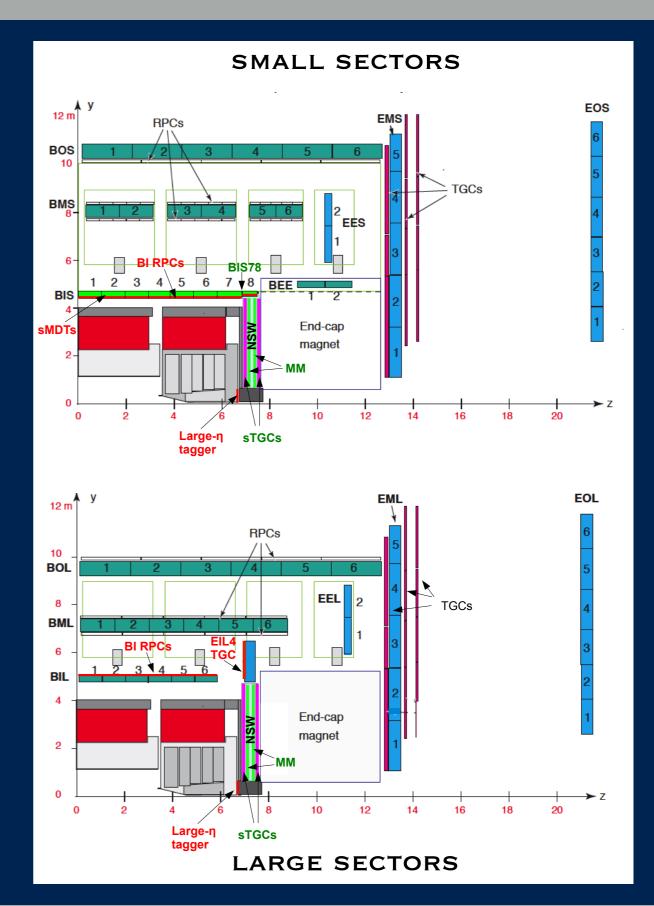
- + HIGH GRANULARITY FULL DATA DIGITAL TRANSMISSION FROM CALORIMETERS
- + LAR AND TILE CALORIMETER ARE SENT SEPARATELY TO FEATURE EXTRACTORS
- + FEXS IDENTIFY ELECTRON/PHOTON/TAU CANDIDATES (EFEX), JETS AND E_T (JFEX) AND LARGE-R JETS (GFEX)
- + HGTD POSSIBLE NEW INPUT TO EXTEND THE ELECTRON AND JET IDENTIFICATION
 CAPABILITIES AND TO PROVIDE PILEUP REJECTION IN THE FORWARD REGION
- + OUTPUTS TO GLOBAL AND TOPOLOGICAL PROCESSORS



MUON DETECTORS

+ MOTIVATION:

- REDUCE THE TRIGGER FAKE RATE IN BARREL AND END-CAP REGIONS
- INCREASE TRIGGER PERFORMANCES
- INCREASE GEOMETRICAL COVERAGE IN THE BARREL
- + NEW DETECTORS:
 - BARREL INNER RPC + SMDT:
 - + OLD BIS MDT REPLACED BY NEW (SMDT + RPC)
 - NEW RPC MOUNTED ON TOP OF EXISTING BIL MDT
 - TGC EIL4
 - LARGE-ETA-TAGGER: UP TO $|\eta|=4$; SEVERAL PHYSICS CHANNELS IDENTIFIED AND UNDER STUDY

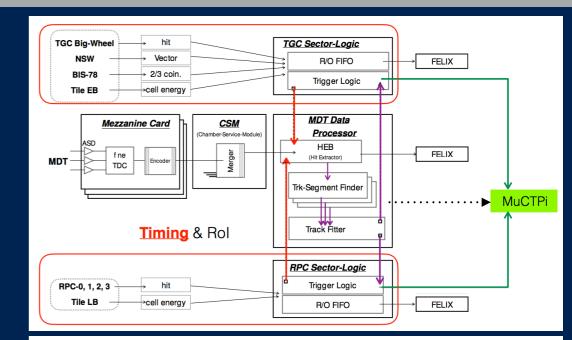


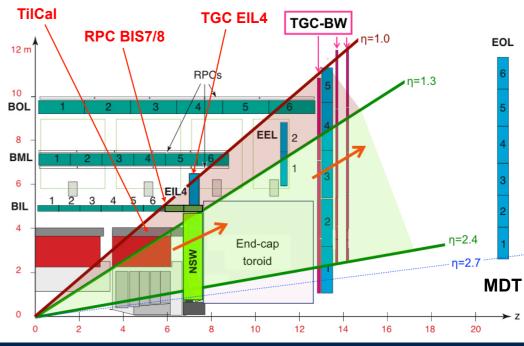
LEVEL-O MUON TRIGGER (LOMUON)

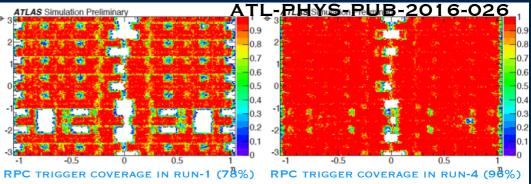
- * THE DATA FROM THE RPC, TGC, AND NSW DETECTORS USED IN THE PHASE-I SYSTEM WILL BE COMPLEMENTED WITH BI RPC, TILE CALORIMETER AND MDT
- * INCREASED SELECTION EFFICIENCY AND REDUCE FAKE TRIGGERS
- * NEW MDT TRIGGER SHARPENS TURN-ON CURVE AND INCREASE REJECTION POWER
- + POSSIBILITY TO LOOSE RPC TRIGGER SELECTION TO INCREASE THE GEOMETRICAL ACCEPTANCE IN THE BARREL, FROM ~70% TO ~95%
- + RATE SUPPRESSION OF $\sim 50\%$ FOR MUONS WITH P_T < 20 GEV
- * NEW ON-DETECTOR BOARDS FULL DIGITAL DETECTOR DATA SENT OFF-DETECTOR @ 40 MHz
- * BARREL AND END-CAP NEW OFF-DETECTOR

 BOARDSPERFORM THE TRIGGER ALGORITHM + SEND THE

 SEED TO THE MDT TRIGGER PROCESSORS
- * NEW MDT TRIGGER PROCESSOR BOARDS MATCH MDT HITS WITH THE RPC/TGC SEED VECTORS IN SPACE AND TIME (DIFFERENT ALGORITHMS FOR SEGMENT FINDING UNDER STUDY)



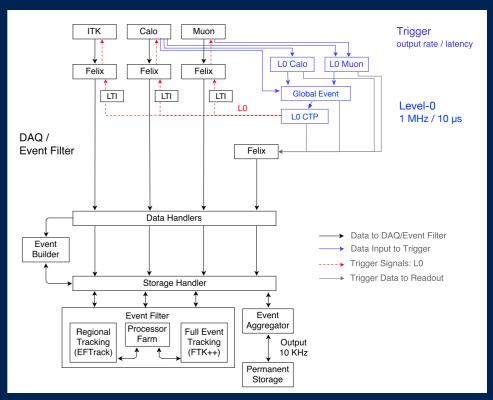




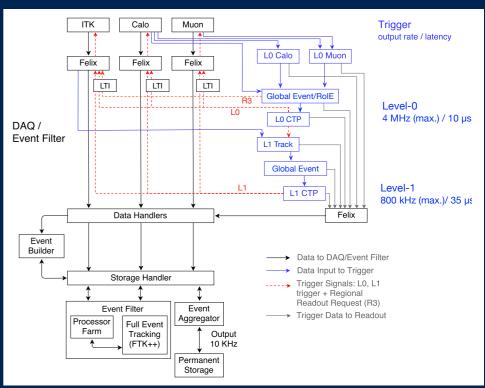
LEVEL-O AND LEVEL-O/LEVEL-1 TDAQ OPTIONS

- * LO TRIGGER RATE = 1 MHz; LO LATENCY = 10 μ s
- * THE GLOBAL EVENT PROCESSOR REPLACES THE EXISTING L1TOPO AND INTEGRATES TOPOLOGICAL FUNCTIONS WITH ADDITIONAL SELECTION ALGORITHMS USING ADDITIONAL INFORMATION FROM THE CALORIMETERS
- * LO/L1 SCHEMA INTRODUCES A SECOND LEVEL OF HARDWARE TRACK TRIGGER (PATTERN RECOGNITION WITH AM CHIPS + TRACK FITTING WITH FPGA)
- + LO TRIGGER RATE = 4 MHz; LO LATENCY = $10 \mu s$
- * L1 TRIGGER RATE = 800 KHz; L1 LATENCY = 35 μ s
- * THE LO GLOBAL EVENT PROCESSOR GENERATES THE COMMANDS REQUEST FOR THE READ OUT OF THE CORRESPONDING DATA FROM THE ITK DETECTOR
- + THE L1TRACK RECEIVES ROI DATA FROM ITK AND PERFORMS
 TRACK FINDING
- * THE L1 GLOBAL EVENT PROCESSOR REFINES **C/γ**, **T**, JETS AND E_T MISS SIGNATURES AND IMPROVES REJECTION BY COMBINING THE REFINED CALORIMETER SIGNATURE INFORMATION WITH THE TRACKING INFORMATION FROM L1TRACK

LEVEL-O ONLY SCHEMA



LEVEL-O/LEVEL-1 SCHEMA



CONCLUSIONS

- * THE LARGE DATASETS THAT CAN BE COLLECTED WITH THE HIGH-LUMINOSITY LHC WILL ALLOW TO PERFORM PRECISION MEASUREMENTS IN THE 125 GEV HIGGS BOSON SECTOR, THE SEARCH FOR RARE HIGGS BOSON DECAY MODES AND THE STUDY OF LOW PRODUCTION CROSS SECTION STANDARD MODEL PROCESSES, AS WELL AS THE SEARCH FOR NEW PHENOMENA BEYOND STANDARD MODEL
- + PHASE-I UPGRADES:
 - ADVANCED STATE, PRODUCTION STARTING SOON FOR MOST OF THE SYSTEMS
 - PROVIDES IMPROVED RATE CAPABILITIES AND BACKGROUND REJECTION FOR L=2-3x10 CM S
- + PHASE-II UPGRADES:
 - 34 -2 -1 -1 - DESIGNED FOR L=5-7.5 x 10 CM S AND 3000 FB
 - UP TO FACTOR 10 INCREASE IN RADIATION HARDNESS
 - IMPROVED PILE-UP HANDLING WITH NEW TRACKER AND POSSIBLE TIMING DETECTOR
 - TRIGGER AND READOUT CAPABILITIES
 - DIFFERENT OPTIONS FOR THE UPGRADES UNDER EVALUATION
 - TDR BY THE END OF 2017 (STRIP ITK TDR RECENTLY SUBMITTED)