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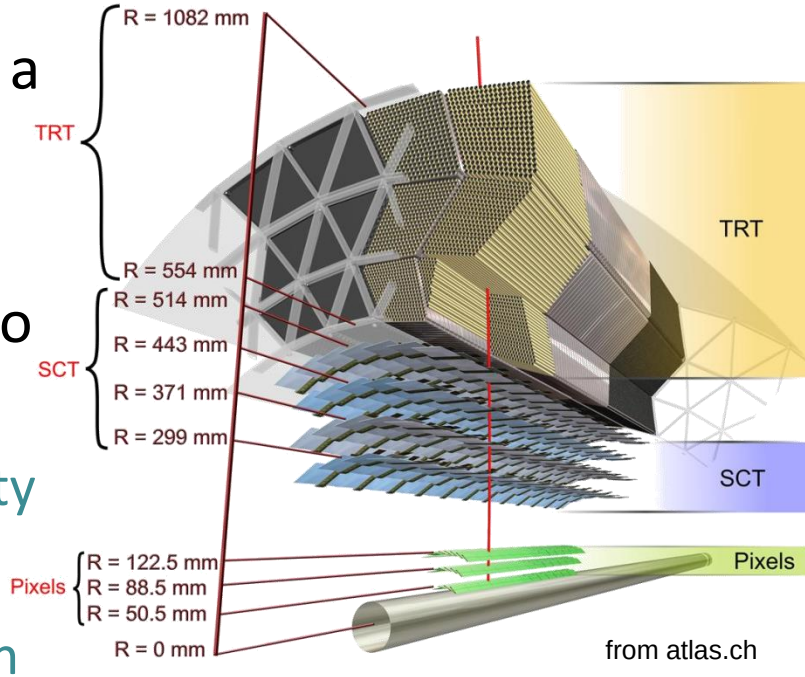
The ATLAS Upgraded Tracker for the High-Luminosity LHC

Jens Dopke for the ATLAS Collaboration

Introduction (current ATLAS Tracker)

- Tracking of charged particles with a <10um on track resolution
  - Using about 36 hits per track
- Designed for the LHC lifetime up to long shutdown 3
  - 300 fb^{-1} total integrated luminosity
  - 1e34 $cm^{-2}s^{-1}$ instant. luminosity
  - Currently operated beyond design



from atlas.ch

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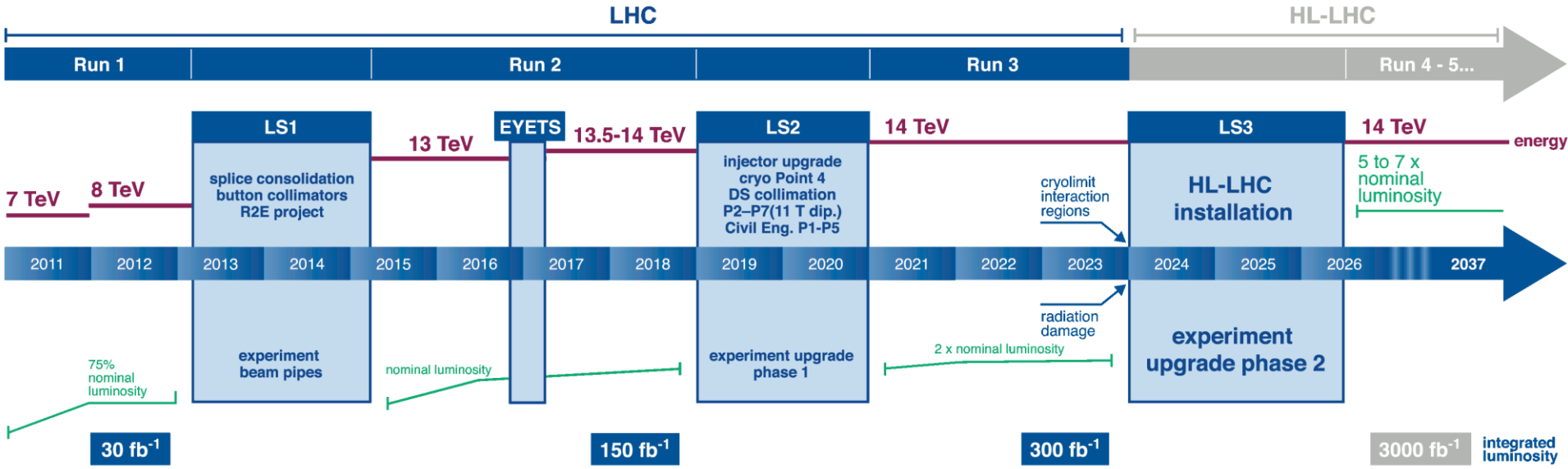
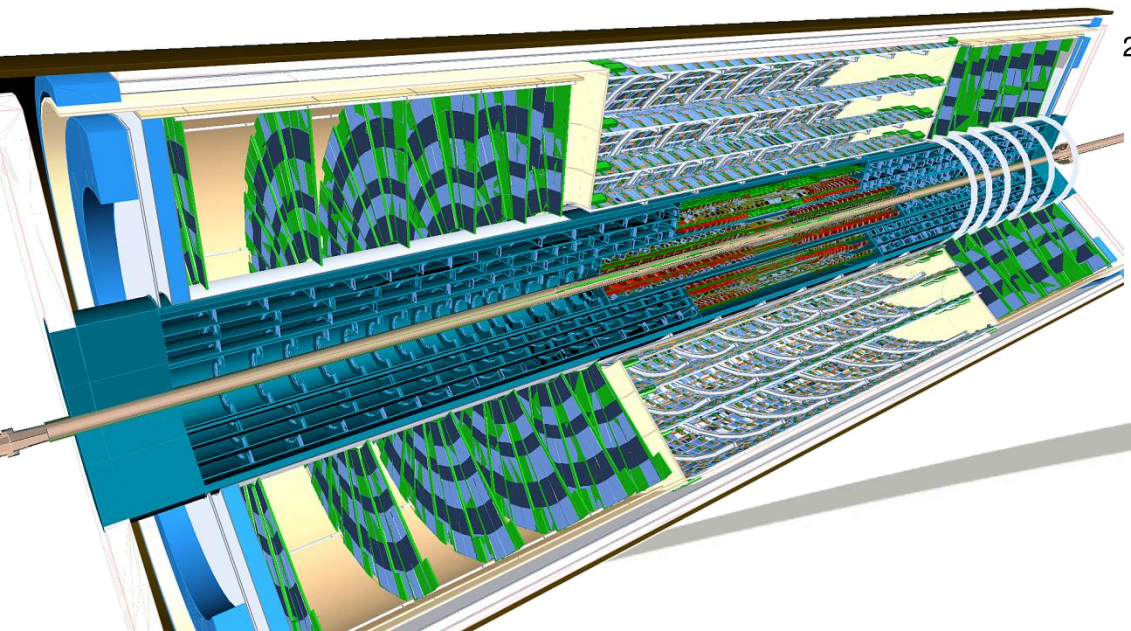
Expectations for the HL-LHC

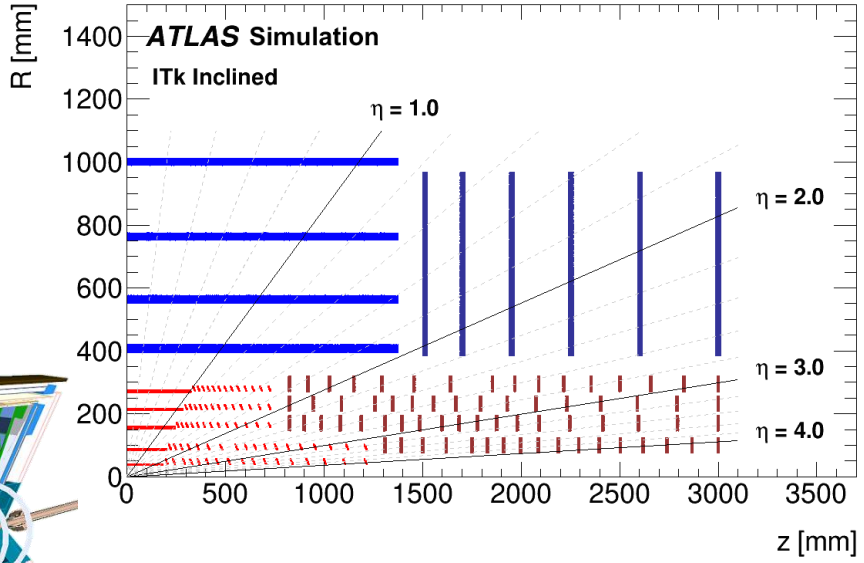


- Higher Luminosity leading to higher:
  - Occupancy (transmission rate limits): expected up to 200 interactions per bunch crossing - current Strips fall over at ca. 85 PU
  - Radiation damage – designing to 4000 fb^{-1}
  - Resolution
    - TRT saturation
    - Higher P_T expectation, hence higher track density in jets
- More recent hardware allowing for better detectors to be built

The Inner Tracker (ITk) upgrade

- Future all Silicon based tracker
  - Outer Strip tracker
  - Inner Pixel tracker
- Total of >13 hits per track
- Eta coverage up to |4|





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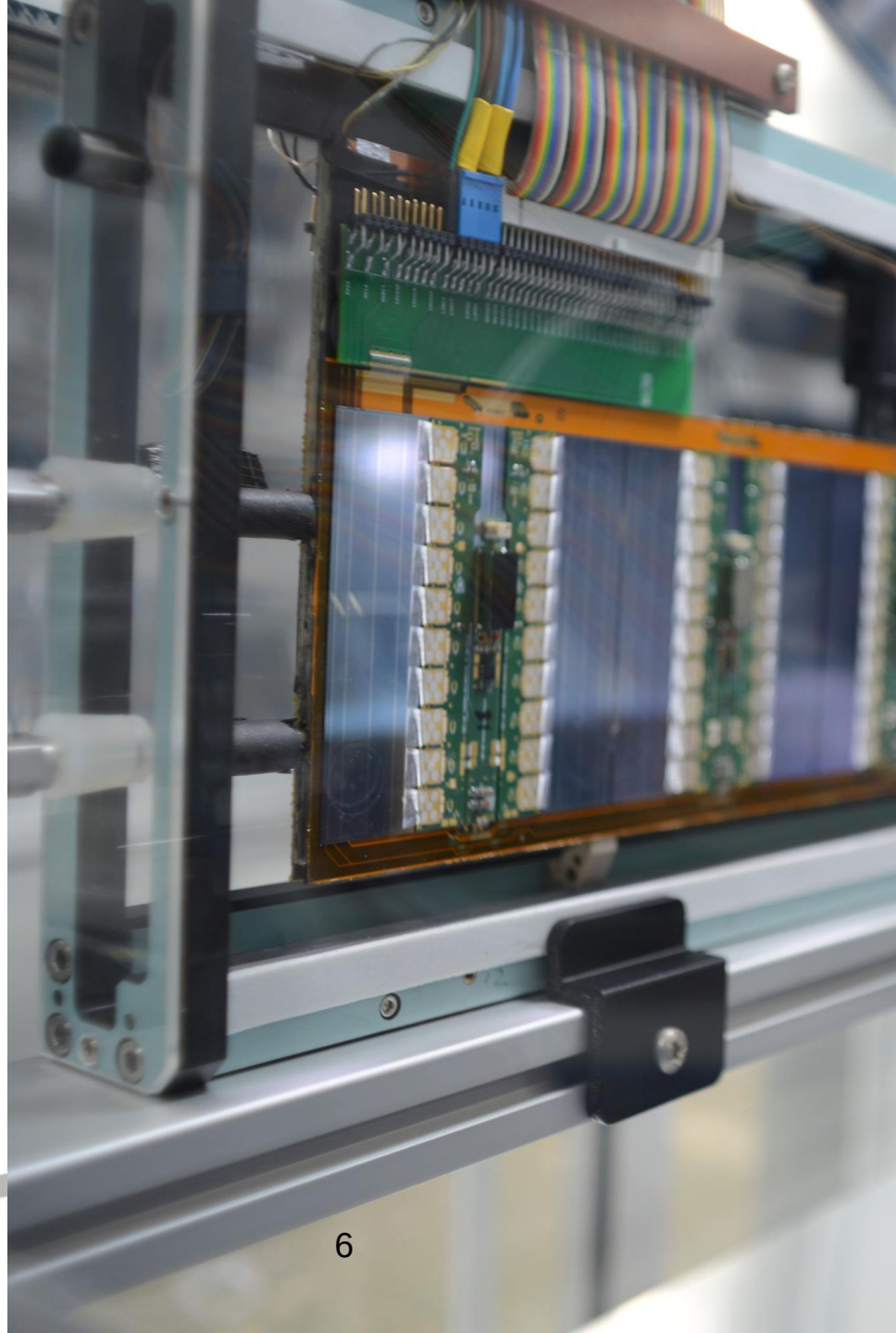
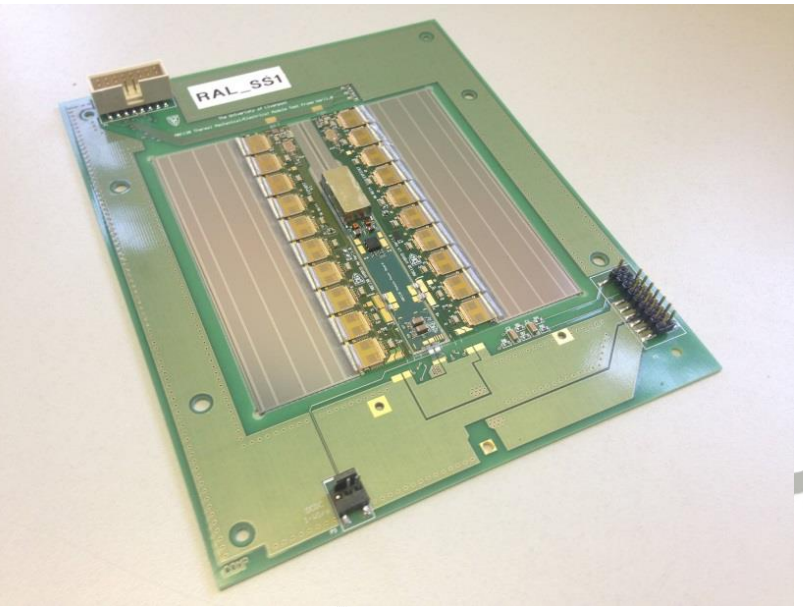
Strip Tracker

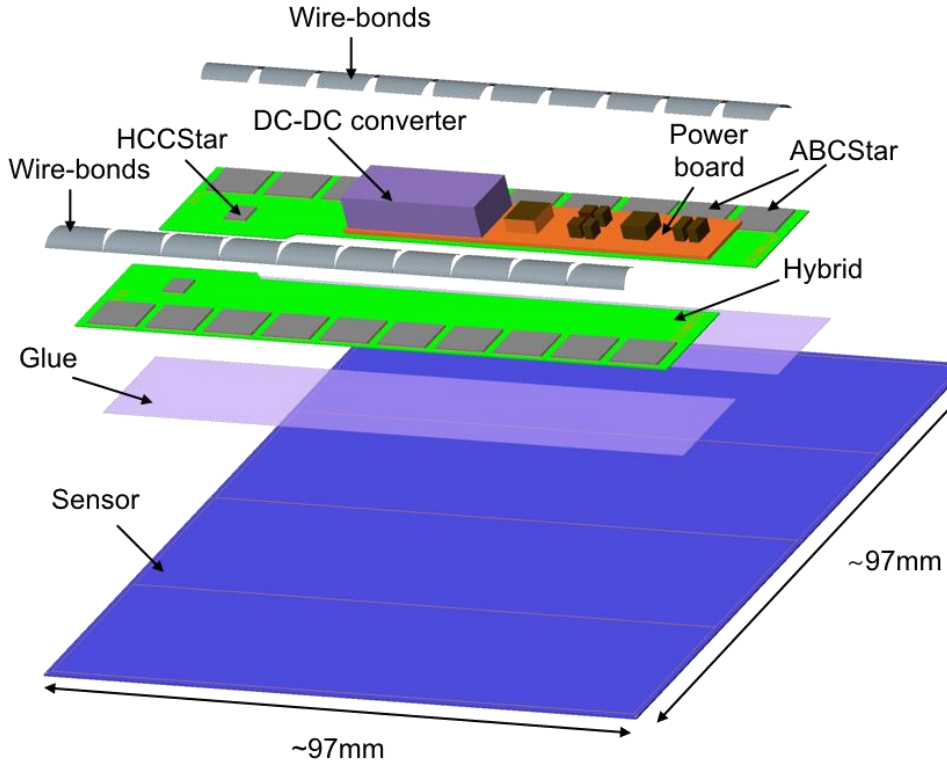
- 4 Barrel layers, 6 end-caps disks per side
  - All endcap disks are the same
  - Barrel layers differ inner/outer in the types of modules they employ
- Just short of 18000 sensor tiles, 165m^2 silicon
- Total available readout bandwidth around 18Tbit/s



Barrel Modules

- Sensors are n-in-p
  - 5k/2.5k sensing elements
- Front-end ASICs are 130nm feature size
- Local power conversion from >10V down to 1.5V





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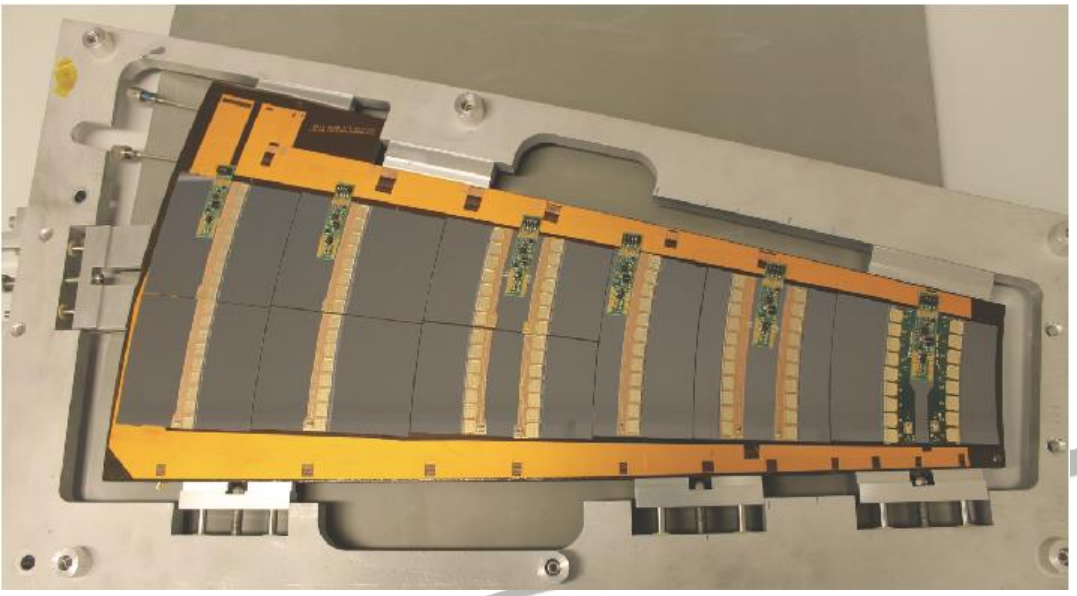
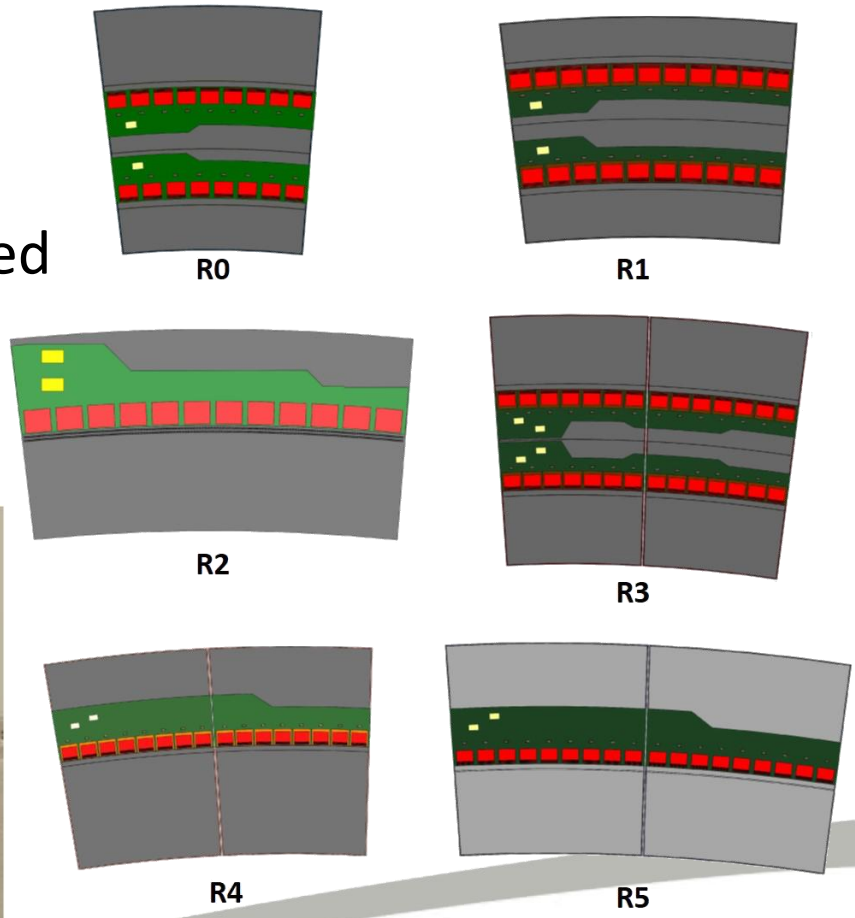
Endcap Modules

- Round sensor edges!
- Increased complexity due to multiple sensors being interlinked
- Strip length varies with radius





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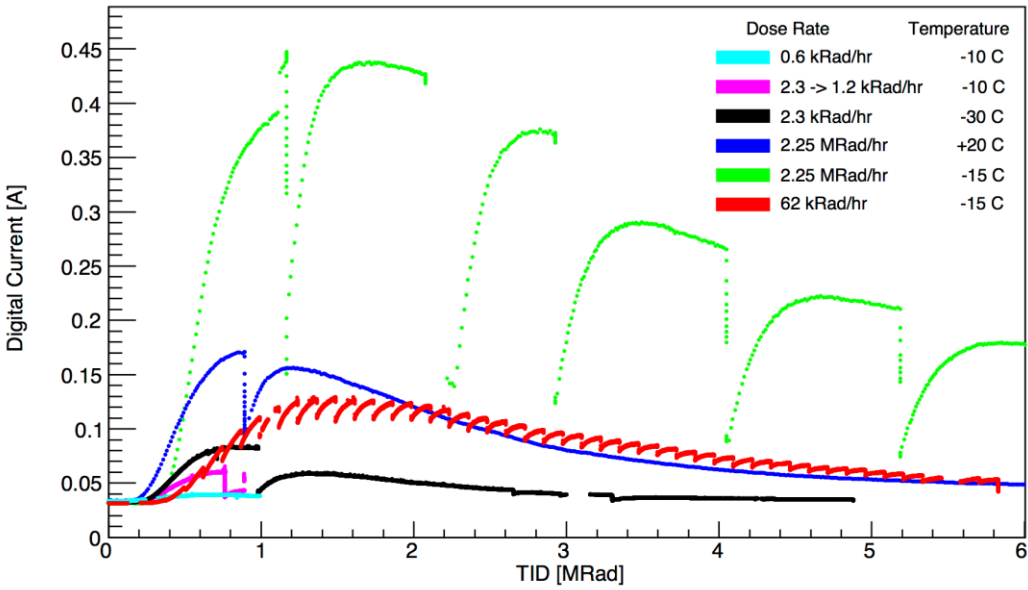
Radiation Hardness

- ITk Strip Tracker requires 10 times the previous tracker radiation hardness:
  - 1e15 n/cm^2 NIEL
  - O(100Mrad) ionising
  - New sensors acquire electrons
- New technology nodes suffer from radiation induced power consumption
  - Currently evaluating the combined effect on the system load



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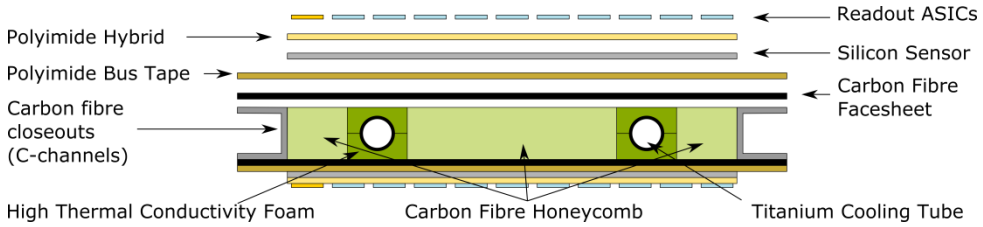
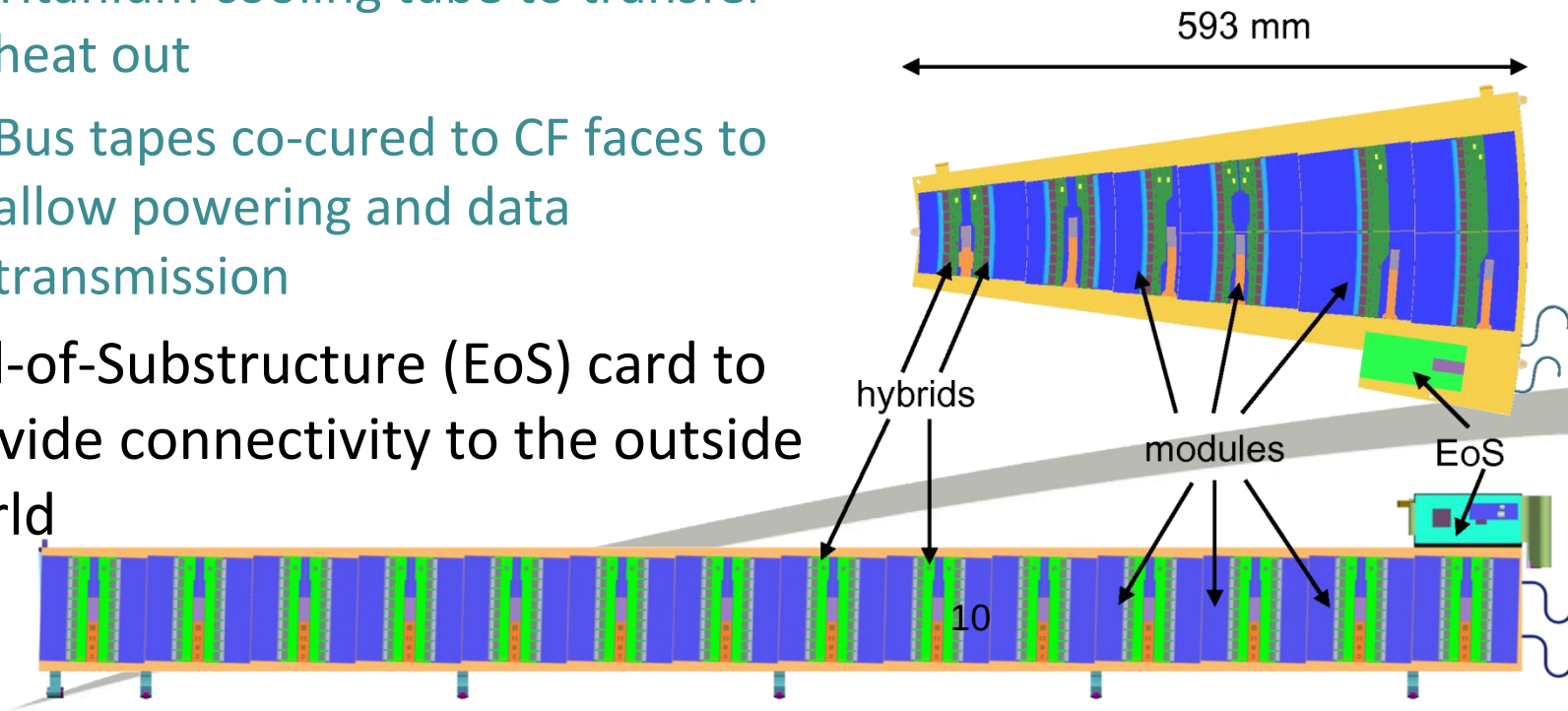
Local Support Structures

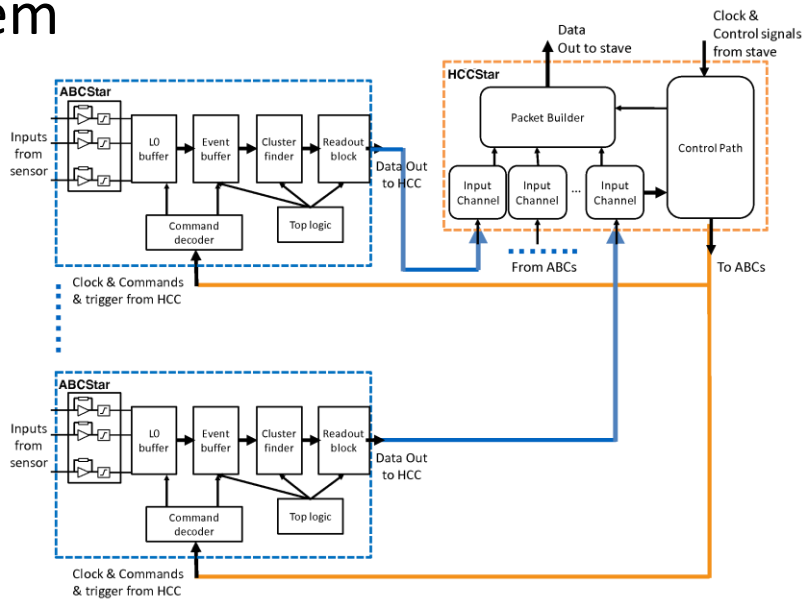


- Local support cores for barrel and endcap based on the same concept:
  - Carbon fibre sandwich panel
  - Titanium cooling tube to transfer heat out
  - Bus tapes co-cured to CF faces to allow powering and data transmission
- End-of-Substructure (EoS) card to provide connectivity to the outside world



Readout

- Baseline 1MHz trigger rate system
  - Required a new readout scheme within each module: Star architecture
  - Still supporting a two stage trigger system (4M/ca. 500k)
- 640Mbit/s downlinks from each hybrid controller chip
- Shared 160Mbit/s control link
- Links are aggregated through 1 or 2 CERN lpGBT(s) at the end-of-substructure card (10/20 Gbit/s per side)
  - Optical transmission from here



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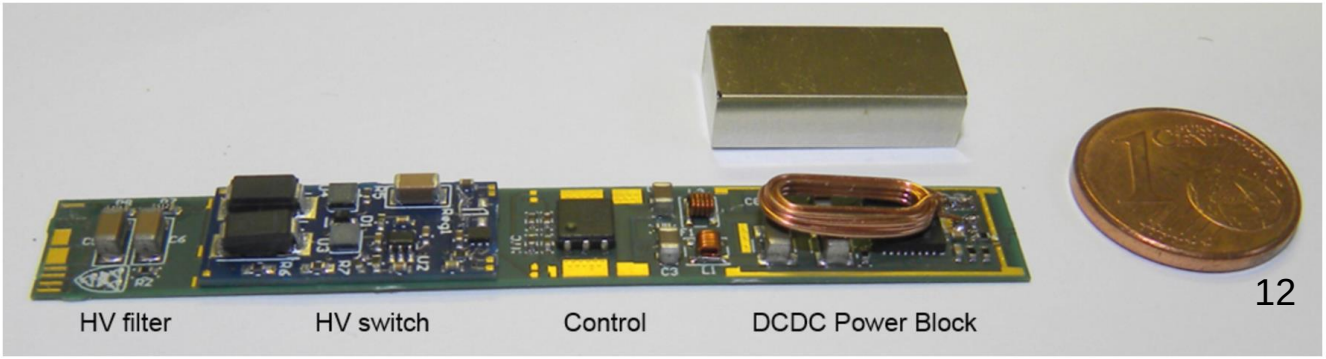
Services

- To minimise the outside power consumption, the strip detector operates low voltage powering based on a 2-step DC-DC conversion:
  - 48V to 12V at high radius (O(5m)) within the ATLAS detector
  - 12V to 1.5V only at the module
    - Reduces current supplied within the local support structure and therefore material within the tracker
- Only two temperature sensors per local support structure will be wired out directly (allowing cooling system interlocks)
  - All other monitoring will be merged into the data stream, allowing fine grained monitoring
- Optical readout through new optical fibre cables



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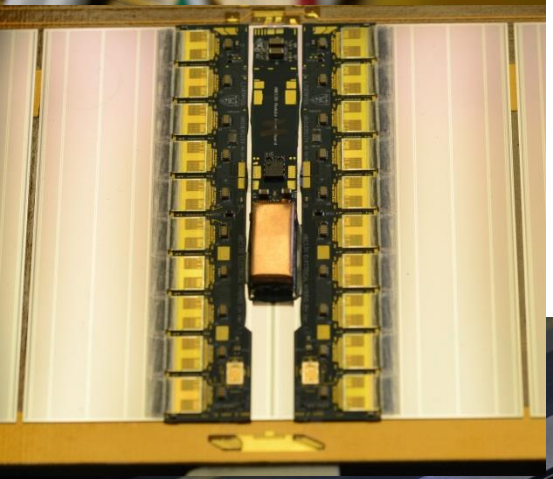

Current Status

- With the TDR published, the strip detector project is currently undergoing production preparation
- All Object types have been built (excluding global structures)
- Production methods are still being refined

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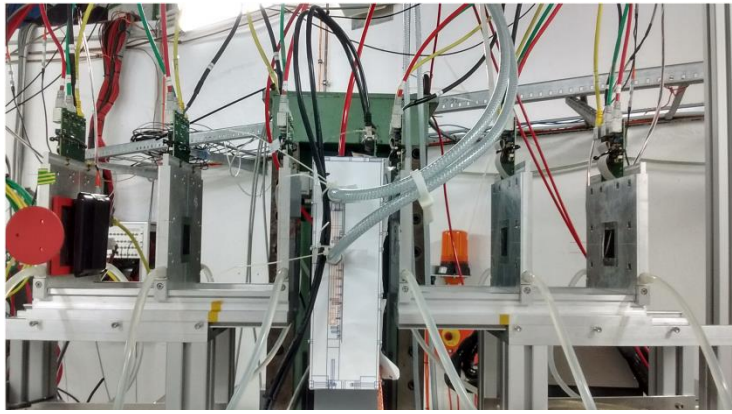
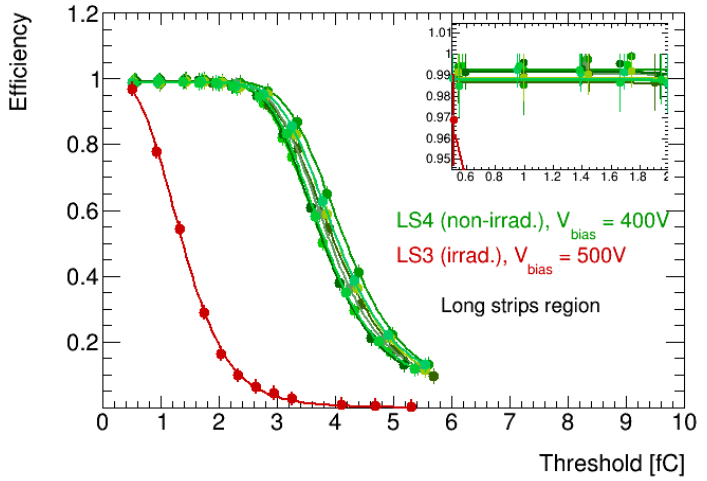
Testbeam results

- Multiple Modules of different dimensionality and irradiation level operated successfully in test beams
- Given current sensors and ASICs, we expect better than 20:1 S/N after irradiation in the final chipset
  - New Frontend amplifier design in response to current 130nm ASIC behaviour, already proven in silicon





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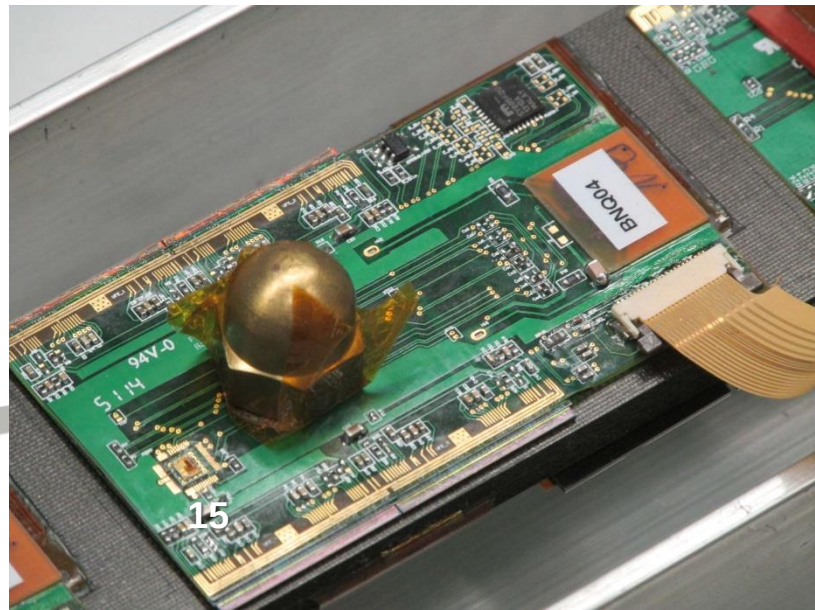
A word on Pixels

- New Front-end ASIC in 65nm technology:
  - Analogue frontend already tested as standalone circuit
  - First full chip revision expected soon
- Modules built from 1-4 Front-end ASICs
- Strip-equivalent local support structures, but:
  - Smaller structures
  - Higher power densities
  - Higher readout rates

4 Chip Module



Summary & Outlook

- The ITk strip tracker project recently published its TDR: https://cds.cern.ch/record/2257755?ln=en
- Prototyping has gone through O(10) years of ASIC, module and structure design
  - Structures are going through last changes as per layout taskforce recommendation (longer staves)
  - Next Asics round is expected to be production material
- Pre-production of the ITk strip tracker to start in 2018
  - Production procedures are still being refined, but working
- Expecting to write the ITk pixel TDR within this year