Inductive Adders for Ultra-stable Kicker Pulse Generation

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Outline

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  - Specifications for CLIC DR Extraction Kicker System
  - Challenges and Issues
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  - Methods to Improve the Pulse Flat-top Stability
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  - Specifications for the Two 3.5 kV Prototype Inductive Adders
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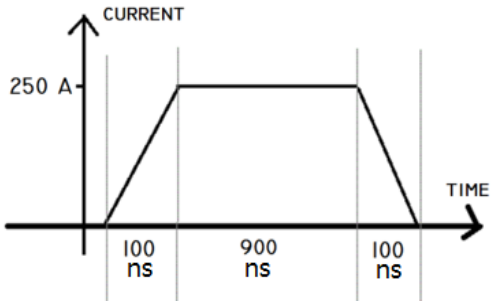
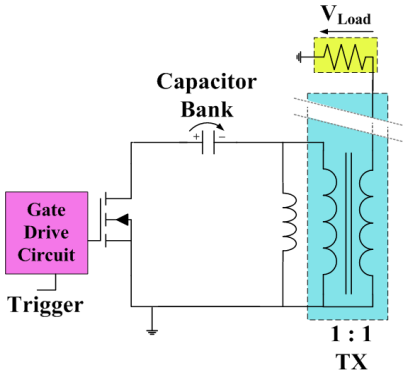
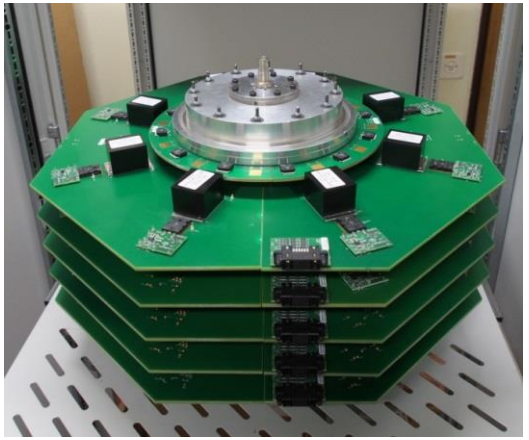
  - Evaluation of Magnetic Core Material for 12.5 kV Prototypes
  - Summary of Measurements with 3.5 kV Prototypes
- **12.5 kV Prototype Inductive Adders**
  - Initial Measurements on Pulse Flat-top Stability and Repeatability
- **Summary and Future Work**



Ideal stripline current for 1 GHz option

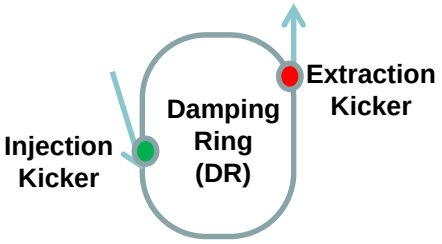




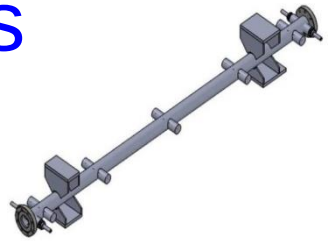
Specifications for the CLIC DR Extraction Kicker Systems

	CLIC DR (1 GHz | 2 GHz)
Pulse voltage (kV) (per Stripline)	±12.5
Stripline pulse current [50 Ω load] (A)	±250
Repetition rate (Hz)	50
Pulse flat-top duration (ns)	~160 | ~900
Flat-top repeatability	$\pm 1 \times 10^{-4}$ (±0.01 %)
Flat-top stability [inc. droop], (Inj.) per Kicker SYSTEM (Ext.)	$\pm 2 \times 10^{-3}$ (±0.2 %) $\pm 2 \times 10^{-4}$ (±0.02 %)
Field rise time (ns)	1000
Field fall time (ns)	1000
Beam energy (GeV)	2.86
Total kick deflection angle (mrad)	1.5 (0.09 deg)
Aperture (mm)	20
Effective length (m)	1.7
Field inhomogeneity (%) [3.5mm radius] [1mm radius]	±0.1 (Inj.) ±0.01(Ext.)

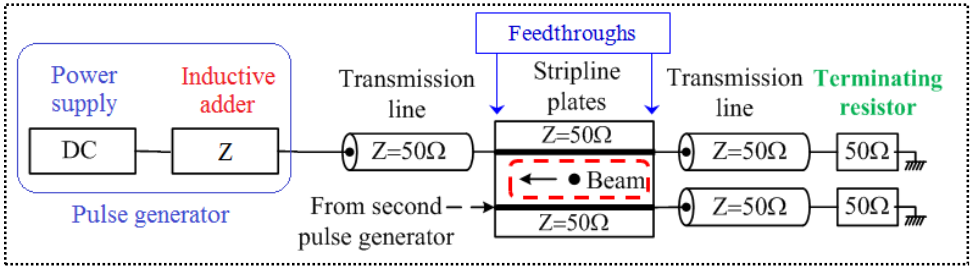
- **NOTE:**
  - **Extremely tight requirements for flat-top stability and repeatability!**
  - **For rise/fall times, ≤ 100 ns desired!**



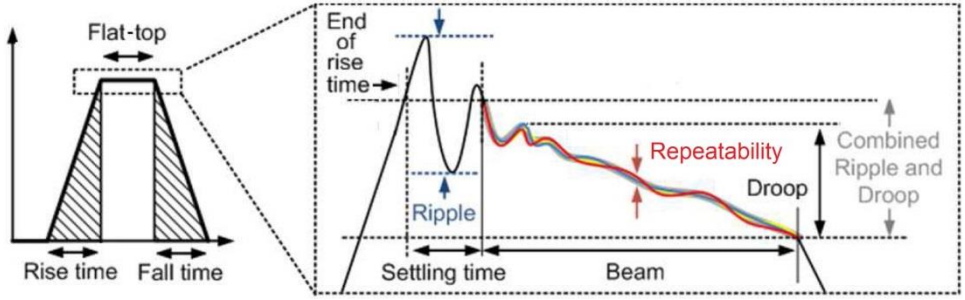
Damping ring kickers



Drawing of the CLIC DR extraction kicker
(Courtesy of C. Belver-Aguilar)

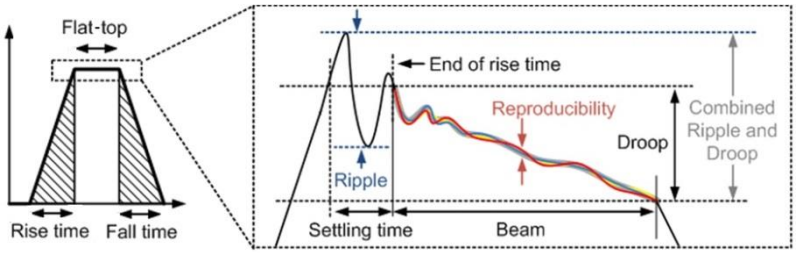


Schematic of a kicker system

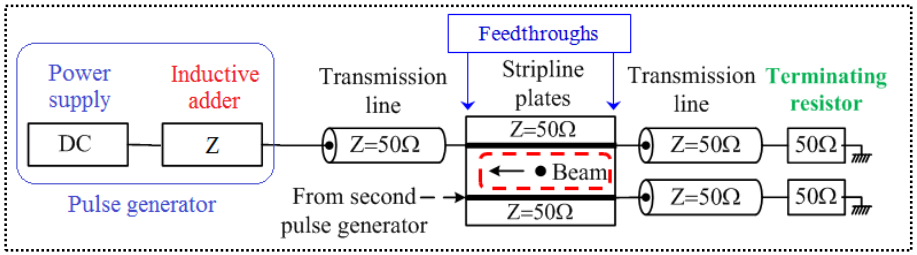


CLIC DR kicker pulse definition

Challenges and Issues

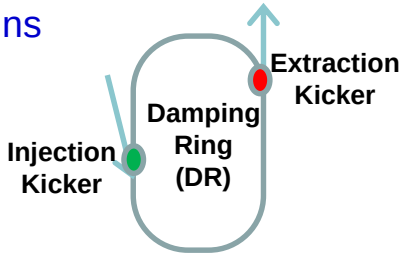


CLIC DR kicker pulse definition



Schematic of a kicker system

- **±0.02 % (± 2.5 V)** requirement for the **flat-top stability** of ±12.5 kV, 160 to ~900 ns pulse is an extremely demanding specification!
  - **An order of magnitude better than in any existing kicker systems!**
  - **Compensation of droop and ripple of the output voltage is required.**



- Adequate impedance matching to minimize duration of settling time:
  - Impedance (and field homogeneity) of the stripline kicker has been optimized: unfortunately the impedance cannot be 50 Ω for both power-off (even) and power-on (odd) operation modes!
  - Odd-mode impedance of the striplines is ~41 Ω (see talk by C. Belver-Aguilar), which causes settling time to be ~100 ns. Therefore **the pulse flat-top duration is at least ~260 | ~1000 ns** (1 | 2 GHz option for DRs)
- Suitable high precision measurements of the pulse in the laboratory:
  better relative precision than ±2.5 V in 12.5 kV required!

Inductive Adder

- Many primary “layers”, each with solid-state switches
- The output voltage is approximately the sum of the voltages of the primary constant voltage layers

+ Control electronics referenced to ground

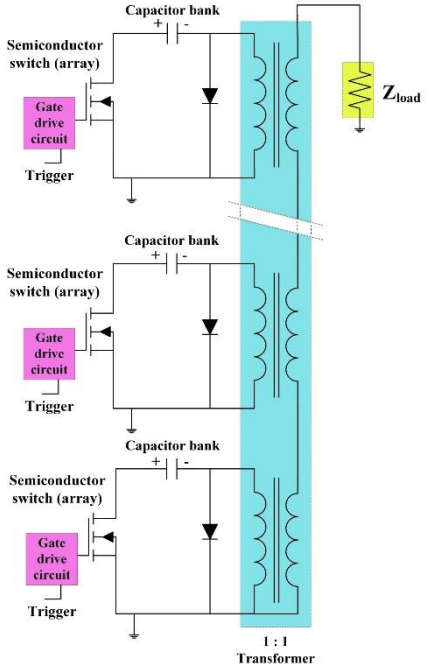
+ No electronics referenced to high voltage despite the high voltage output of the adder

+ The output voltage can be modulated during the pulse with an analogue modulation layer

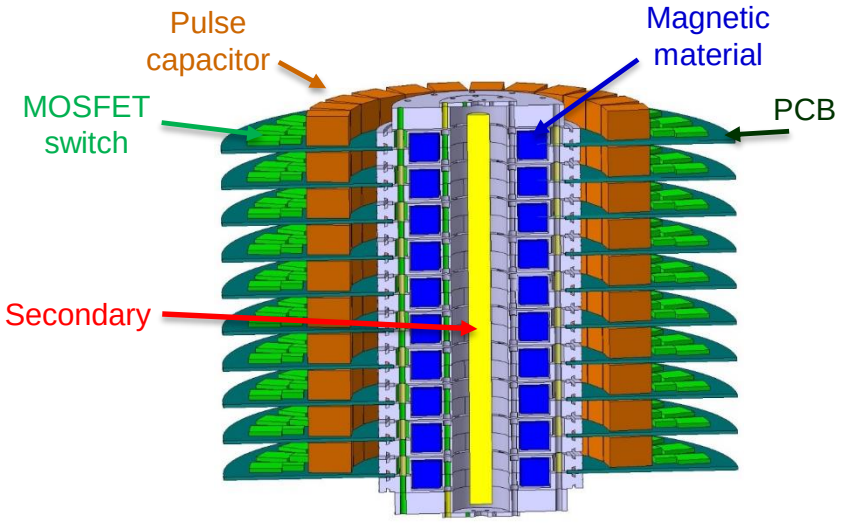
+ Modularity: the same design can potentially be used for kickers with different specifications (CLIC PDR & DR kicker modulators)

+ Redundancy and machine safety: if one switch or layer fails, the adder still gives full voltage or a significant portion of the required output pulse

+ Possibility to generate positive or negative output pulses with the same adder: the polarity of the pulse can be changed by grounding the other end of the output of the adder



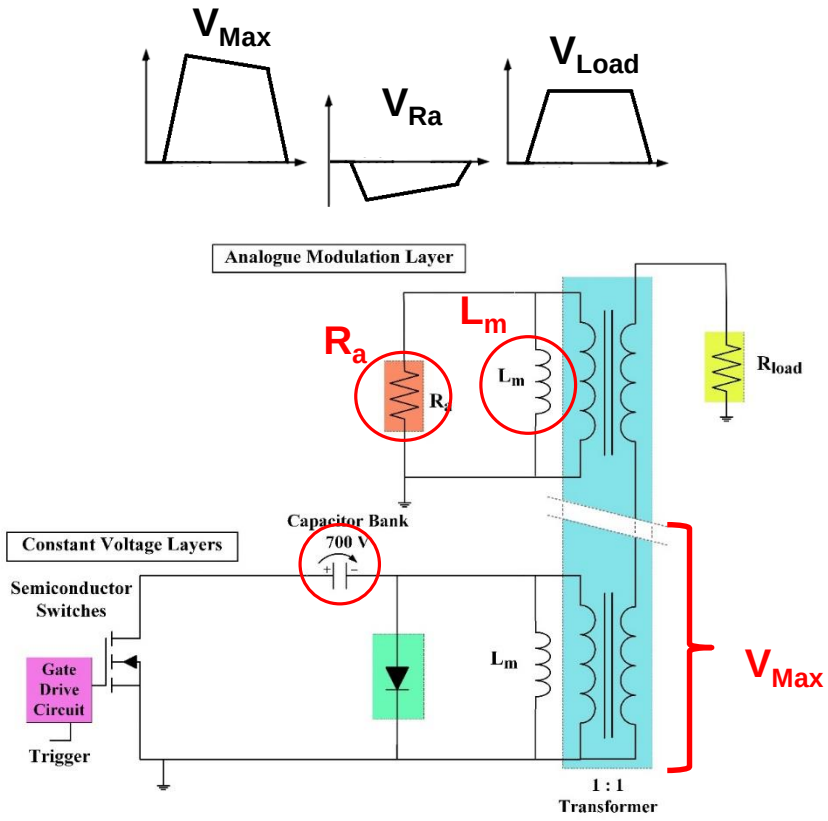
Schematic of an inductive adder



Cross-section of an inductive adder

Improving the Pulse Stability: Passive Modulation

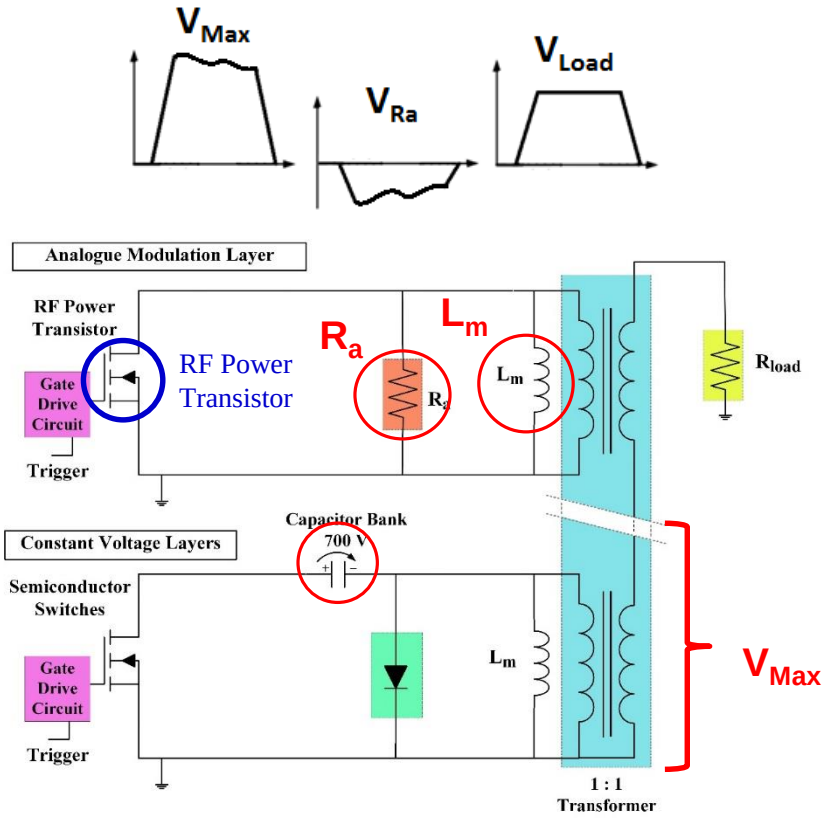
- Droop and ripple of the output pulse of an inductive adder can be compensated with an analogue modulation layer
- In the analogue modulation layer, resistor R_a is effectively in series with the load
- The load voltage is the sum of the voltages across all of the layers.
- Two modes:
  - **Passive mode:** During the pulse, current through $\boldsymbol{L_m}$ increases, which causes current through $\boldsymbol{R_a}$ to decrease. Therefore, voltage over $\boldsymbol{R_a}$ decreases, which can compensate for a reduction (droop) in the primary voltage of the other layers.



Passive analogue modulation

Improving the Pulse Stability: Active Modulation

- Droop and ripple of the output pulse of an inductive adder can be compensated with an analogue modulation layer
- In the analogue modulation layer, resistor R_a is effectively in series with the load
- The load voltage is the sum of the voltages across all of the layers.
- Two modes:
  - **Passive mode:** During the pulse, current through L_m increases, which causes current through R_a to decrease. Therefore, voltage over R_a decreases, which can compensate for a reduction (droop) in the primary voltage of the other layers.
  - **Active mode:** A linear RF power transistor is connected in parallel with resistor R_a. The voltage across R_a can be controlled by controlling the current through the RF power transistor.

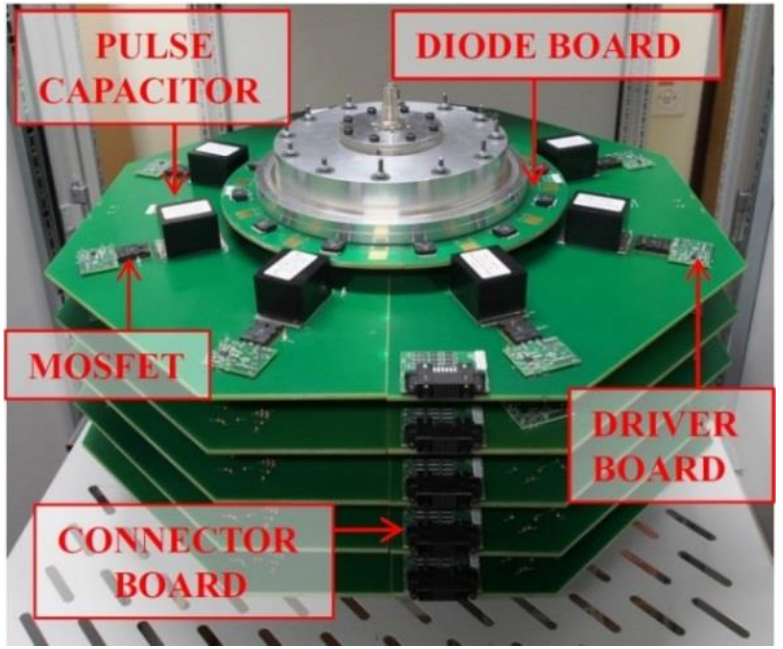


Active analogue modulation

Two 5-Layer Prototype Inductive Adders

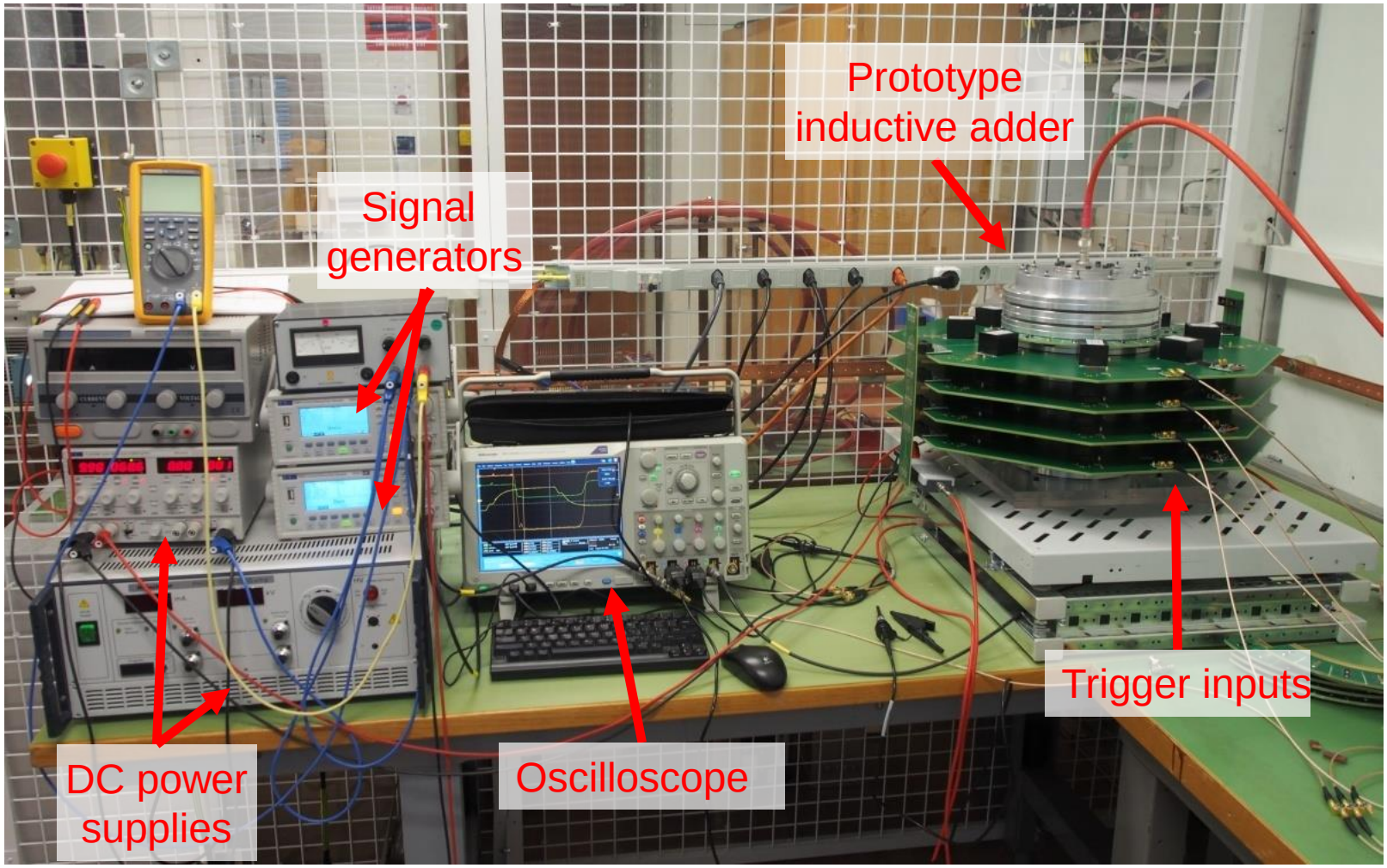
- The purposes of the prototype inductive adders have been:
  - To verify theoretical models, which have been used to predict the operation of an inductive adder with extremely high flat-top stability
  - To verify experimentally design steps for an inductive adder with high flat-top stability
  - To test main components (MOSFETs, pulse capacitors, magnetic cores)
  - To test both passive and active analogue modulation
  - To approach the required ±0.02 % flat-top stability for the output pulse, as specified for the CLIC DR extraction kicker system
  - To evaluate magnetic core material for the 12.5 kV prototype inductive adder

Design Parameter	Prototype Inductive Adder	CLIC DR Extraction Kicker Modulator
Output Voltage (kV)	**3.5**	12.5
Output Current [50 Ω load] (A)	**70 (250)**	250
Voltage per layer	**700**	700
Number of layers	**5**	20
Pulse flat-top duration (ns)	**Up to 900**	160 – 900
Pulse rise time [0.1-99.9 %] (ns)	**≤ 100**	< 1000
Pulse fall time [0.1-99.9 %] (ns)	**≤ 100**	< 1000
Flat-top stability (for 160 ns)	**≤ ±0.02 %**	±0.02 %
Repetition rate (Hz)	**50**	50



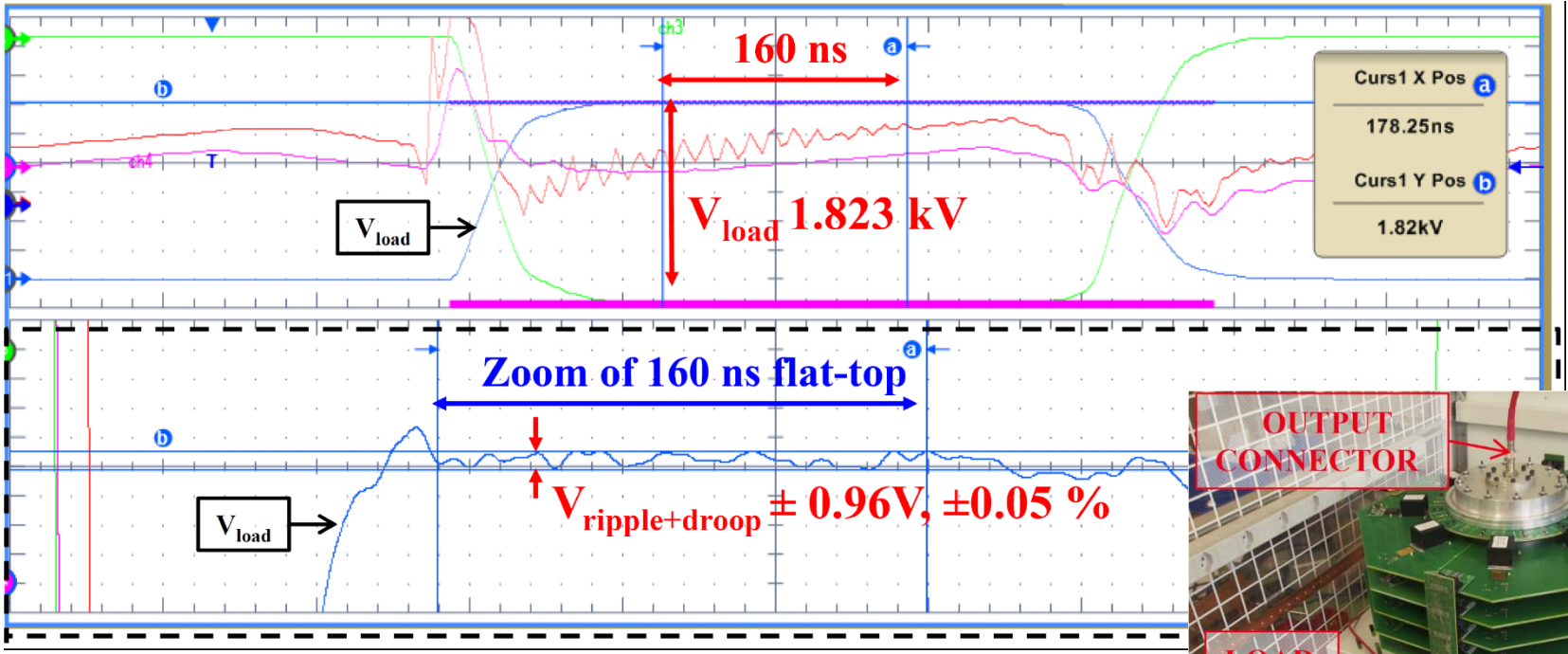
A prototype inductive adder

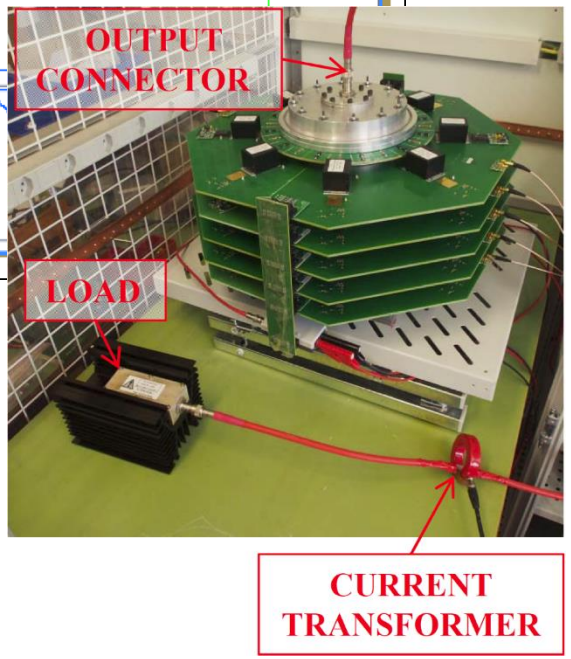
Measurements on the First 5-Layer Prototype Inductive Adders



The prototype inductive adder with the measurement setup

Measurements on Prototypes 1&2:



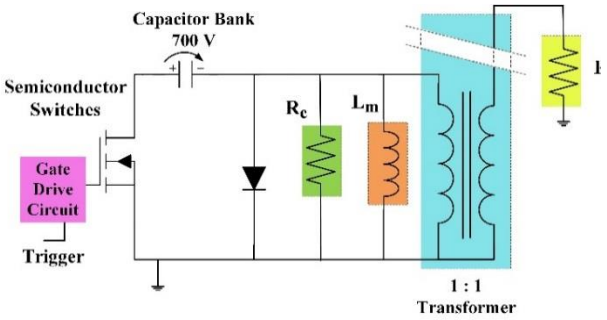


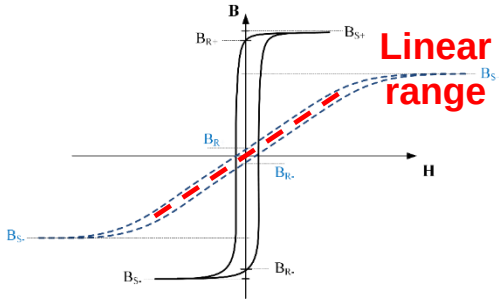
- **Setup for the measurement:**
  - Vacuumschmelze W567 cores
  - 4 constant voltage layers
  - 1 active analogue modulation layer
  - 1 branch powered per half-layer PCB, 2 branches per layer
  - Capacitors (24 µF/layer) initially charged to 551 V
  - **Active compensation of droop and ripple**
  - **Measurements with a 8-bit oscilloscope (average of 1000 pulses)**

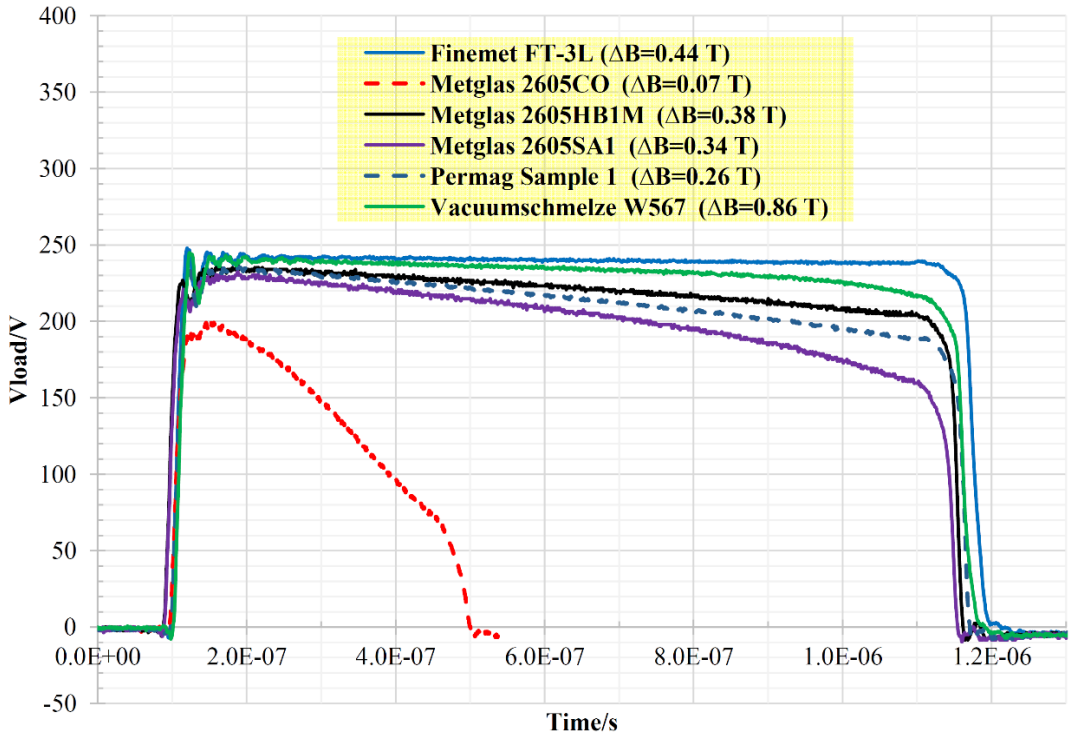
⇨ ±0.05 % (±1 V) flat-top stability over 160 ns

Evaluation of Magnetic Core Material for 12.5 kV Prototypes – No Biasing

- Setup for Measurement:
  - Output voltage of a 5-layer, 3.5 kV, inductive adder with a single layer powered (250 V)
  - No biasing applied
- Six different materials evaluated: Vacuumschmelze Vitroperm 500 F, Metglas 2605CO, Metglas 2605SA1, Metglas 2605HB1M, Permag ”sample”, Finemet FT-3L.
- Best candidates without biasing: Vacuumschmelze Vitroperm 500 F and Finemet FT-3L:
  - Lowest remanent field.
  - Lowest losses
- Limitations of Vacuumschmelze cores:
  - Not available in custom sizes and insulation in small quantities (in 2014)
  - ”Standard” insulation between ribbon layers is not adequate for this application.
- **Finemet FT-3L chosen for 12.5 kV prototypes.**







Summary of the Measurements with two 3.5 kV prototypes

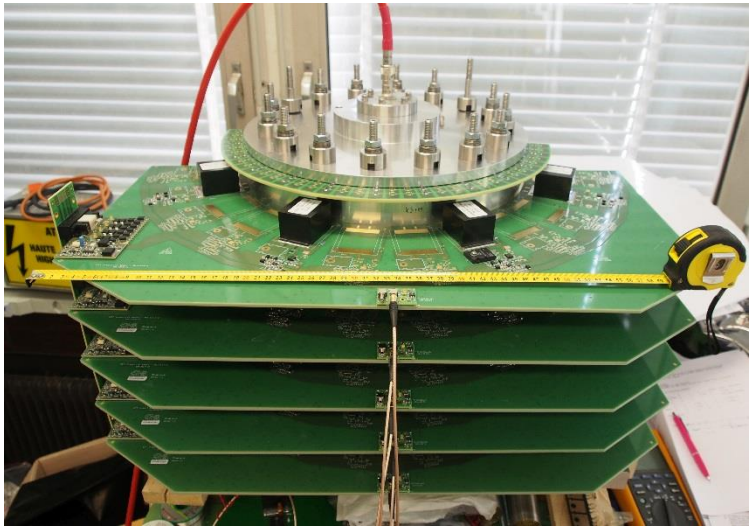
- The required absolute stability (in absolute numbers) was achieved for all damping ring kicker systems (≤ ±2.5 V). Hence, the pulse power modulators for the kicker systems for the CLIC damping rings are very probably feasible.
- The required relative stability (relative to the pulse voltage or current) was not reached for the DR extraction kicker systems (≤ ±0.02 %).
- The required resolution for the direct electrical measurement of the pulse waveform is very close to the limit of the measuremen set-up (Bergoz CT-E.01 current transformer & 8-bit Tektronix oscilloscope DPO 5034).
- Hardware limitations:
  - Maximum voltage up to 3.5 kV
  - Maximum pulse duration up to 350 ns flat-top at 700 V per layer (restricted by cross-sectional area of available magnetic cores)
  - 2 branches powered per layer (increased the amplitude of the droop to be compensated)
  - No amplifier between an RF power transistor and signal generator in the active analogue modulation layer (low gain)
- Magnetic core material evaluated for the 12.5 kV prototype inductive adders

Design of full-scale 12.5 kV Inductive Adders

- Specifications according to requirements for CLIC DR extraction kicker.
- Two 12.5 kV inductive adders needed to power a stripline kicker.
- Target flat-top stability ±0.02 % for 900 ns, target flat-top repeatability ±0.01 % for 900 ns.
- Mechanical design and PCB design compatible with 17.5 kV (to a 50 Ω load)
  - Modifications required: 8 more layers and change of the secondary (a straight rod)
  - 17.5 kV required for CLIC PDR kickers and to test idea of combined extraction + abort kicker for CLIC DRs)
- Status: first 5 ”full-scale” layers assembled and measurements commenced.

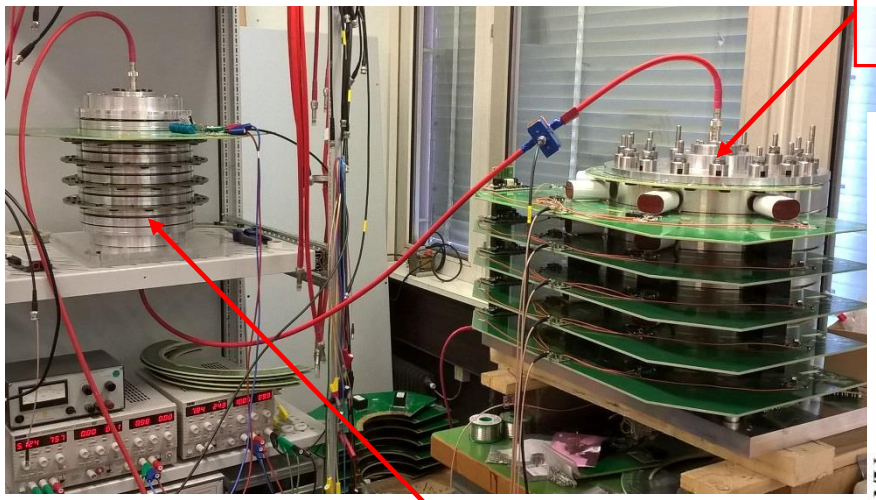
Design Parameter	12.5 kV Prototype Inductive Adder	CLIC DR Extraction Kicker Modulator
Output Voltage (kV)	**12.5**	12.5
Output Current	**305***	250
Voltage per layer	**700**	700
Number of layers	**20**	20
Pulse flat-top duration (ns)	**1100**	160 – 900
Pulse rise time [0.1-99.9 %] (ns)	**100**	< 1000
Pulse fall time [0.1-99.9 %] (ns)	**100**	< 1000
Flat-top stability (for 900 ns)	**≤ ±0.02 %**	±0.02 %
Flat-top repeatability (for 900 ns)	**≤ ±0.01 %**	±0.01 %

*Stripline odd-mode impedance 41 Ω



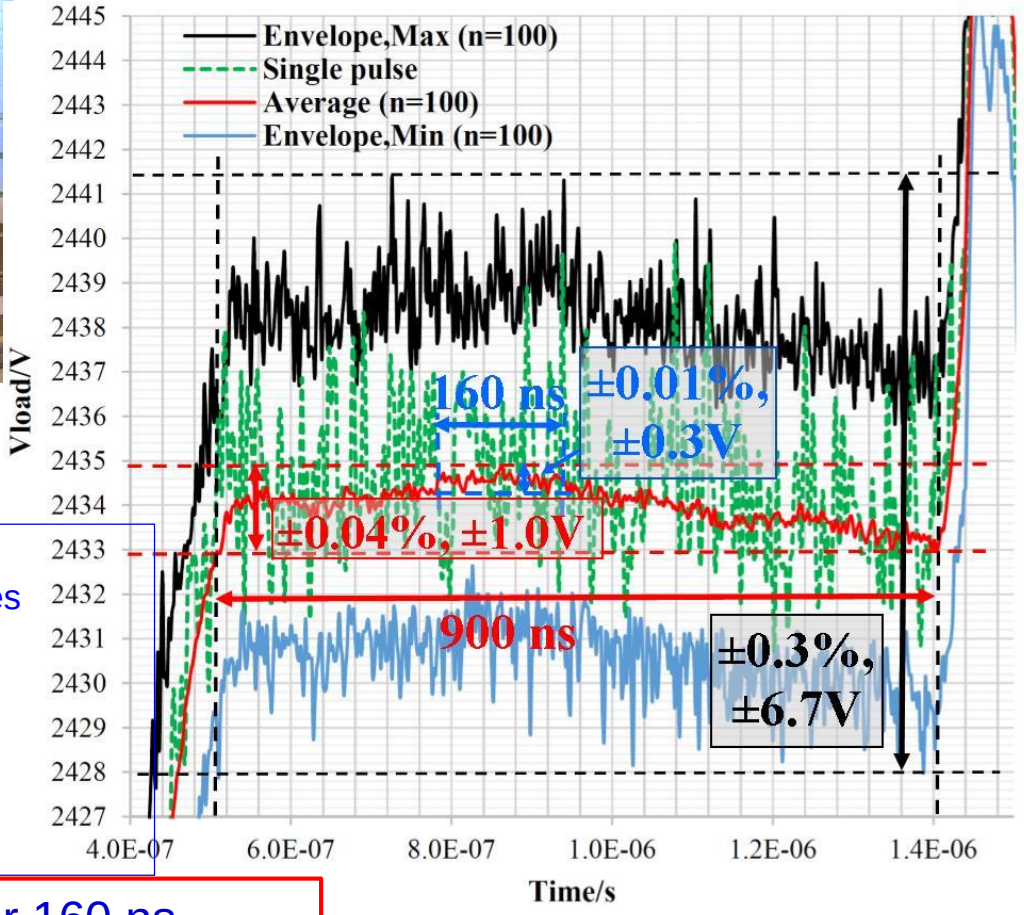
First 5 layers of the 12.5 kV inductive adder assembled at CERN

Initial measurements on prototype 3



New 3.5 kV, 5-layer, full-scale inductive adder prototype

2nd inductive adder with an analogue modulation layer only (in series with the 3.5 kV inductive adder)

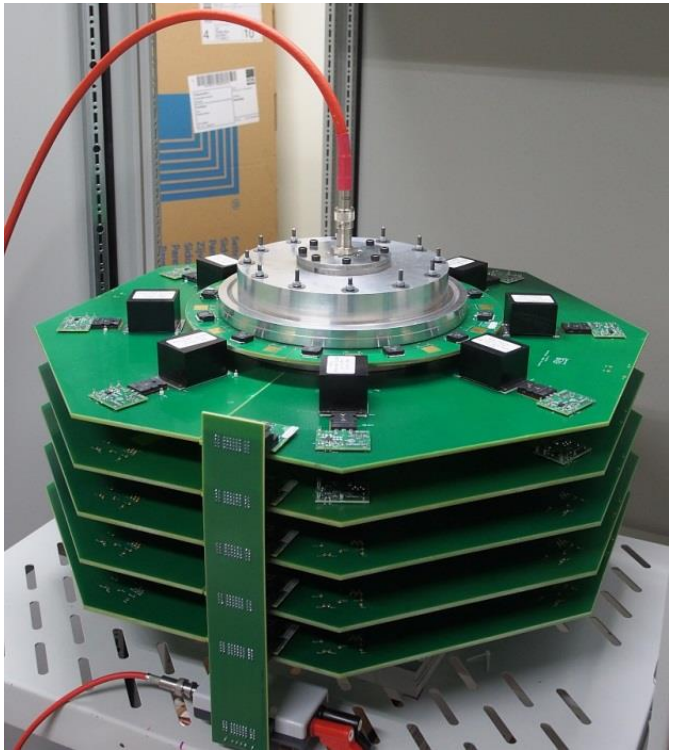


- **Setup for the measurement:**
  - 5 constant voltage layers with Finemet FT-3L cores
  - 1 Active analogue modulation layer
  - 1 branch powered per half-layer PCB
  - Capacitors (24 µF/layer) initially charged to 555 V
  - **Active compensation of droop (not ripple)**
  - **Measurements with a 16-bit (effective) oscilloscope!**

⇨ ±0.01% (±0.3 V) flat-top stability over 160 ns
⇨ ±0.04% (±0.3 V) flat-top stability over 900 ns
⇨ Flat-top repeatability ±0.3 % (±6.7) over 900 ns

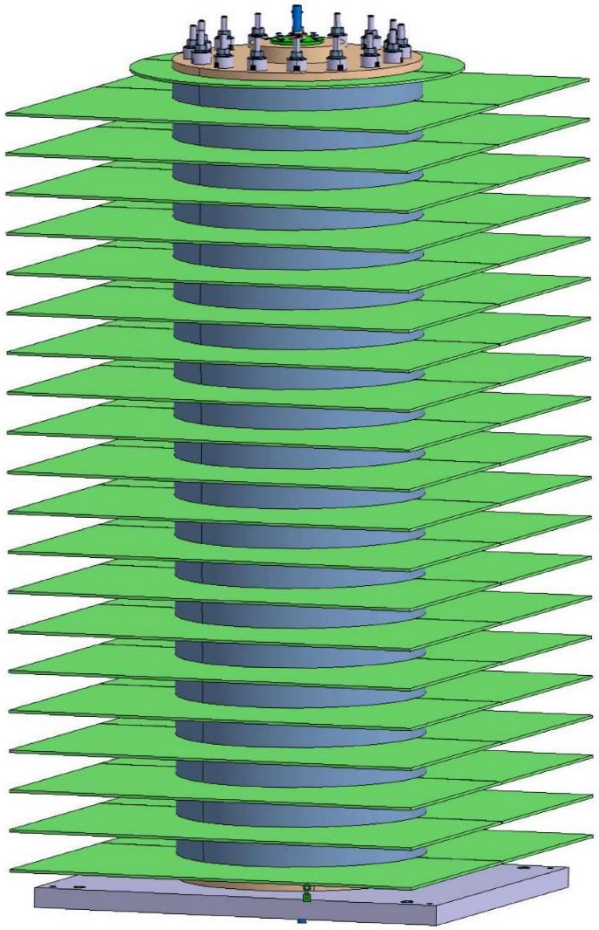
Summary

- **The pulse power modulators for CLIC DR kicker systems are very probably feasible with inductive adder technology.**
- Three 5-layer, 3.5 kV prototype inductive adders have been built and tested at CERN
- Both passive and active analogue modulation methods tested to improve the flat-top stability of the output pulses
- The best measured flat-top stability has been ±0.01 % (±0.3 V) for 160 ns and ±0.04 % (±1.0 V) for 900 ns pulse flat-top at 2.5 kV, which were reached by applying active droop compensation.
- The design of the first full-size, 20-layer, 12.5 kV, 250 A, CLIC DR kicker prototype inductive adder has been finished. The main components and mechanical parts have been received and PCBs are being manufactured.
- The initial measurements have commenced with full-size inductive adder cells (5-layer, 3.5 kV prototype)



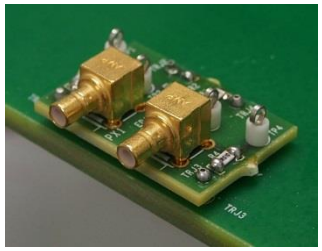
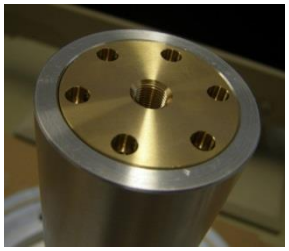
Future Work

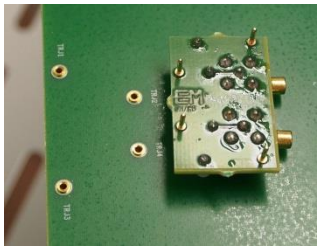
- Assembly and testing of the first 20-layer, 12.5 kV, 250 A, prototype inductive adder (by the end of year 2016).
- Improvement of flat-top stability to ±0.02 % for 900 ns:
  - Active analogue modulation layer with droop and ripple compensation (an RF amplifier between the RF MOSFET and a signal generator).
- Improvement of flat-top repeatabilty to ±0.01 % for 900 ns:
  - Identifying of sources for asynchronous ripple components of pulses.
  - Improved filtering of noise from power supplies.
  - Decreased dynamic range of measurements to improve resolution (”pulse cancelling” technique)
- Measurements of two 12.5 kV inductive adders with a stripline kicker installed in a beamline in an accelerator test facility.
- Other possible applications for inductive adder technology at CERN:
  - FCC kicker systems (20 kV, 3.6 kA, 2.5 µs)
  - PS KFA kicker system (40 kV, 1.5 kA, 2.6 µs)

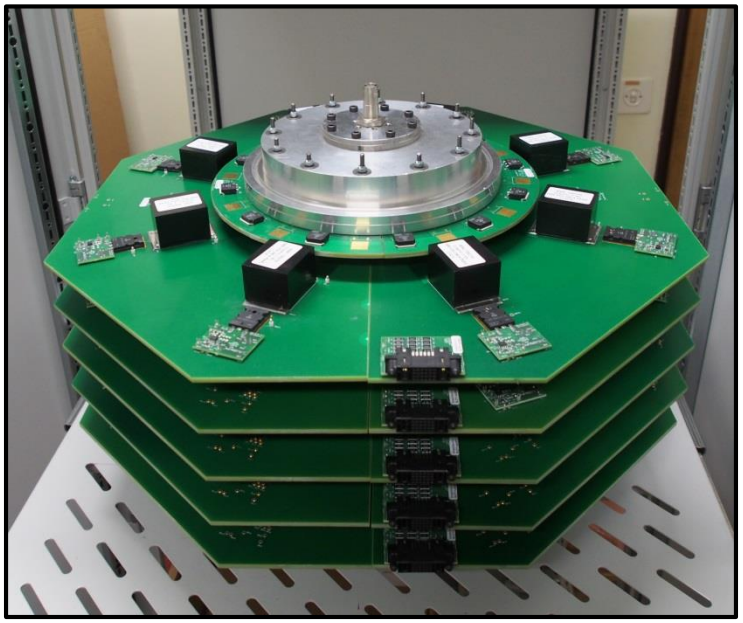


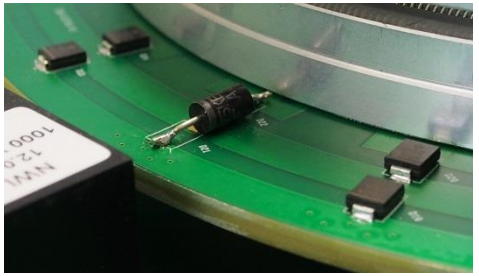
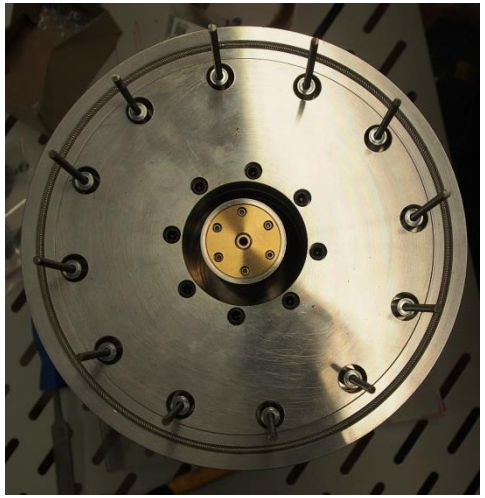
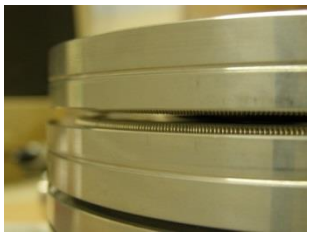
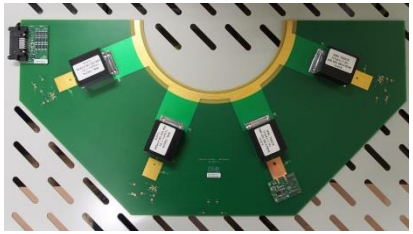
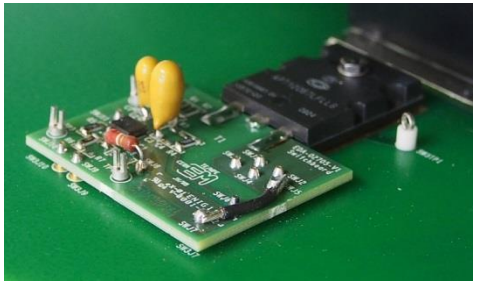
3D model of a 20-layer inductive adder at CERN (Courtesy of P. Faure)

Questions & Comments?





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3. Holma J., ”A Pulse Power Modulator with Extremely Flat-top Output Pulses for the Compact Linear Collider at CERN”, Ph.D. Thesis, Aalto University, School of Electrical Engineering, Helsinki, Finland, 2015.

4. Holma J., Barnes M.J.: ” The Prototype Inductive Adder With Droop Compensation for the CLIC Kicker Systems.”, IEEE Trans. Plasma Sci., Vol. 42, No. 10, Oct. 2014.

5. Holma J., Barnes M.J., Belver-Aguilar C.: ”Measurements on a Prototype Inductive Adders with Ultra-flat-top Output Pulses for CLIC Kicker Systems”, Proc. IPAC’14, Dresden, Germany, June 15-20, 2014.

6. Holma J., Barnes M.J.: ”Initial Measurements on a Prototype Inductive Adder for the CLIC Kicker Systems”, Proc. of PPC’13, San Francisco, CA, USA, June 16-21, 2013.

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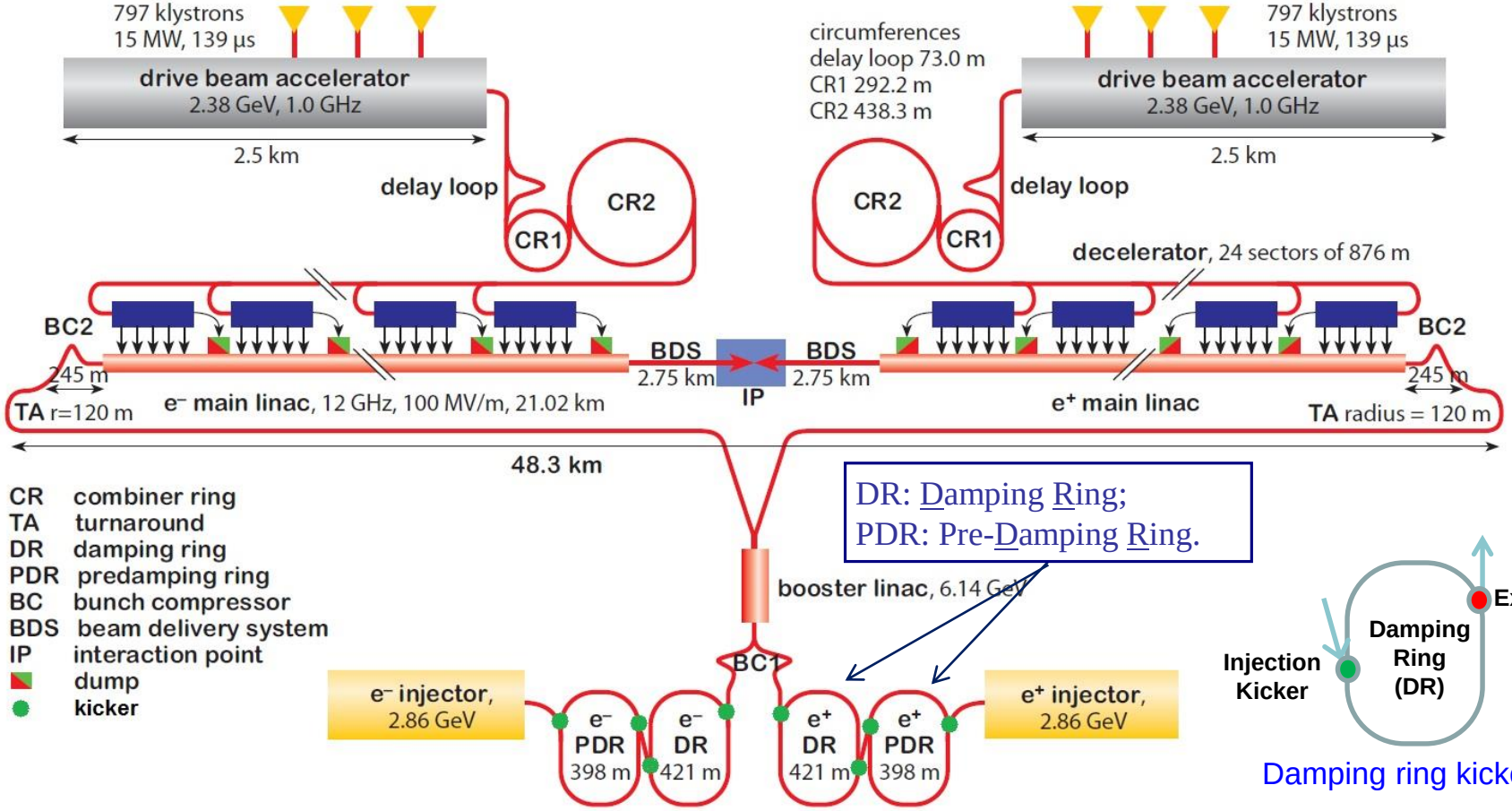
9. Holma J., Barnes M.J.: “Evaluation of Components for the High Precision Inductive Adder for the CLIC Damping Rings”, Proc. of IPAC 2012, New Orleans, USA, May 20-26, 2012.

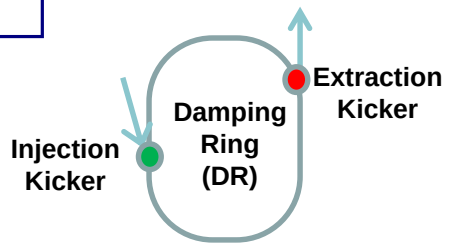
10. Holma J., Barnes M.J.: “Pulse Power Modulator Development for the CLIC Damping Ring Kickers”, CLIC-Note-938, CERN, Geneva, Switzerland, April 27, 2012.

Spare Slides

CLIC General Layout



DR: Damping Ring;
PDR: Pre-Damping Ring.



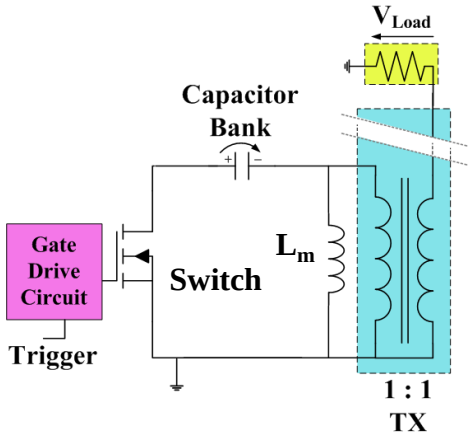
Damping ring kickers

PDR & DR Kickers (●):

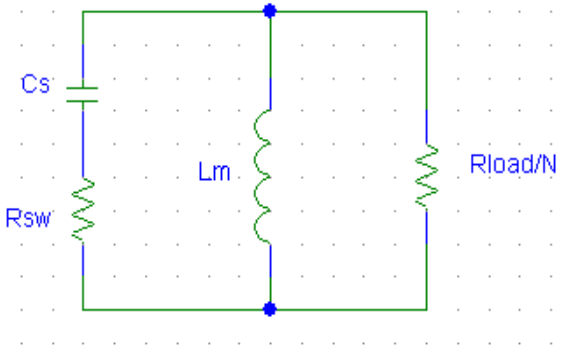
- One injection and extraction system per ring and per beam (8 systems);
- Damping rings reduce beam emittance; hence kickers must be high stability (low ripple);
- Low beam coupling impedance and good field homogeneity are required (talk by C. Belver-Aguilar).

Contributors to the Droop of the Output Waveform of an Inductive Adder

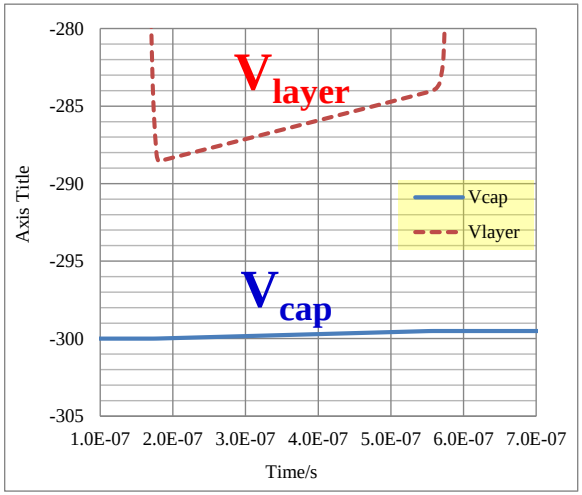
- The droop of the output pulse of an inductive adder is caused by:
  - The small voltage droop of the storage capacitor (C_s) as it supplies charge during the pulse
  - The resistive losses in the primary switch and in the primary circuit (R_{sw}), which depends on the current through the magnetizing inductance (L_m).
- **Only the voltage droop of the capacitors can be compensated by adding more capacitance per layer!**
- **The only methods to effectively decrease the droop, caused by a combination of resistive losses and magnetizing inductance of the transformer core, is to apply either passive or active analogue modulation (or both) for the output pulse.**
- **These methods are necessary to reach very low droop (<< 1 %).**



Simplified schematic of a constant voltage layer of an inductive adder



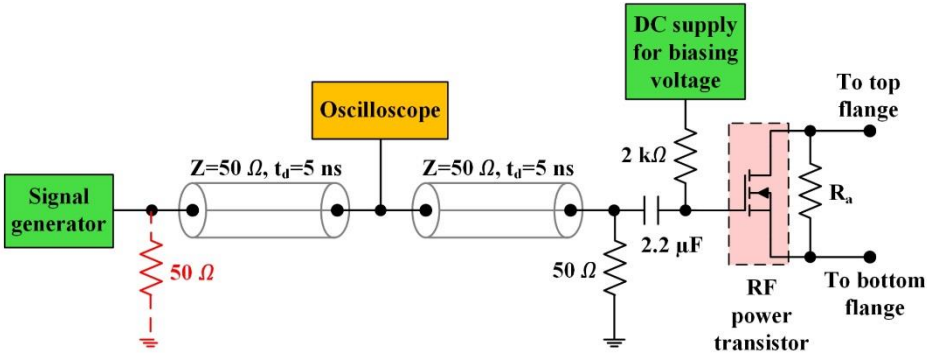
Simplified model of a layer of an inductive adder during the pulse

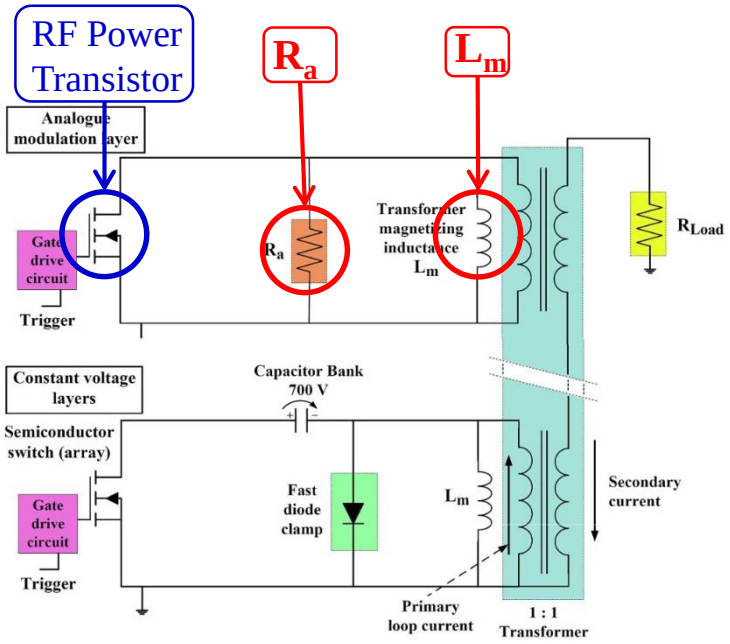


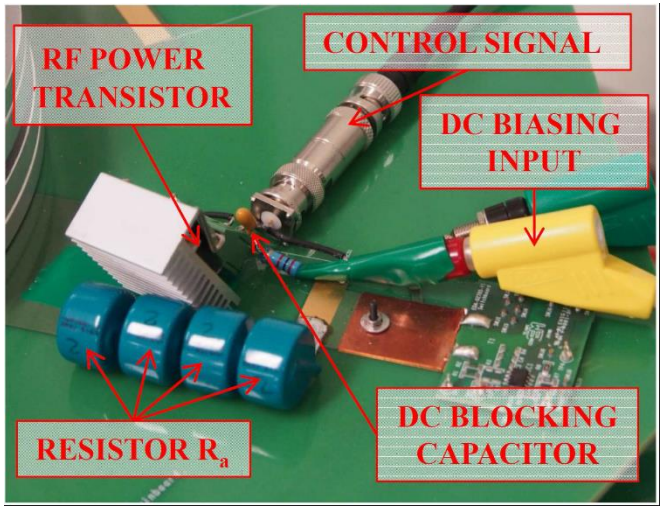
Capacitor voltage V_{cap} and voltage of a layer V_{layer} during a pulse. C_s = 24 uF, Rsw = 0.34 Ω and R_{load}/N = 10 Ω.

Measurements: Passive Compensation of Droop and Active Compensation of Droop and Ripple

- **Setup for the measurement:**
  - The prototype adder with 4 constant voltage layers and an analogue modulation layer
  - 1 branch powered per half-layer PCB, 2 branches per layer
  - Capacitors (24 µF/layer) charged initially to 350...553 V.
  - Passive or active analogue modulation applied







Schematic and layout of the active analogue modulation layer

Measurements: 3.5 kV Output Pulse - No Modulation

- **Setup for the measurement:**
  - The prototype adder with 5 layers
  - 1 branch powered per half-layer PCB, 2 branches per layer
  - Capacitors (24 µF/layer) charged initially to 750 V
  - 50 Ω, 18 kV load by Diconex
  - No modulation applied.
- **Output pulse parameters**
  - Output voltage: 3.5 kV
  - Rise time (0.1...99.99 %) 160 ns
  - Droop: ~3.4 % (120 V) for 170 ns flat-top duration
  - Small intra-pulse voltage (~10 V).

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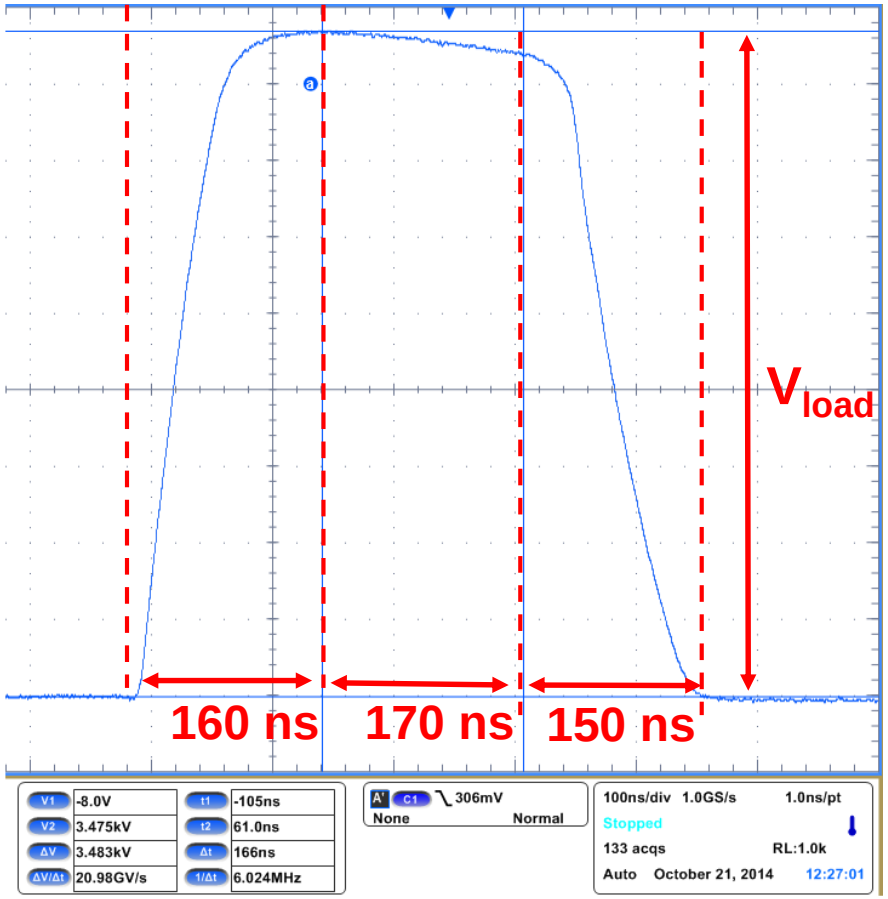
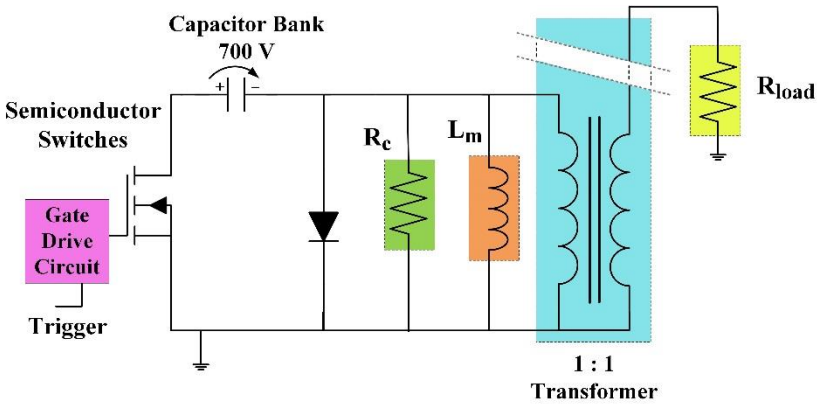
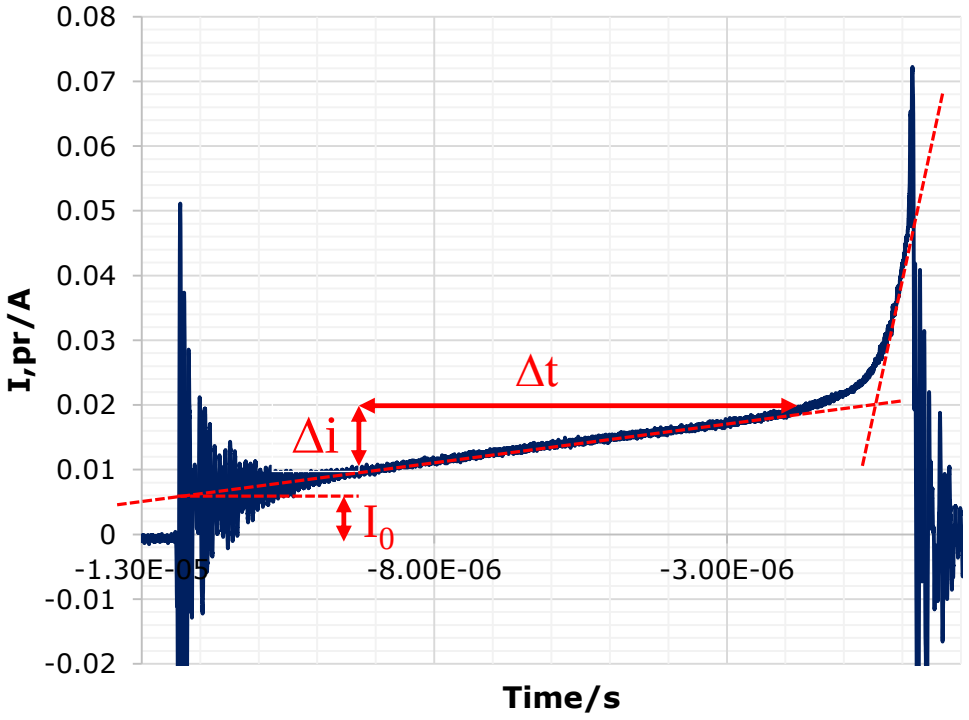
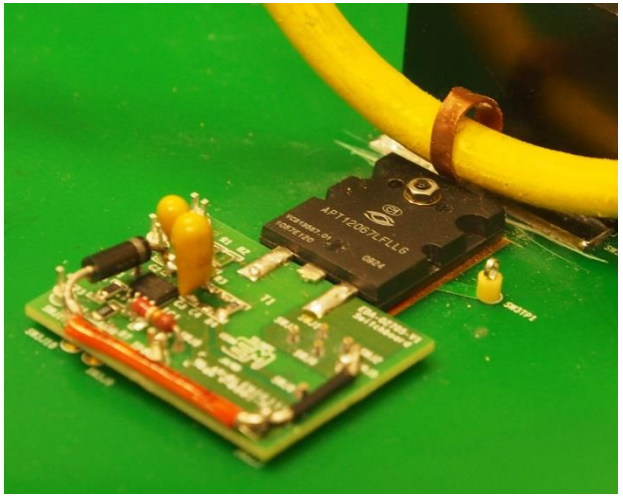


Evaluation of Magnetic Core Material for 12.5 kV Prototypes

- Core materials were evaluated by measuring primary current (***I,pr***) of a single layer with a Rogowski coil current transducer.
- Numerical estimates for R_c and L_m:
  - $R_c \approx V_{Rc} / I_0$
  - $L_m \approx (V_{Lm} \times \Delta t) / \Delta i_{Lm}$



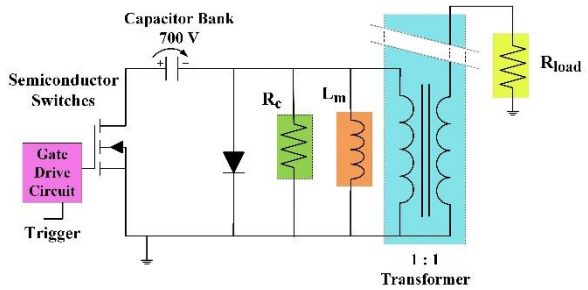


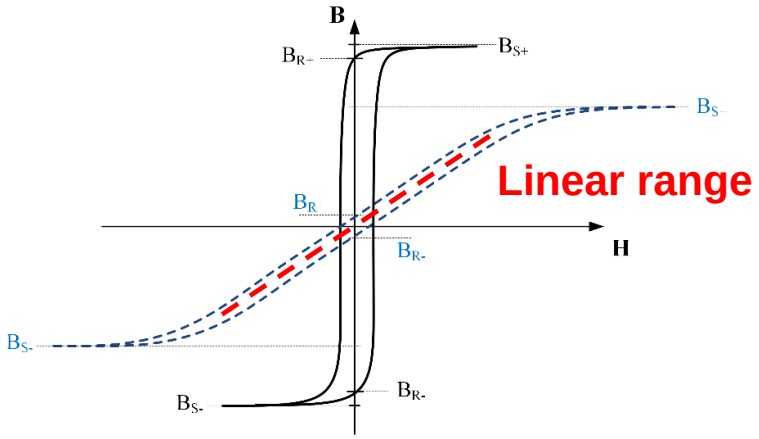


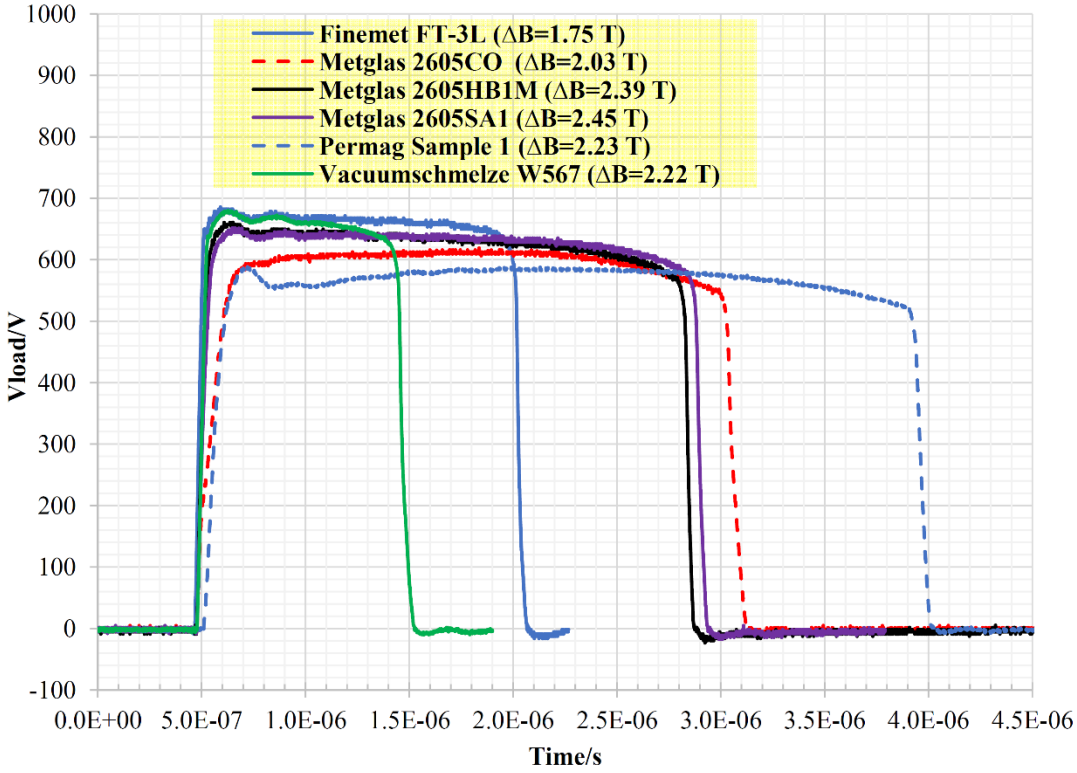
Measurement set-up for magnetizing current

Evaluation of Magnetic Core Material for 12.5 kV Prototypes – with Biasing

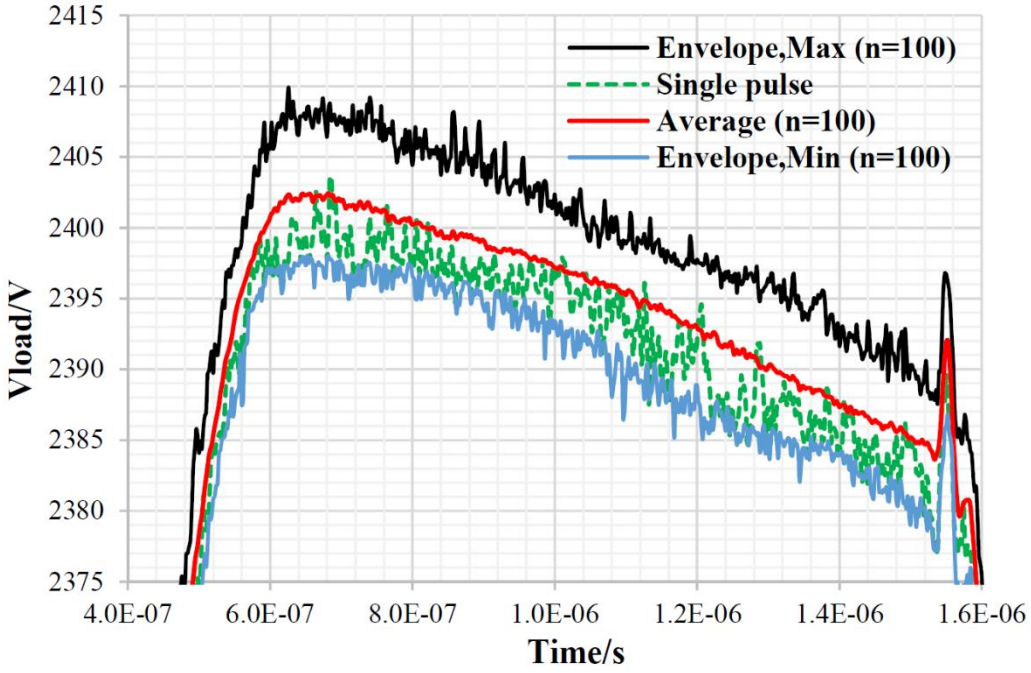
- Set-up for measurement:
  - Output voltage of an inductive adder with single layer powered (700 V)
  - Biasing (8 A, DC) applied, to use most of the flux swing range
- Biasing circuit (large inductor) causes ripple for the pulse flat-top and off-time voltage, which is not acceptable for CLIC DR kicker system.







Initial measurements on prototype 3



- **Setup for the measurement:**
  - 5 constant voltage layers with Finemet FT-3L cores
  - 1 branch powered per half-layer PCB
  - Capacitors (24 µF/layer) initially charged to 555 V
  - **No compensation**
  - **Measurements with a 16-bit (effective) oscilloscope!**

⇨ Flat-top repeatability ±0.3 % (±7.0) over 900 ns