Power Matters.™

SiC MOSFET & Diode Roadmap

September 12, 2016
DPG-PDM

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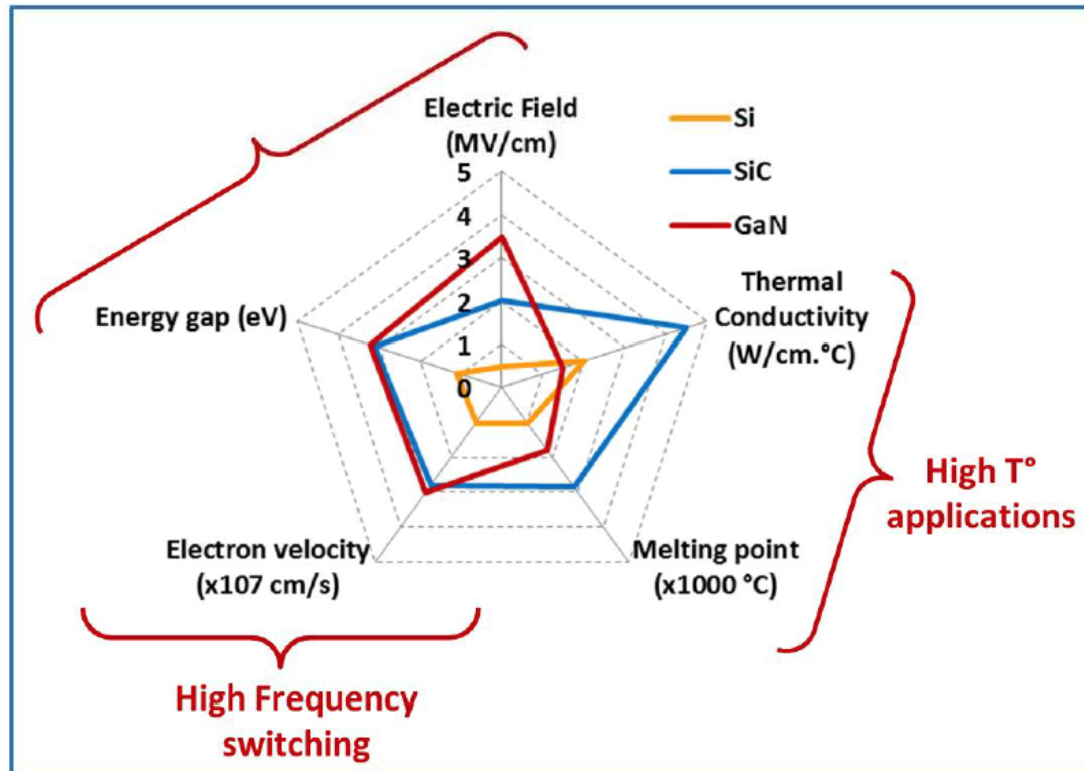
SiC Capabilities Vs. Silicon

SEMICONDUCTOR DEVICES: PLENTY OF OPPORTUNITIES FOR WIDE BANDGAP

Figure-of-merit

Base upon intrinsic properties, Wide BandGap capabilities are much more better than Silicon

- SiC will stay the preferred choice for high T° application
- GaN could possibly reach high-voltage values but thus will require bulk-GaN as the substrate.
- Silicon cannot compete at the high-frequency range



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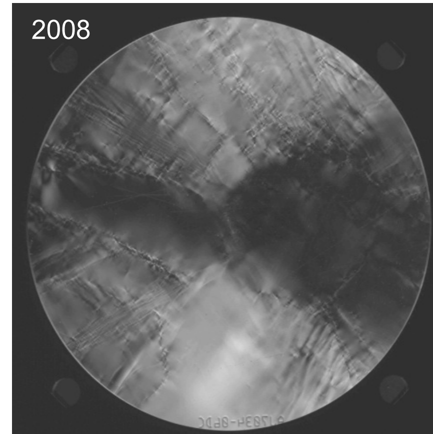
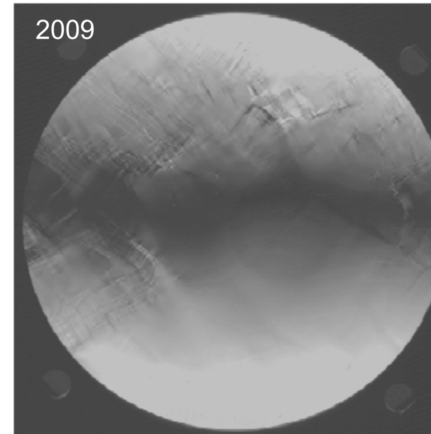
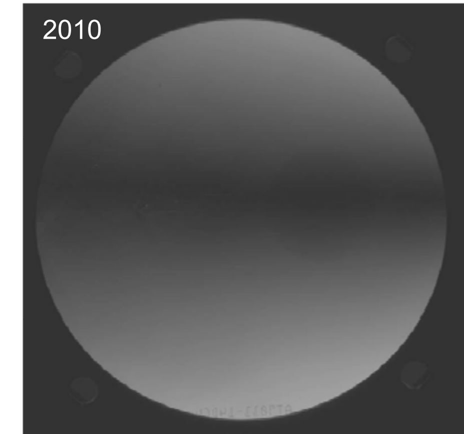
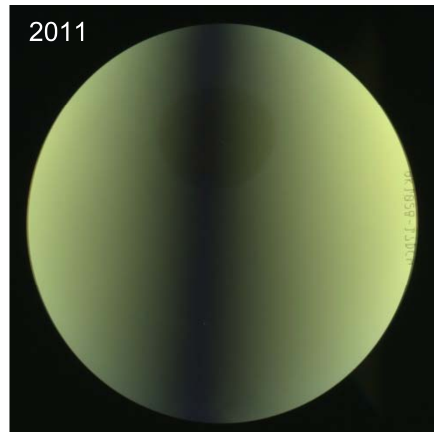
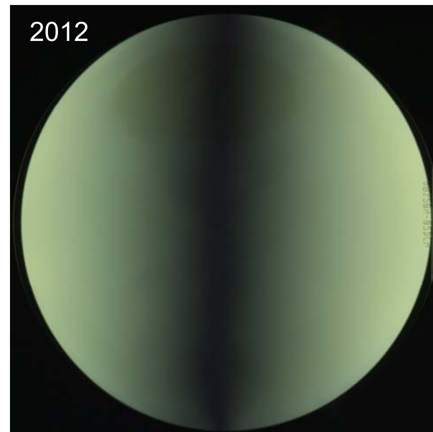
SiC Epitaxial Wafer
Cross-Polarization History

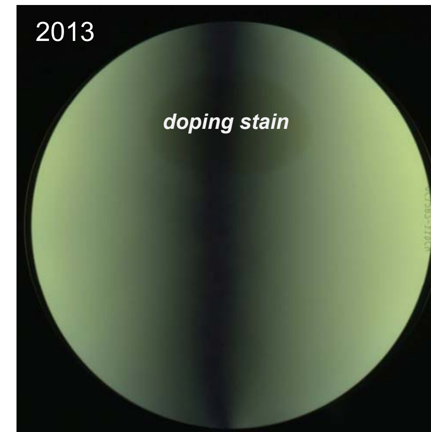


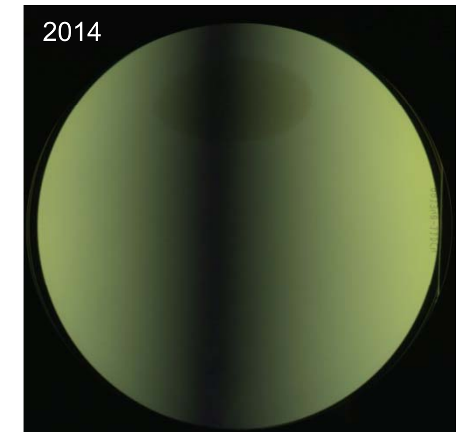












Birefringence induced by lattice strain. A perfect crystal will produce a uniform appearance when viewed between crossed polarizers, as the polarized light rotation will be the same everywhere. Lattice strain induced by lattice defects, polytype inclusions, compositional in-homogeneities, etc. can all result in regions that induce locally different rotations of the polarized light. The local variations in light rotation are easily imaged with this technique, providing a picture of crystal quality.

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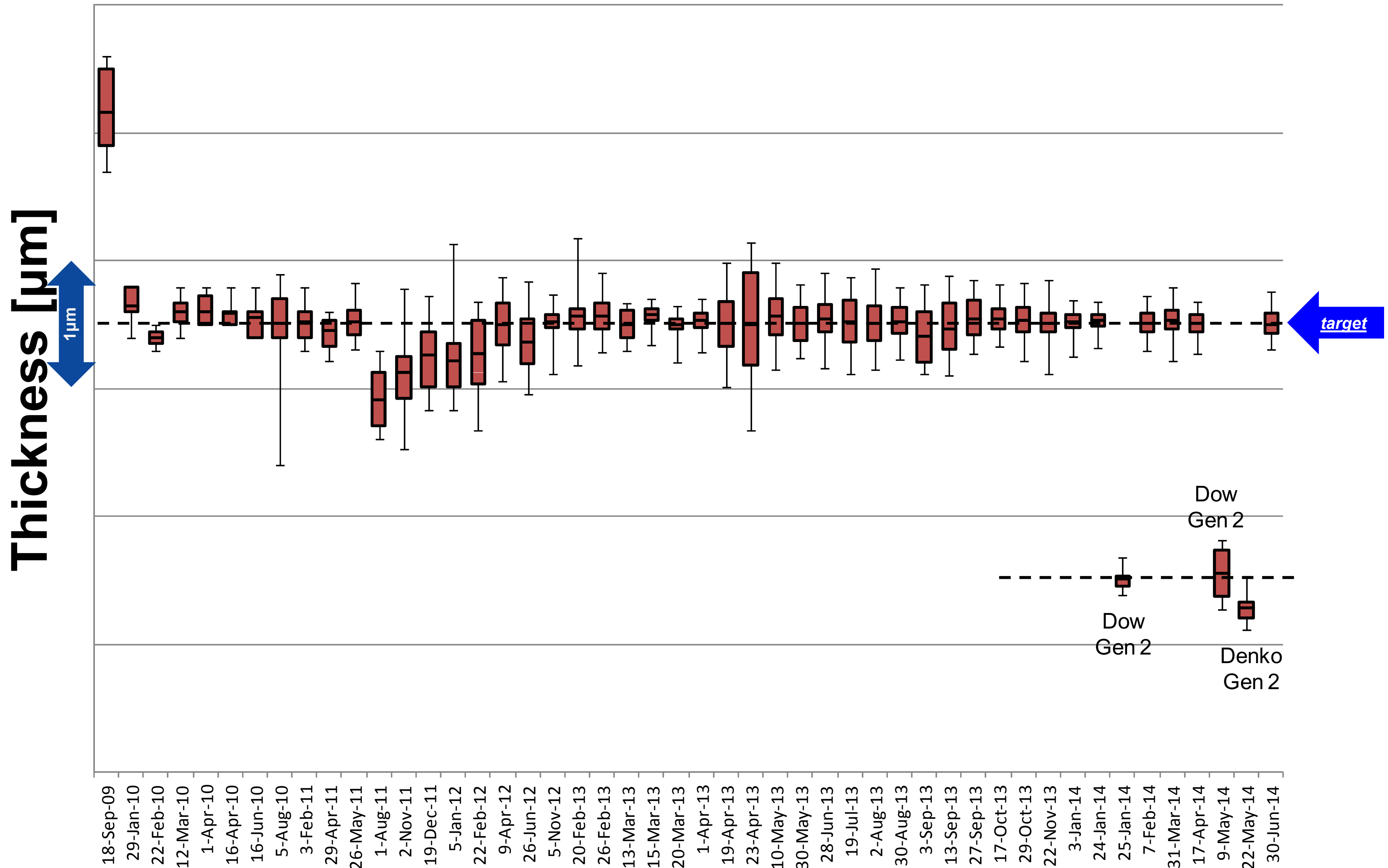
Epitaxial Layer Thickness



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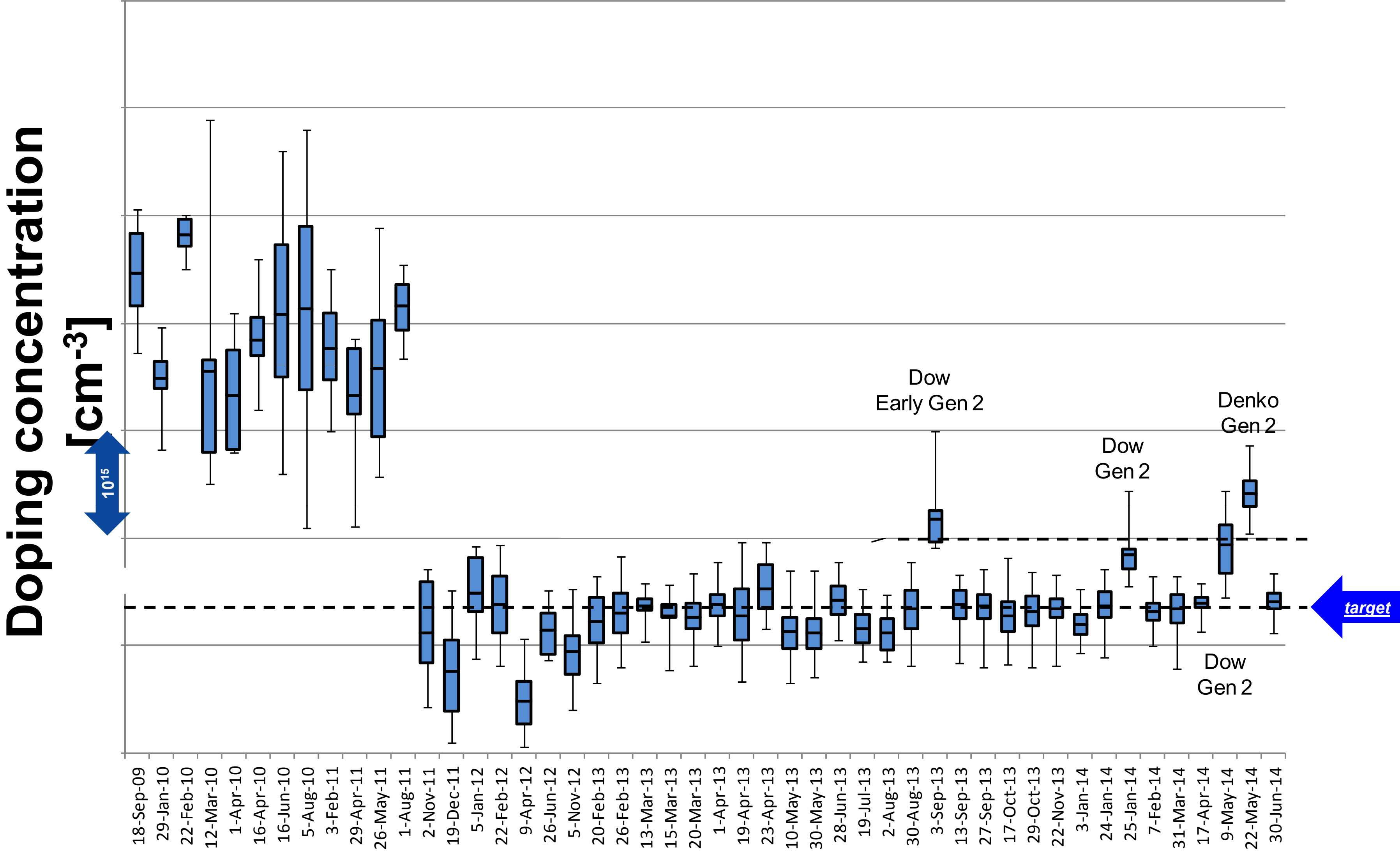
Epitaxial Layer Doping



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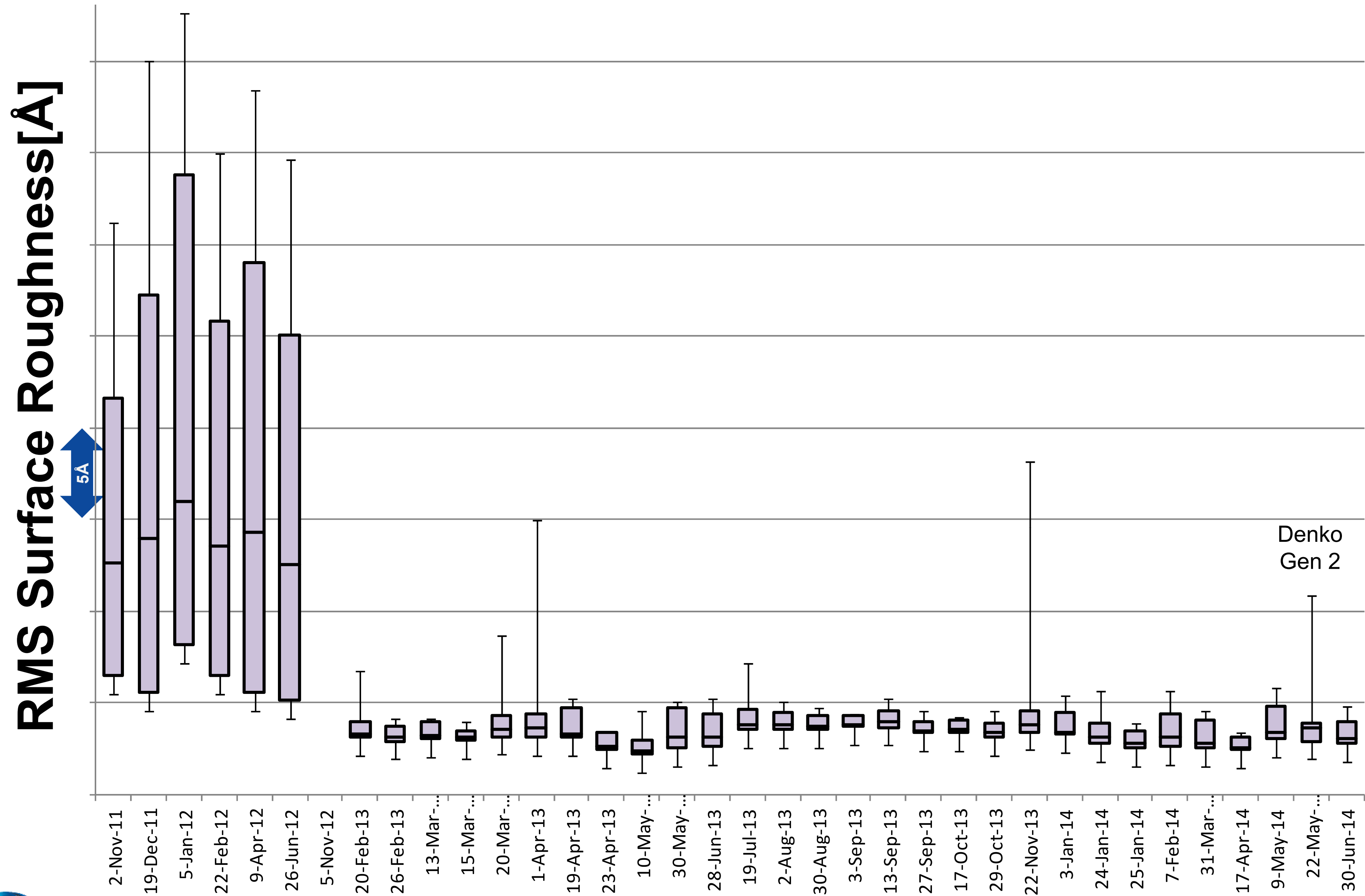
Epitaxial Layer Surface Roughness



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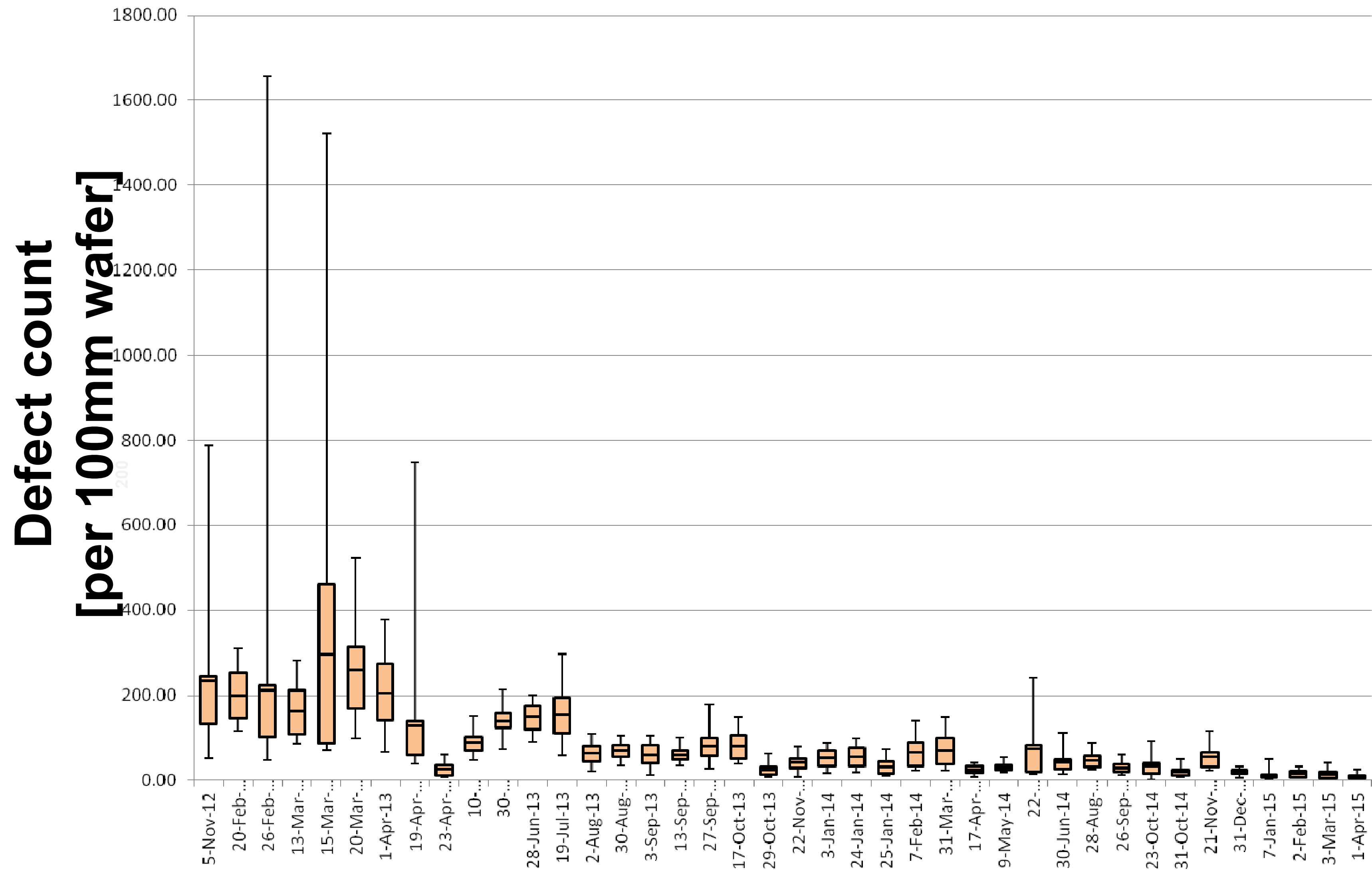
Epitaxial Layer Defect Count



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Special Processing
Contrast to Silicon Technology

- Dopant introduction by implant at elevated temperatures
- Dopant activation, implant damage anneal at high temperatures
- No diffusion
- High temperature gate oxidation
- Above translates into all layer removal post dopant introduction for electrical activation
- Alignment is critical

E220
Production Implanter

CentroTherm CHV-100
Post Implant Annealing to 1700° C

Hi Temp Oxidation
SiC MOSFET Gate Oxidation

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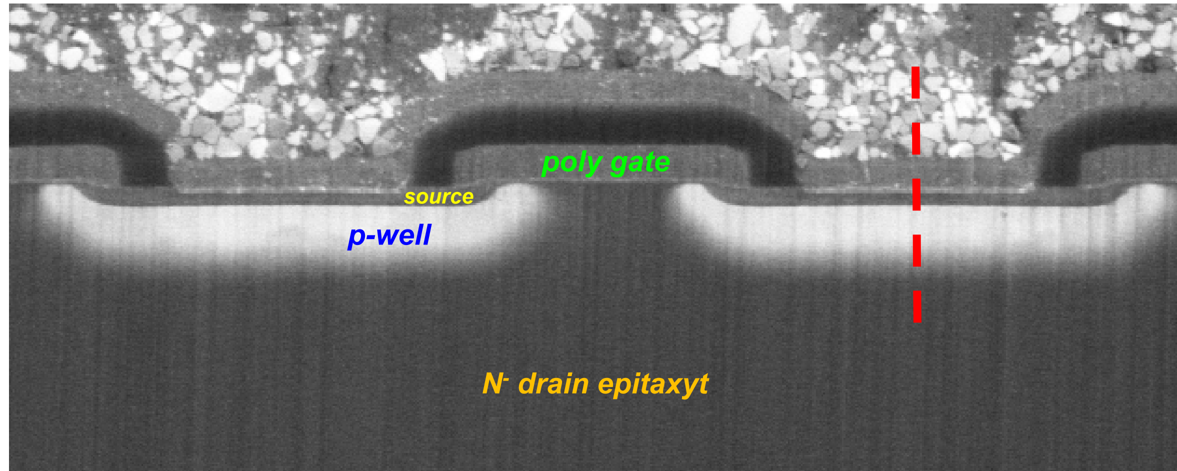
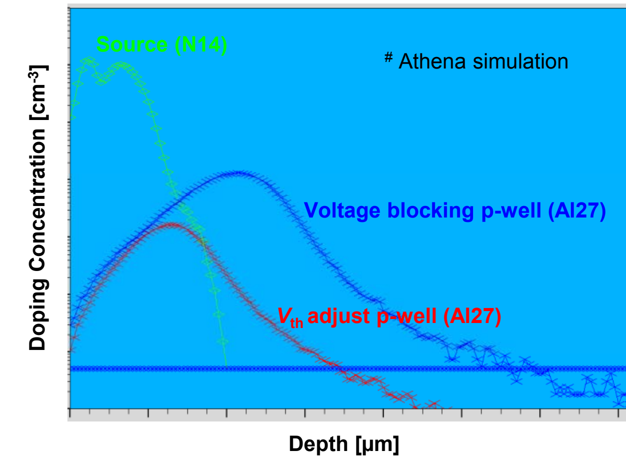
SiC MOSFET Transistor X-Section





- Simulation-based technology development to cut cycles of learning
- Flexibility of design variations for special applications
- Thick Al-Cu metallization for interconnect and bond pads
- Dual layer metal process integration for maximized packing density
- Thick final passivation for maximum reliability

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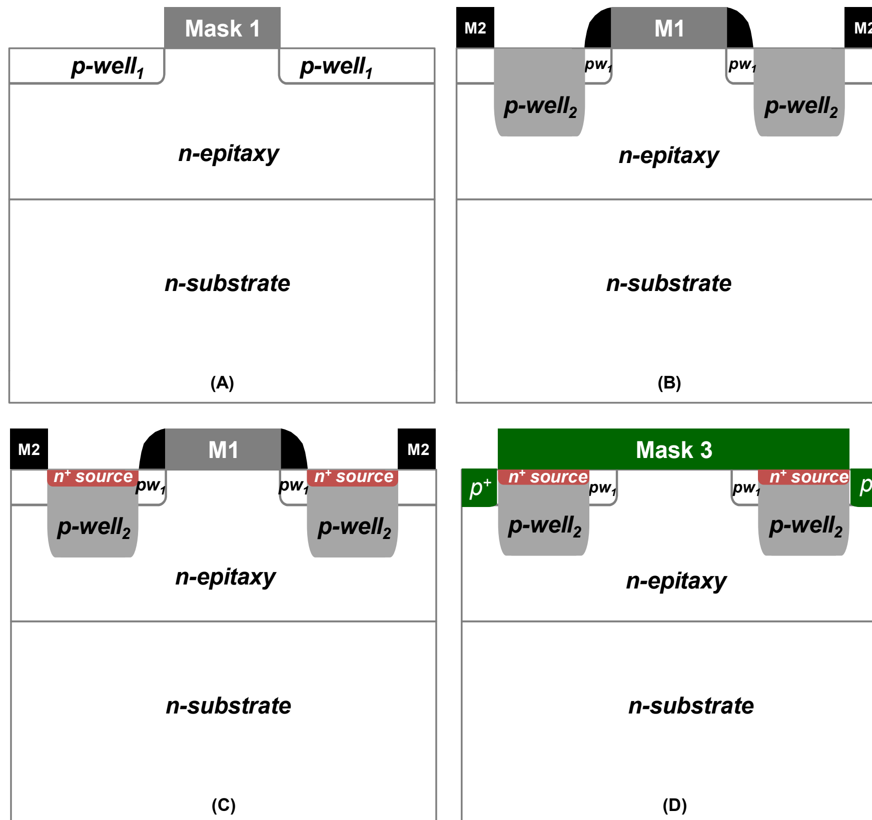
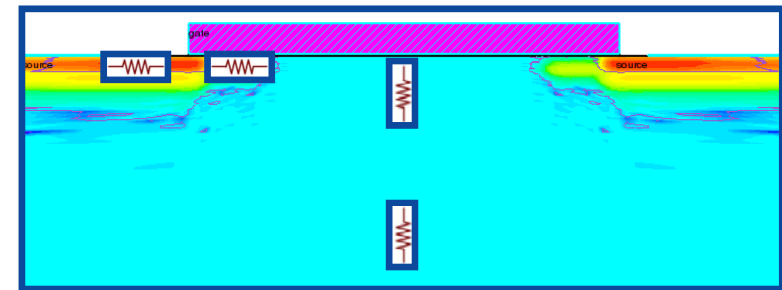
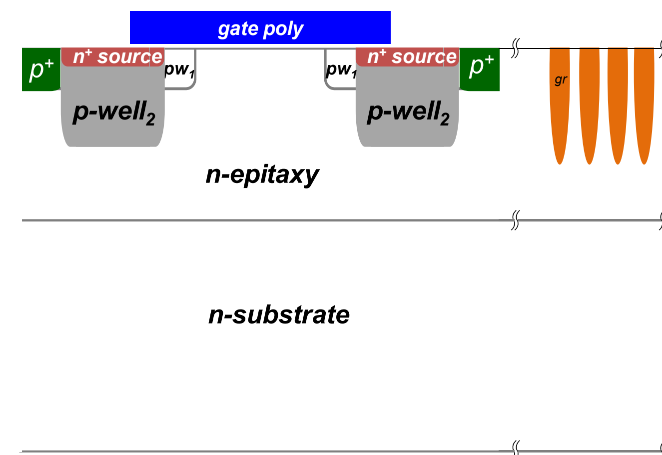
Process Integration

- P-well implants for reduced $R_{DS(ON)}$ contribution from JFET region
  - V_{th} adjustment implant
  - Voltage blocking implant
- Balance between guard-ring, p-well voltage blocking enables UIS capability
- Topology conforming backend metallization for high yield







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Microsemi SiC MOSFETs

Voltage	Current	$R_{DS(ON)}$	Part Number	Package	Samples Availability
700V New	35A	~100mΩ	APT35SM70B APT35SM70S	TO-247 D3	Mid-August
700V	70A	53mΩ	APT70SM70B APT70SM70S APT70SM70J	TO-247 D3 SOT-227	Mid-August
700V New	130A	33mΩ	APT130SM70B APT130SM70J	TO-247 SOT-227	End-July
1200V	25A	140mΩ	APT25SM120B APT25SM120S	TO-247 D3	Early-August
1200V	40A	80mΩ	APT40SM120B APT40SM120S APT40SM120J	TO-247 D3 SOT-227	Mid-June then Early-July
1200V	80A	40mΩ	APT80SM120B APT80SM120S APT80SM120J	TO-247 D3 SOT-227	Mid-June then Mid-July
1700V	5A	800mΩ	APT5SM170B APT5SM170S	TO-247 D3	Early-October

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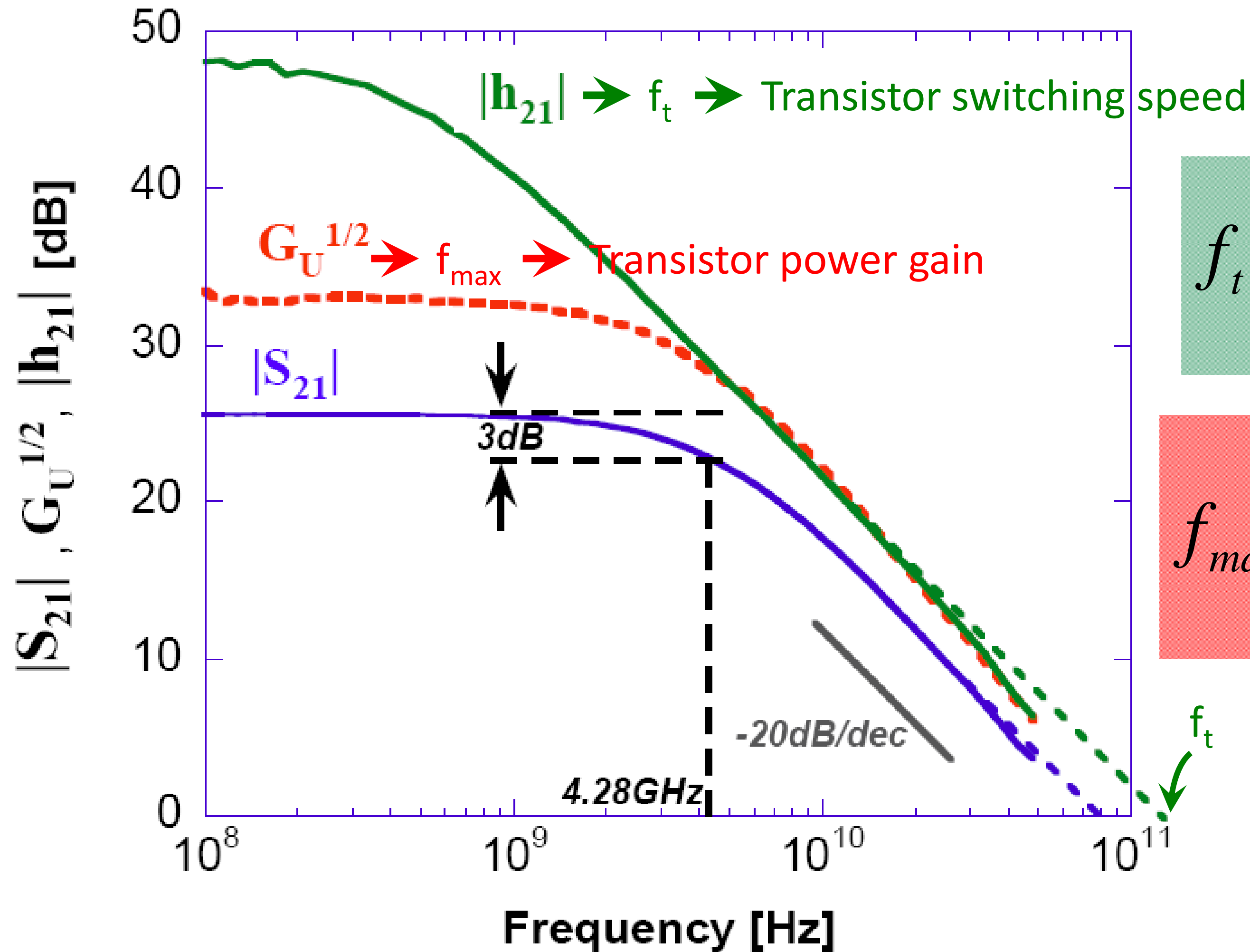
What Makes A High Speed Switch

Typical Transistor Gain Characteristics



$$f_t \propto \frac{g_m}{C_{gs} + C_{gd}}$$

$$f_{max} \propto \sqrt{\frac{f_t}{r_g \cdot C_{gd}}}$$

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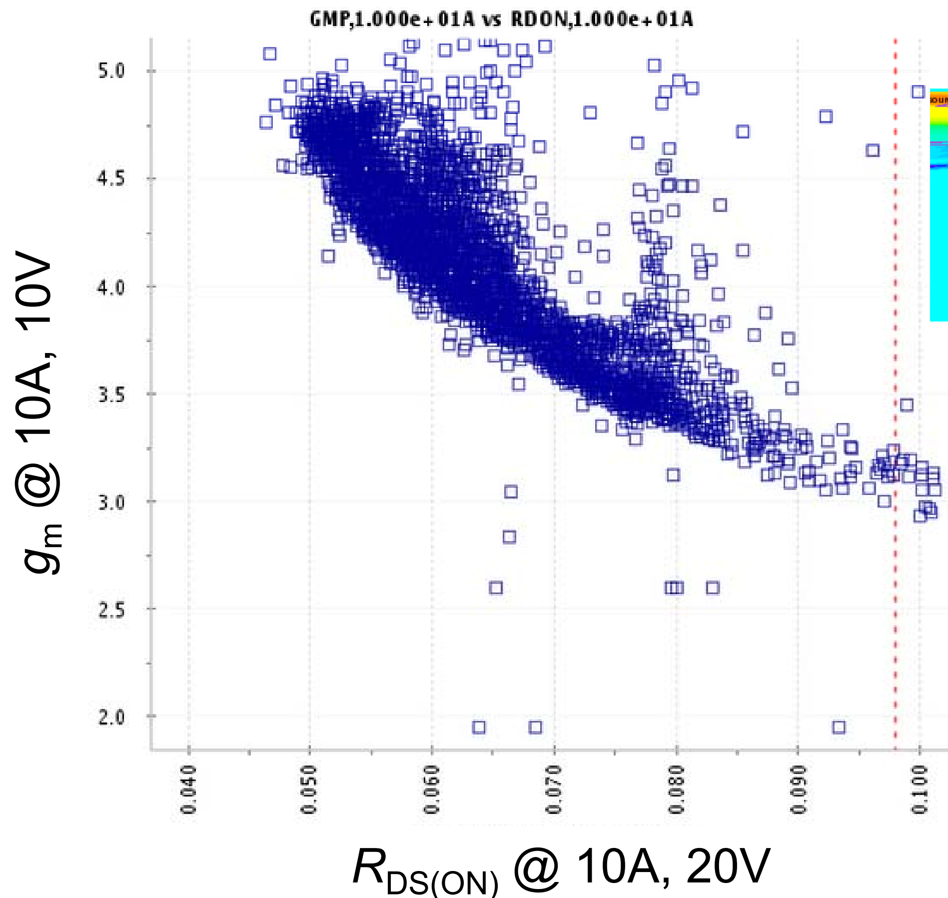
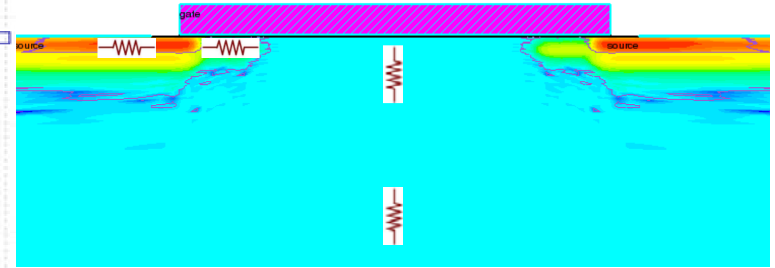
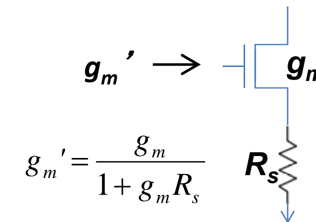
g_m Optimization



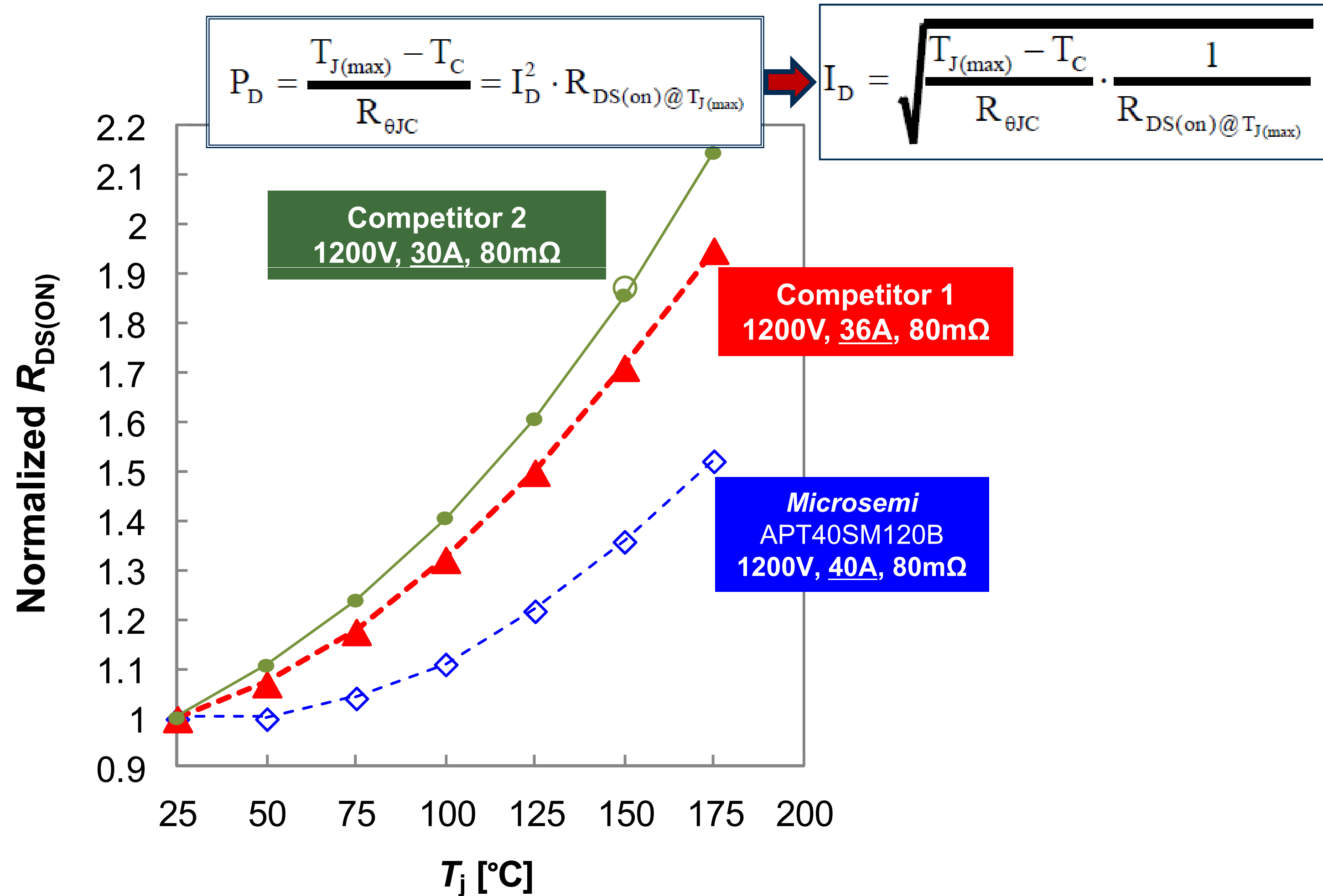




- Packing density (without increasing parasitic capacitance)
- Source resistance minimized (g_m vs. $R_{DS(ON)}$ plot)
  - Perfection of source contact formation
  - Push the limit on gate/source overlap without trading manufacturability

DC Characteristics Key to Switching Performance

Best in Class $R_{DS(ON)}$ vs. Temperature



- Lower $R_{DS(ON)}$ at temperature provides higher ceiling for continuous current rating

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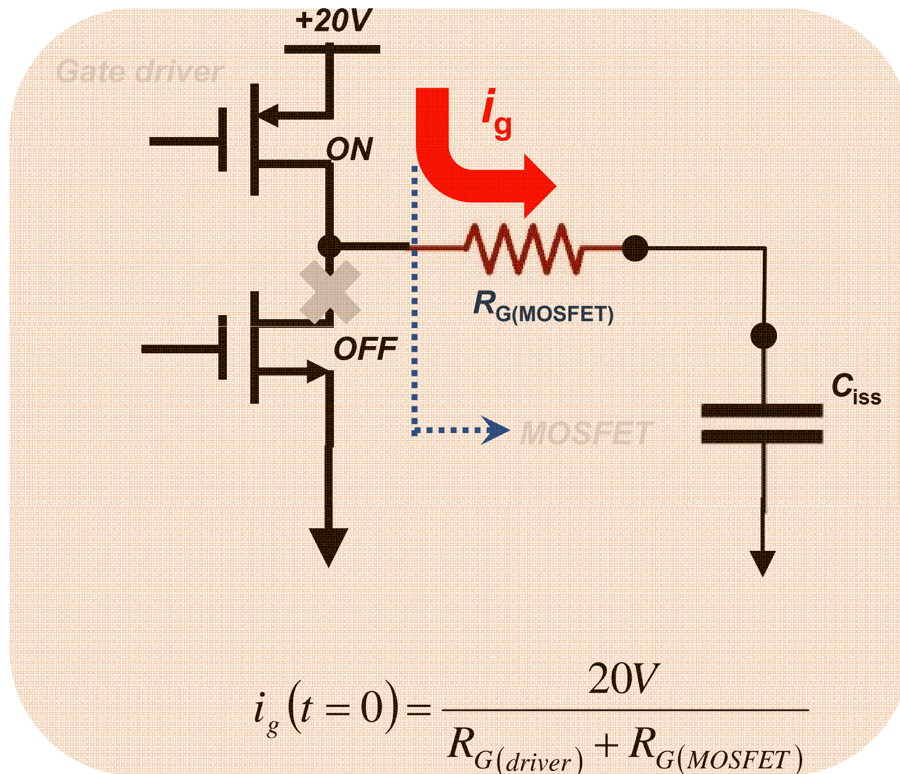
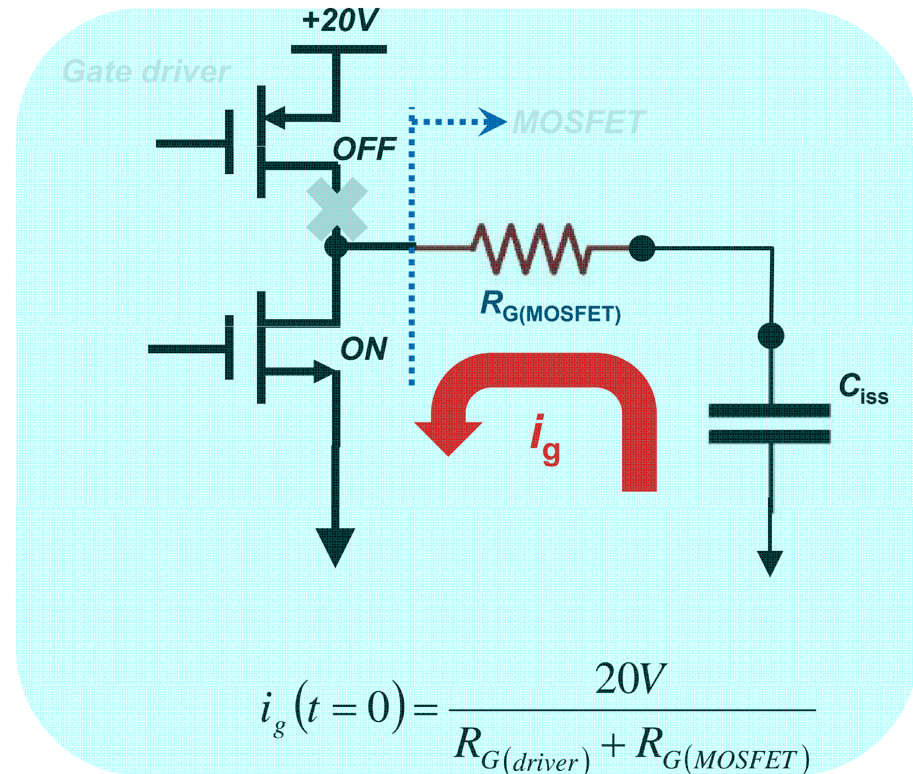
R_G & Dynamic Performance

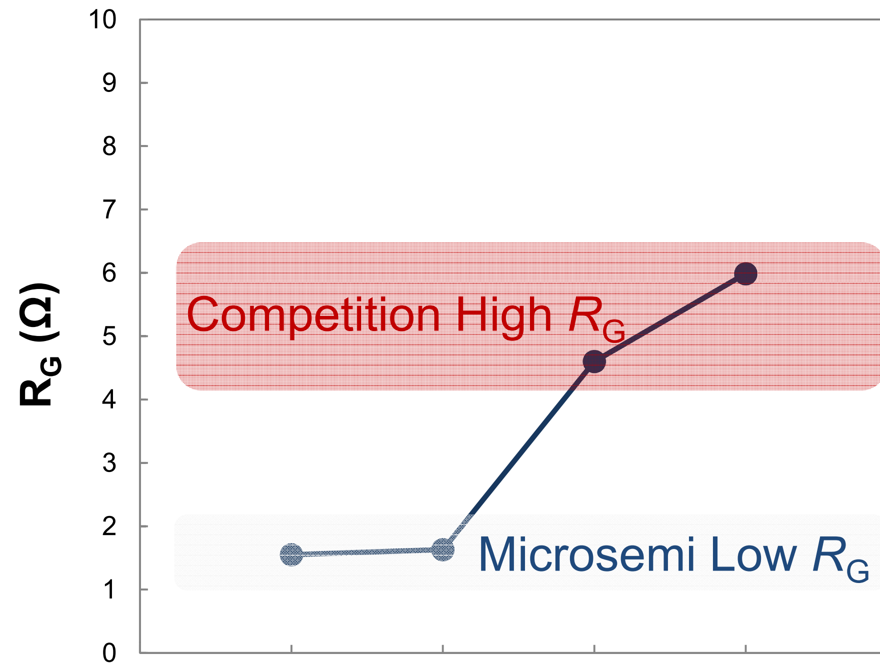




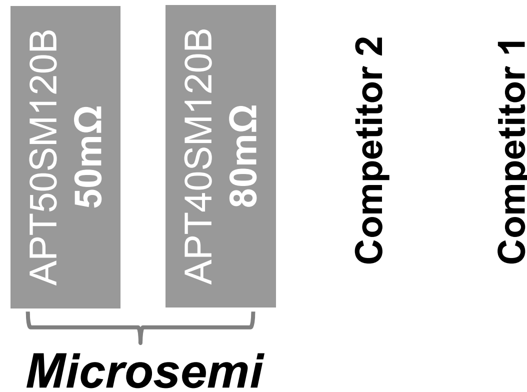
- High gate resistance limits available charging current, consequently, retards transistor switching performance

Ultra Low Gate Resistance

Minimized Switching Energy Loss & Higher Switching Frequency



Oscillation-free with minimal external R_G



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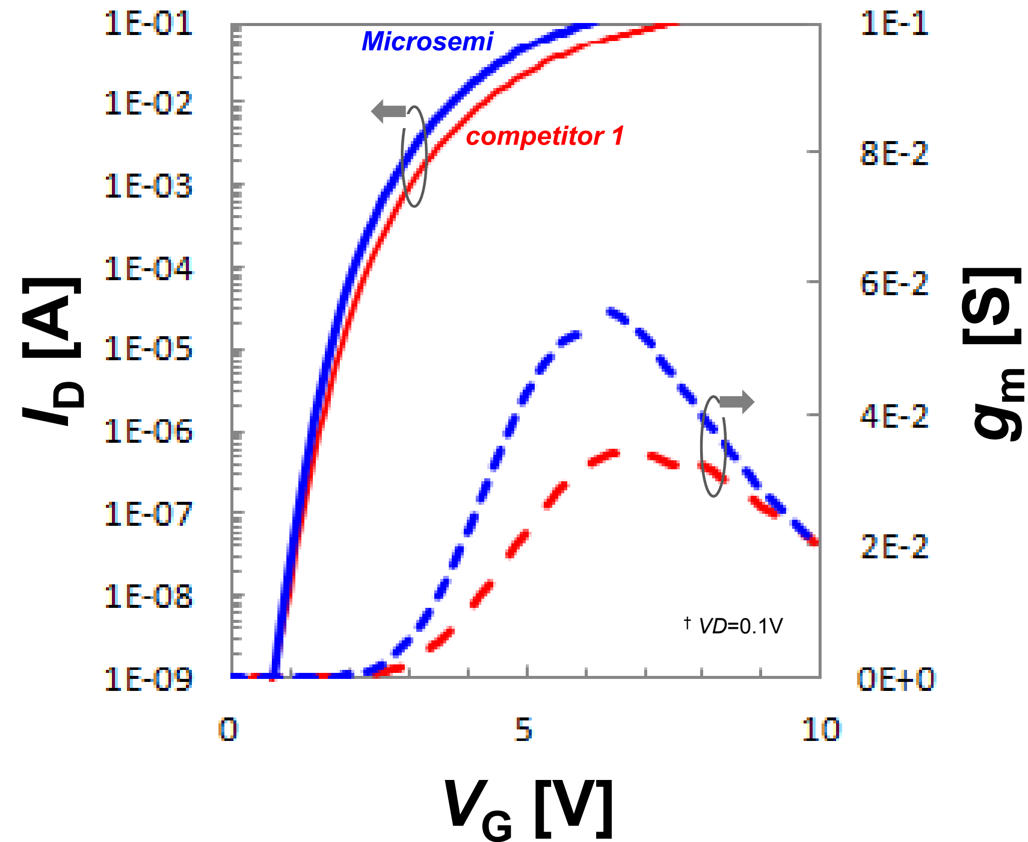
High Transconductance (g_m) Cuts t_{on}



- 2 × g_m at the start of the turn-on process

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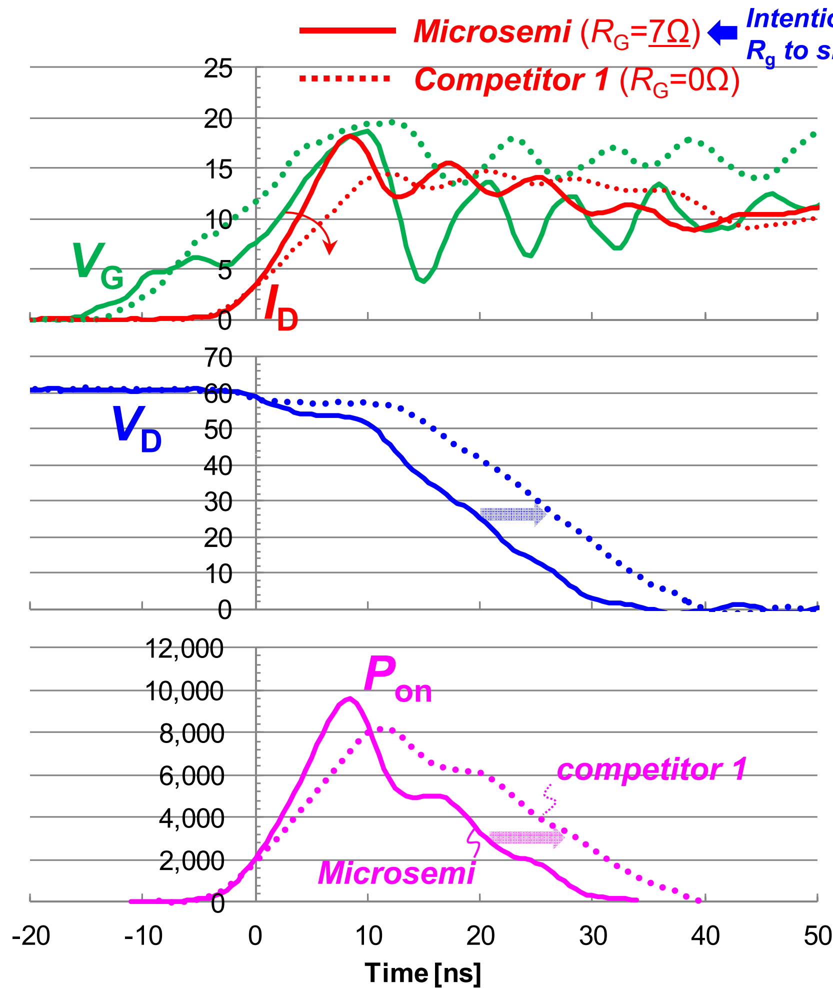
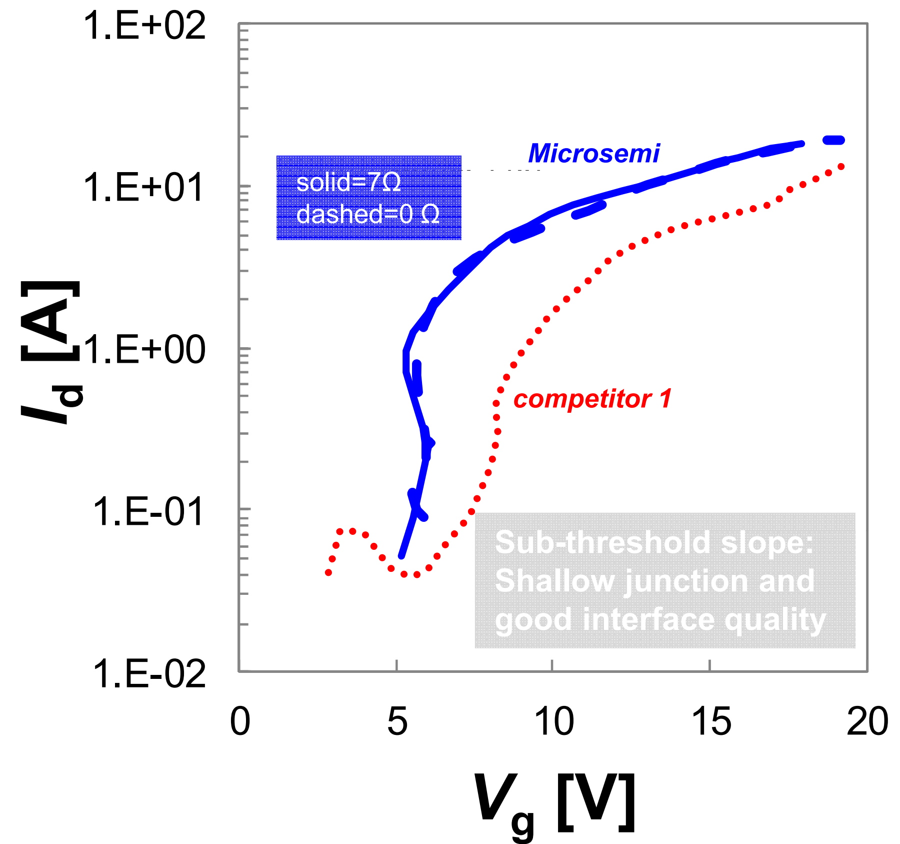
High Transconductance (g_m) Cuts t_{on}





- Superior sub-1A g_m jumps start the turn-on process

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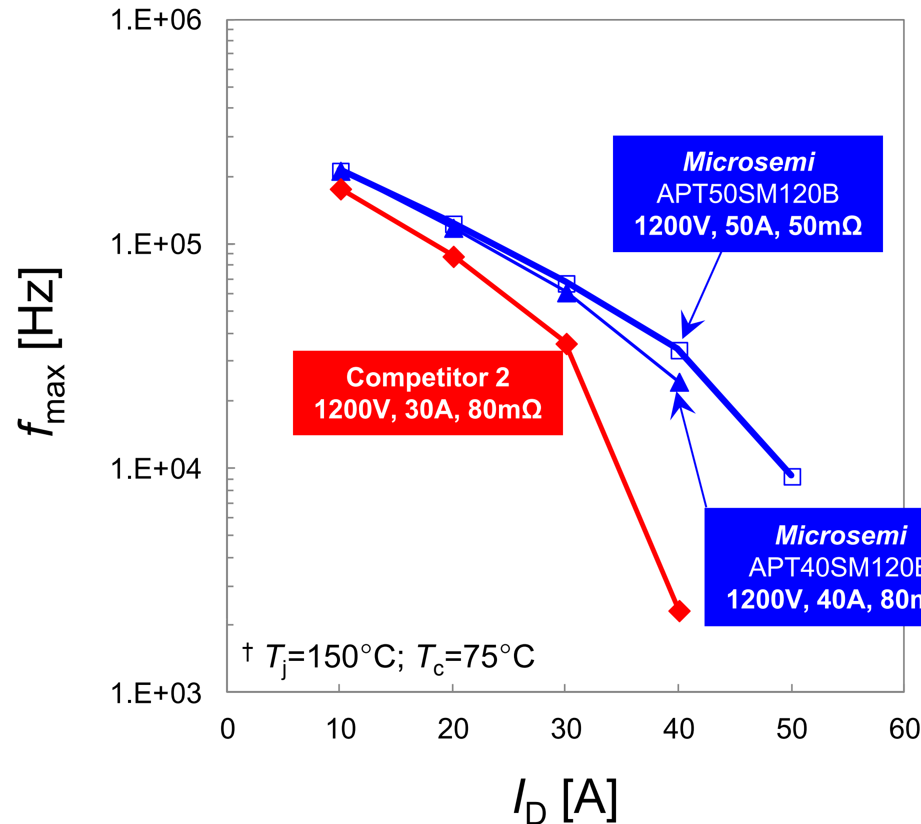
Maximum Switching Frequency, f_{max}



Limitation 1

Total switching time ≤ 5% switching period

$$f_{max1} = \frac{1}{T_s} = \frac{0.05}{t_{d(on)} + t_{d(off)} + t_r + t_f}$$

Limitation 2

Thermally limited switching frequency

$$f_{max2} = \frac{1}{t_{diss}} = \frac{\frac{T_J - T_C}{R_{\theta JC}} - P_{cond}}{E_{on2} + E_{off}}$$

$$P_{diss} = \frac{T_J - T_C}{R_{\theta JC}} = P_{cond} + \frac{E_{on2} + E_{off}}{t_{diss}}$$

Dynamic performance breakaway enablers:

- Superior $\boldsymbol{E_{on}}$ ($\boldsymbol{t_{on}}$) due to high $\boldsymbol{g_m}$, ultra low $\boldsymbol{R_G}$
- Superior $\boldsymbol{E_{off}}$ due to extremely low $\boldsymbol{R_G}$ (yet oscillation free with very low external $\boldsymbol{R_G}$)
- Low $\boldsymbol{R_{DS(ON)}}$ at high temperatures extends switching frequency and current capability

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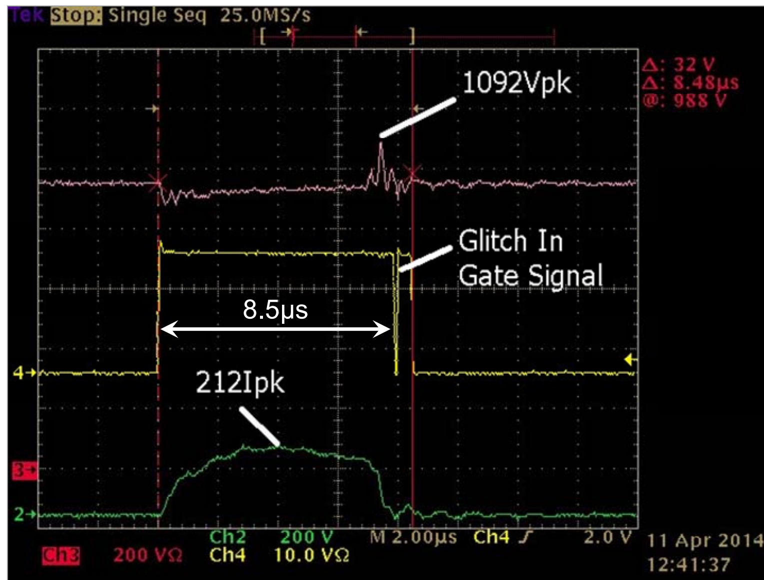
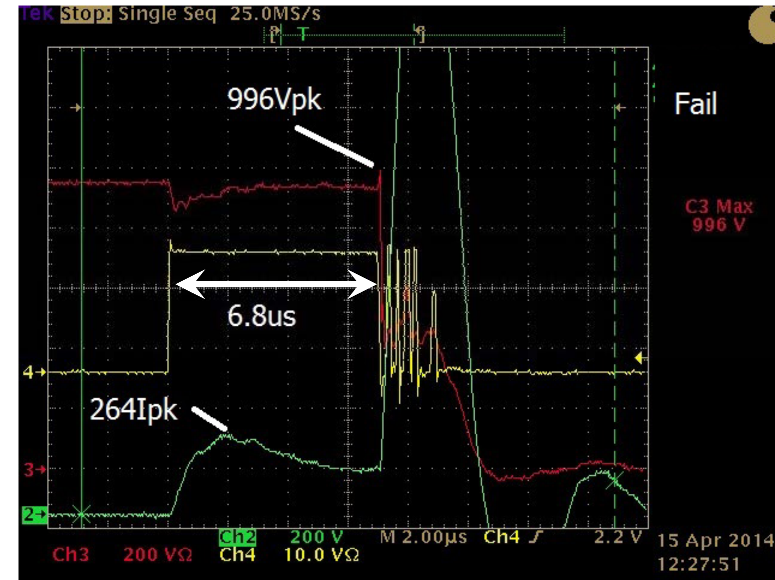
Superior Short Circuit Withstand

Microsemi | **Competitor 1**

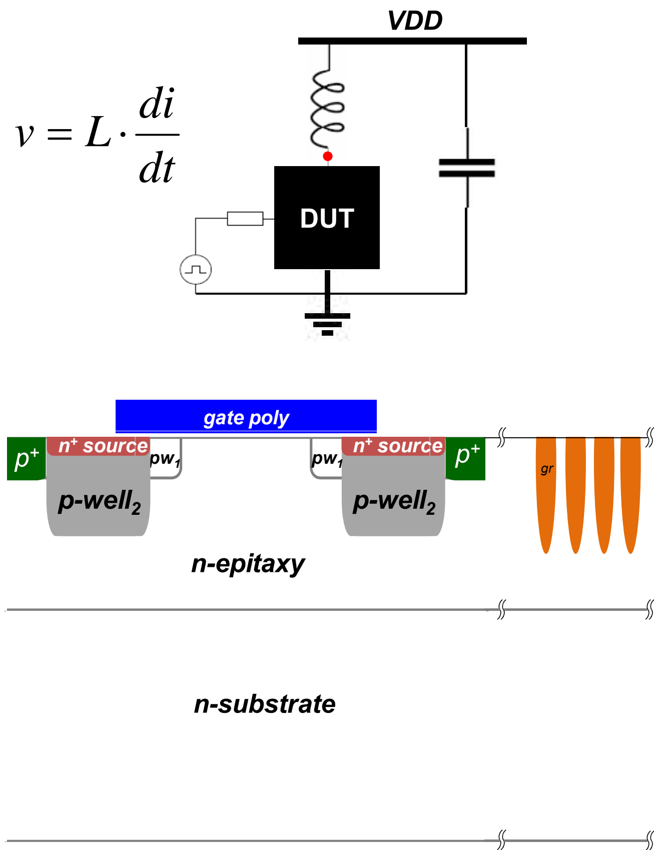


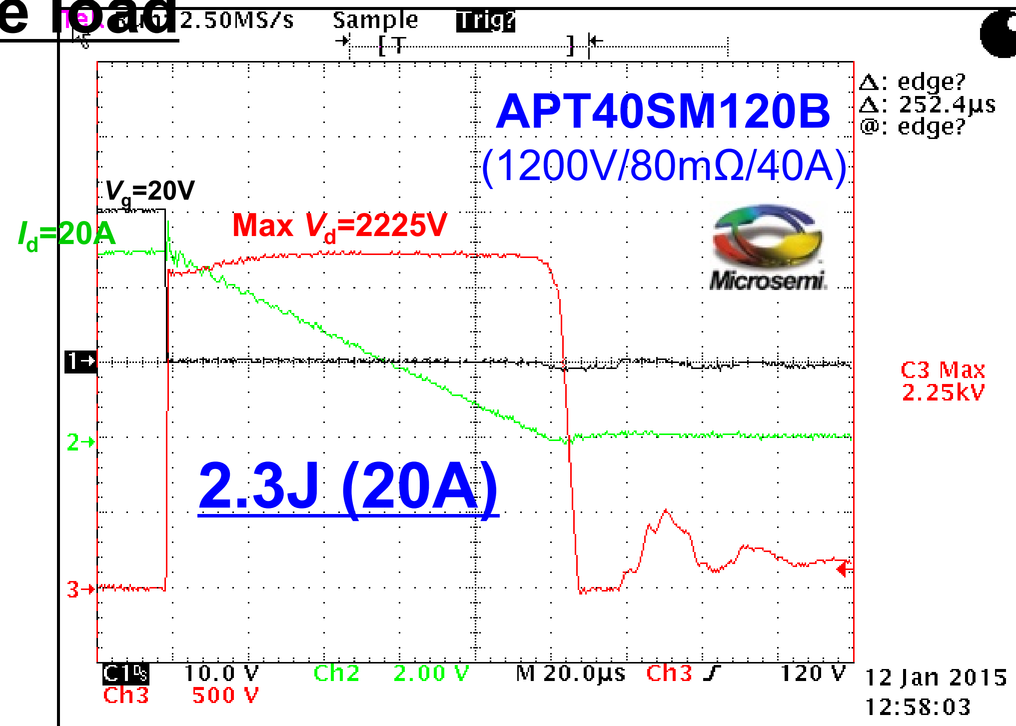


- Microsemi's 80mΩ SiC MOSFET demonstrates **25%** longer short circuit capability

Superb Avalanche Ruggedness

Unclamped inductive load





- Competitor1 not UIS rated, competitor2 *GEN*2 1200V/80mΩ/36A E_a=1J **(20A)**

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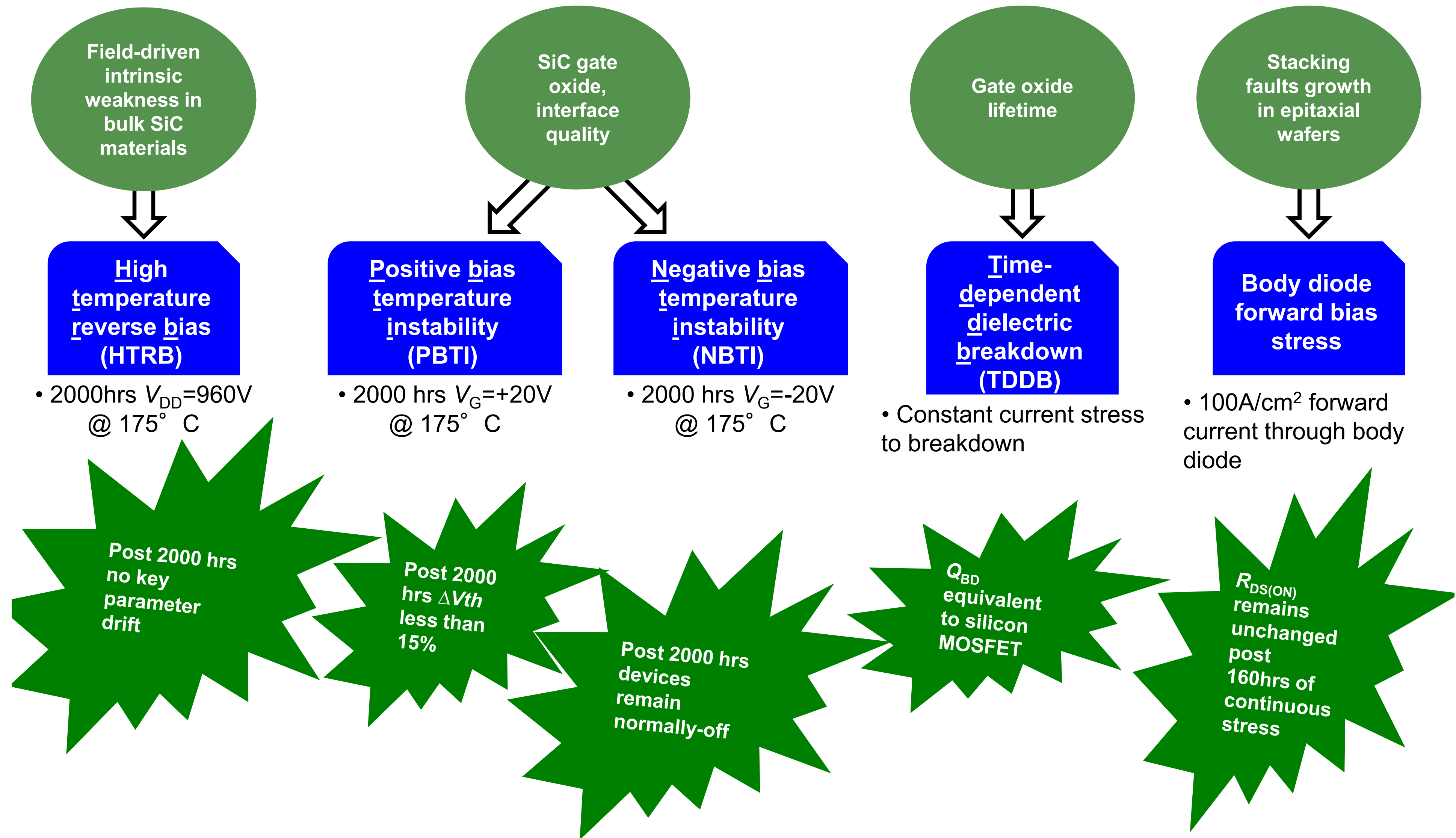
SiC MOSFET Technology Reliability Assessment



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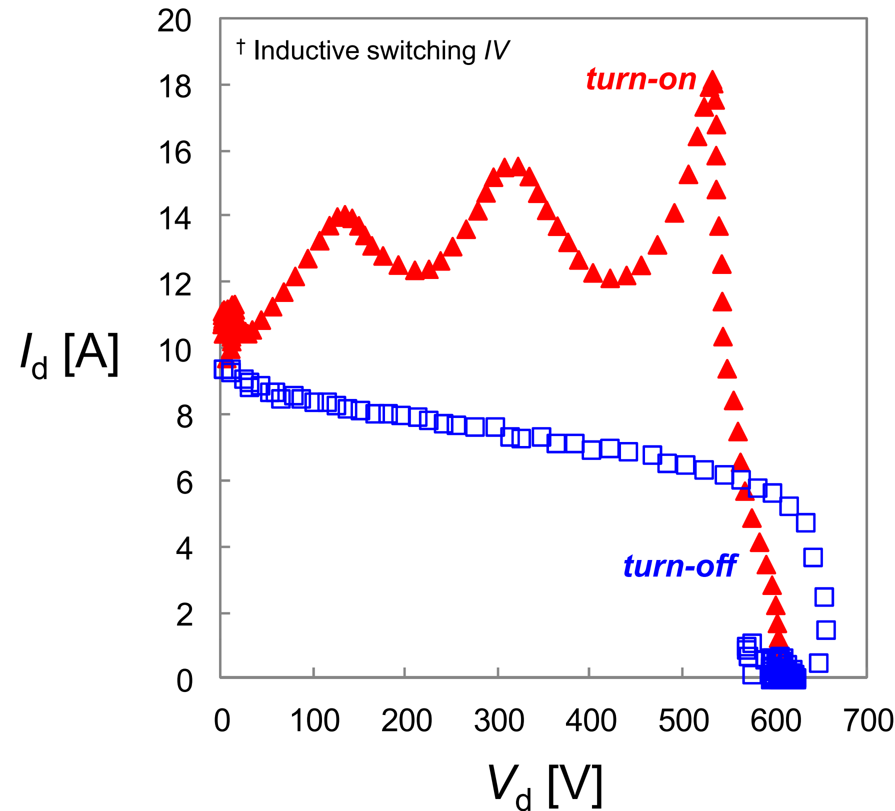
Die Size Scaling

Larger=More capacitance=More Switching Loss?

Difference Between On/OFF (not described by Q_g characteristic)



- Turn-on: An energizing process with transistor g_m generator hard at work
- Turn-off: Capacitive
- Area under the dynamic load-line: E_{on}>E_{off}

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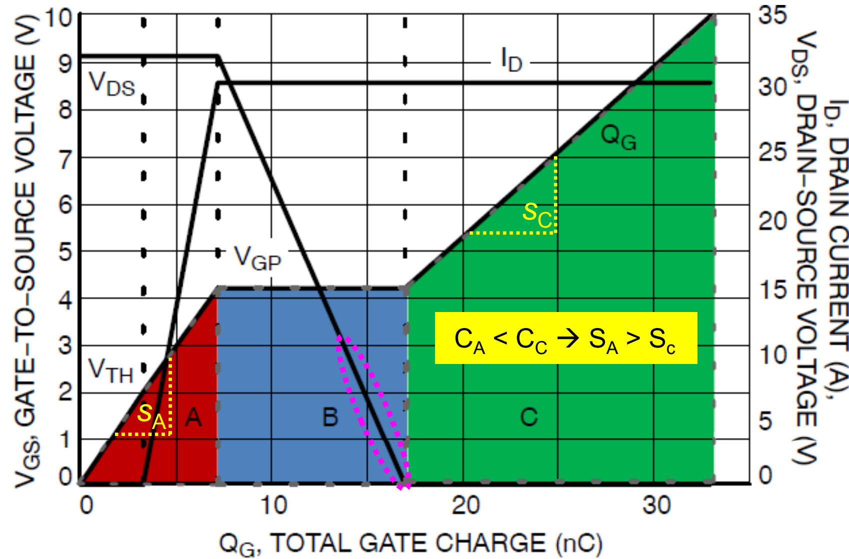
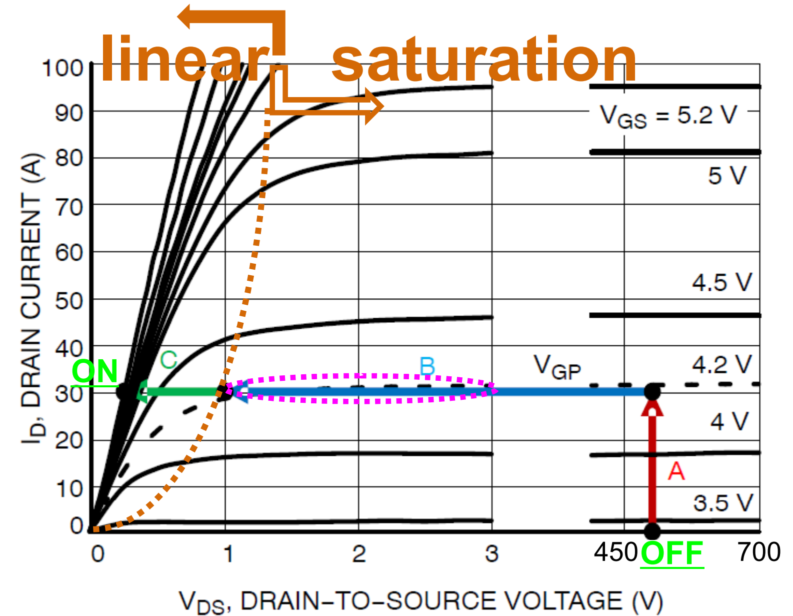
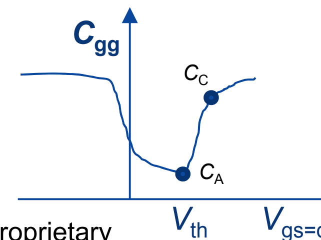
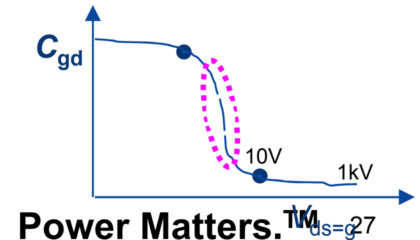
Gate Charge (Q_g) Characteristic





• Plateau voltage: g_m (but note: Q_g characteristic has no g_m action, i.e., high g_m does not speed things up due to the very choked gate current contrast to real switching. Further, more gate charge does not mean higher switching loss necessarily)
• Slope of V_g in region A: Capacitance at weak turn-on (C_A)
• Flatness of V_g in region B: Degree of saturation
• Slope of V_g in region C: Capacitance at strong turn-on (C_C) → No contribution to switching power loss (V_d=0)





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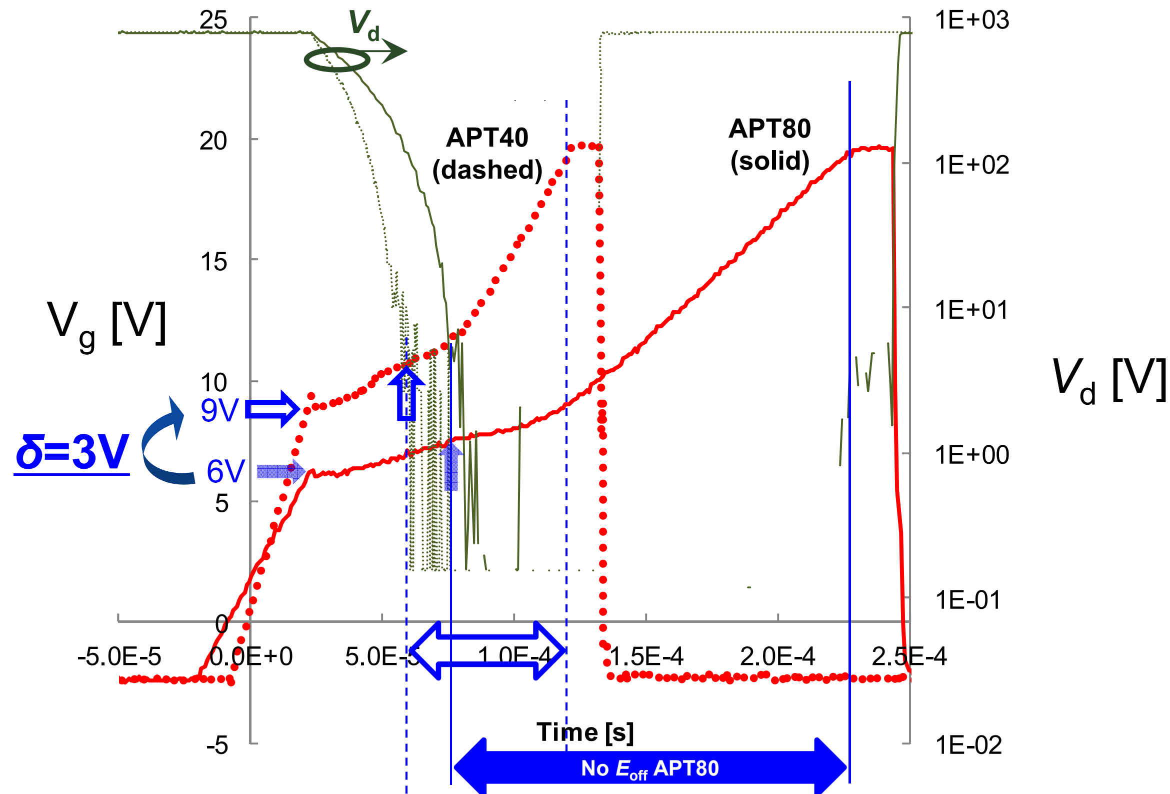
Low Current Q_g @ 10A

† Transistor size
APT80=2 × APT40



- Apparent: Bigger transistor=More capacitance (V_g slope, duration)
- Not so obvious: Bigger transistor=Lower $V_{plateau}$=Higher g_m
- Turn-on: g_m-dictated process → bigger transistor wins
- Turn-off: E_{off} worse for the bigger transistor (E_{off} is purely capacitance)
- E_{total} remains constant (current/capacitance scaling) → equal for big and small @ low/moderate currents

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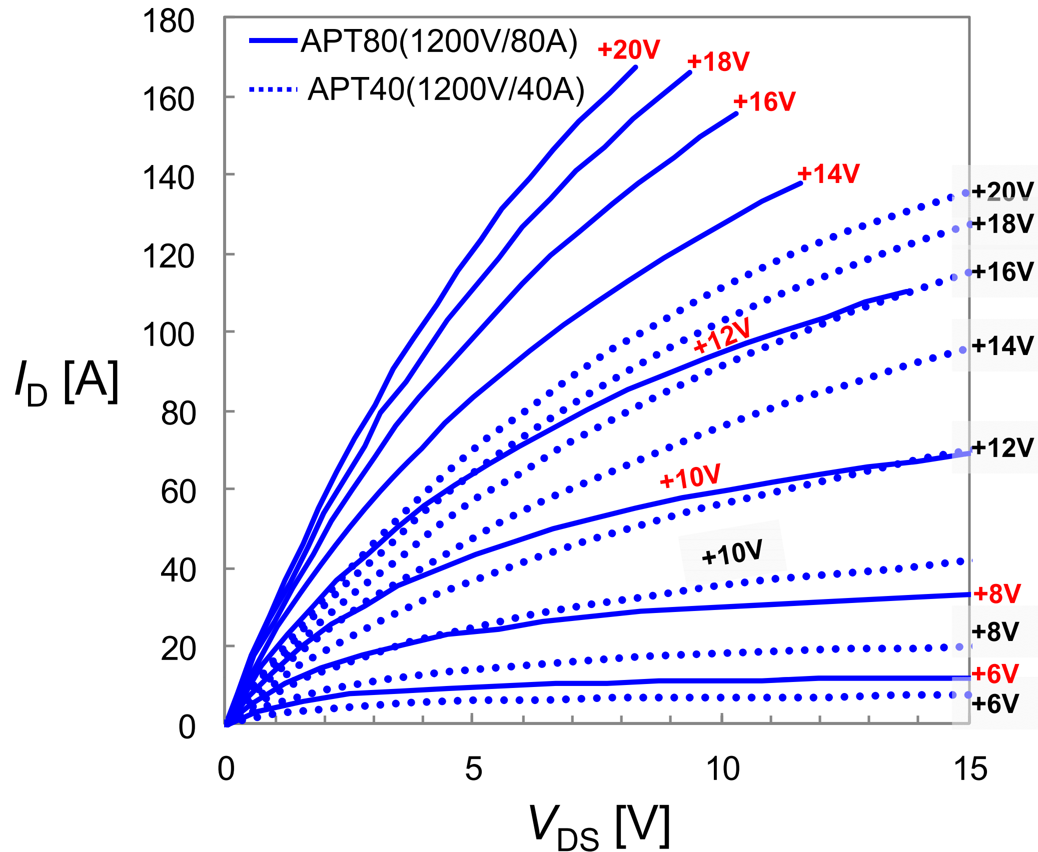
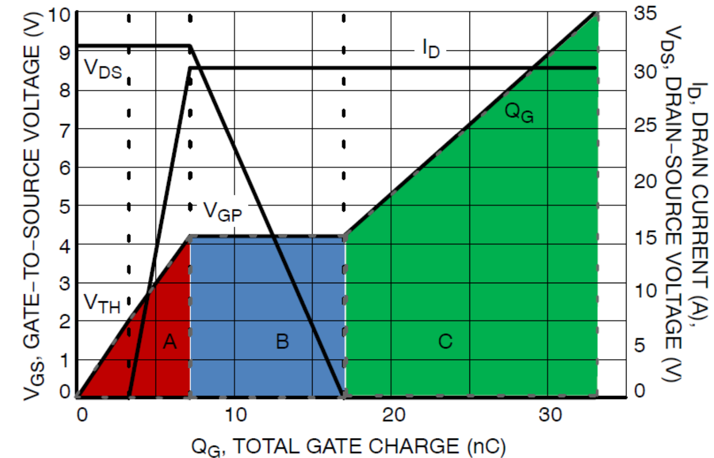
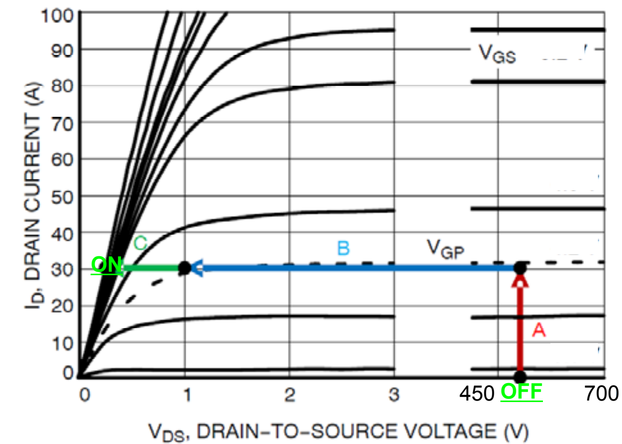
High Switching Current







- V_G required for a larger transistor to support a given current is lower
- @ a given high switching current, V_G of a smaller transistor is required to climb to a higher value to support I_D in the turn-on process → Lag in V_D fall time to complete turn-on → E_{on} ↑

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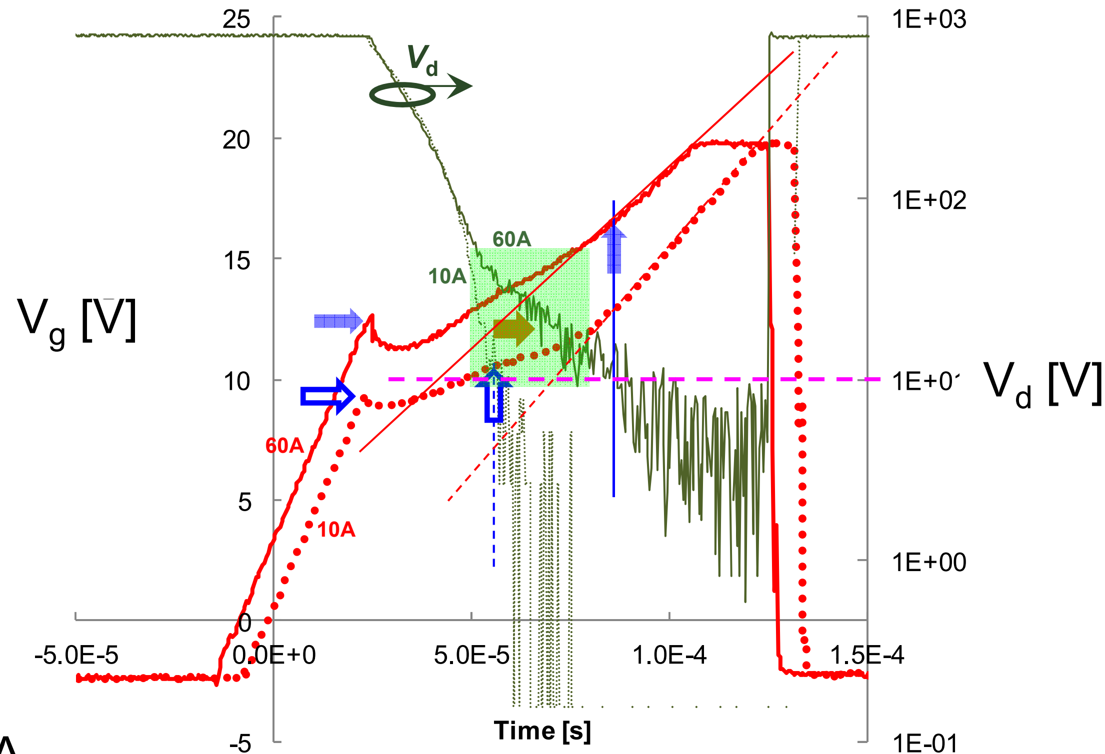
High vs. Low Switching Current Q_g

(for APT40SM)



- In contrast to 10A
  - o 60A pushes the transistor to higher V_g (more saturated) to support current
  - o Transistor struggles to support the current
  - o Higher V_d is required
  - o Lag in V_d fall results
  - o Note the worse gate voltage slope indicative of higher gate capacitance at higher V_g (no contriution to loss)

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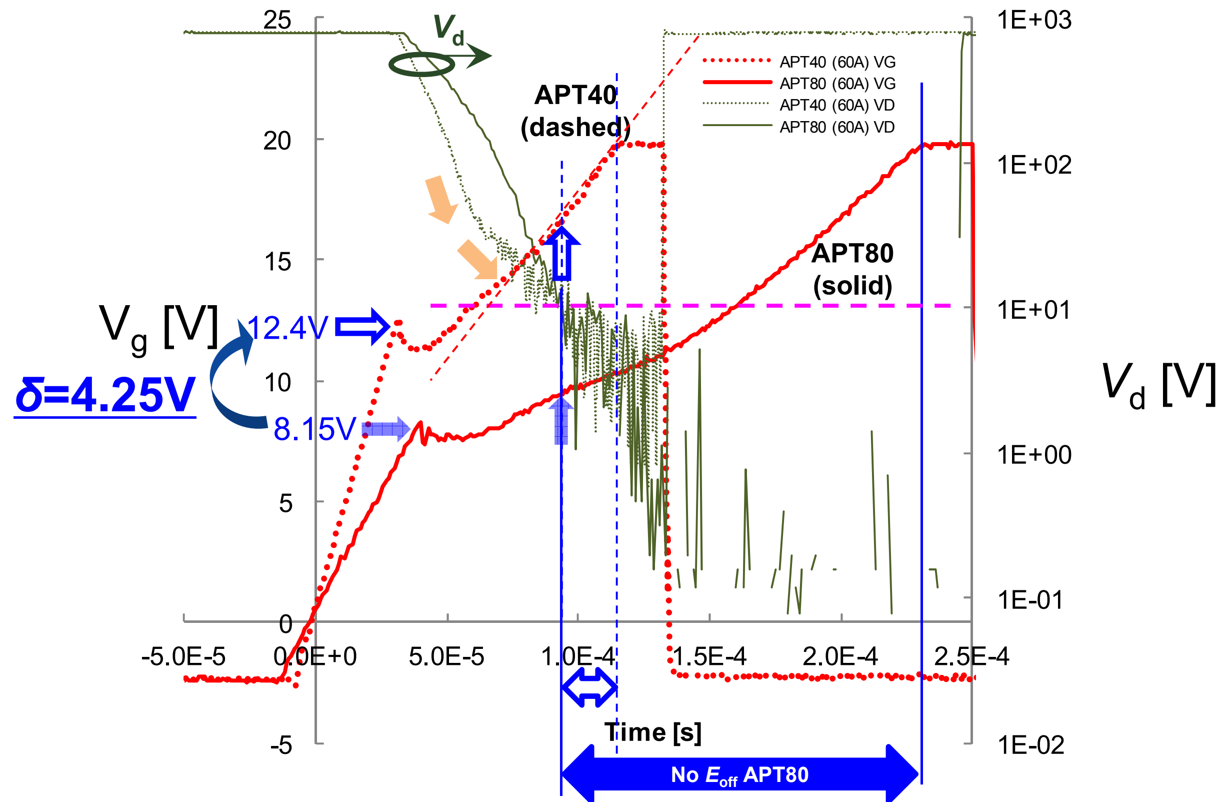
High Current Q_g @ 60A

(APT40 vs. APT80)



- Smaller transistor screaming for g_m (requires higher V_g to support high current)
- The falling of V_d slows toward the end of Miller plateau → onset of saturation for smaller transistor to support current at a higher V_d
- Lag in V_d dissipates more power during turn-on

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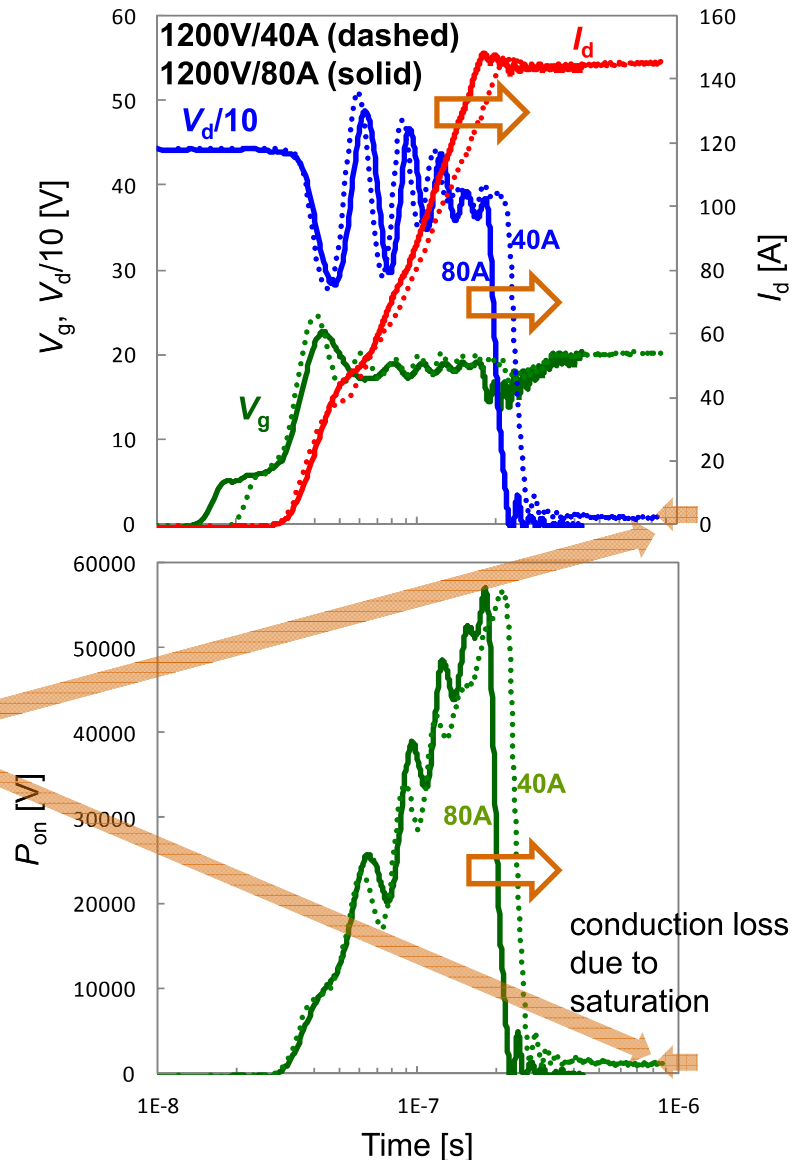
High Current Turn-On Lag

- @ a given high switching currents
  - o Smaller transistor lags in g_m → required to sweep to a higher voltage (V_g, V_d)
  - o Smaller transistor turn-on lag leads to higher turn-on switching loss

- A smaller transistor can only support a high switching current at a higher V_{ds} due to saturation, i.e., drain voltage never falls sufficiently leading to the increase of switching/conduction loss → conduction loss → a bigger transistor is needed



Transistor Size Scaling Summary

- Larger transistor → Lower conduction loss ($R_{DS(ON)}$)
- For a given voltage
  - @ low/moderate switching current → Equal E_{total} performance
  - @ high switching current → Larger transistor has lower switching loss
- At a switching current where drain voltage fails to complete its fall →

Transistor size cannot support the current and a bigger transistor is required

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Microsemi 700V SiC MOSFET Benchmarked Against 700V Silicon Superjunction MOSFET

Microsemi SiC MOSFET APT70SM070B: 700V, 53mΩ
Silicon Superjunction MOSFET IPW65R045C7: 700V, 45mΩ

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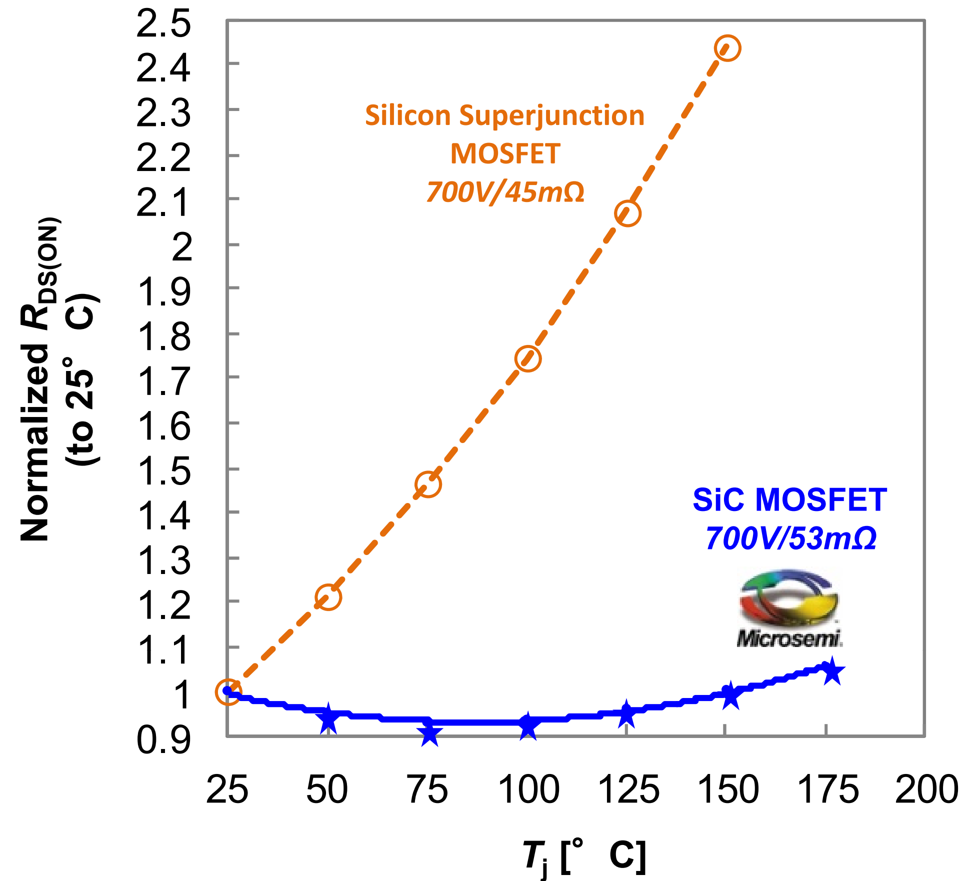
Thermal Friendly SiC MOSFET



- For silicon superjunction MOSFET, conduction loss deteriorates rapidly with temperature while SiC MOSFET remains temperature insensitive.
- Switching/conduction loss deteriorates at high current/temperature due to saturation

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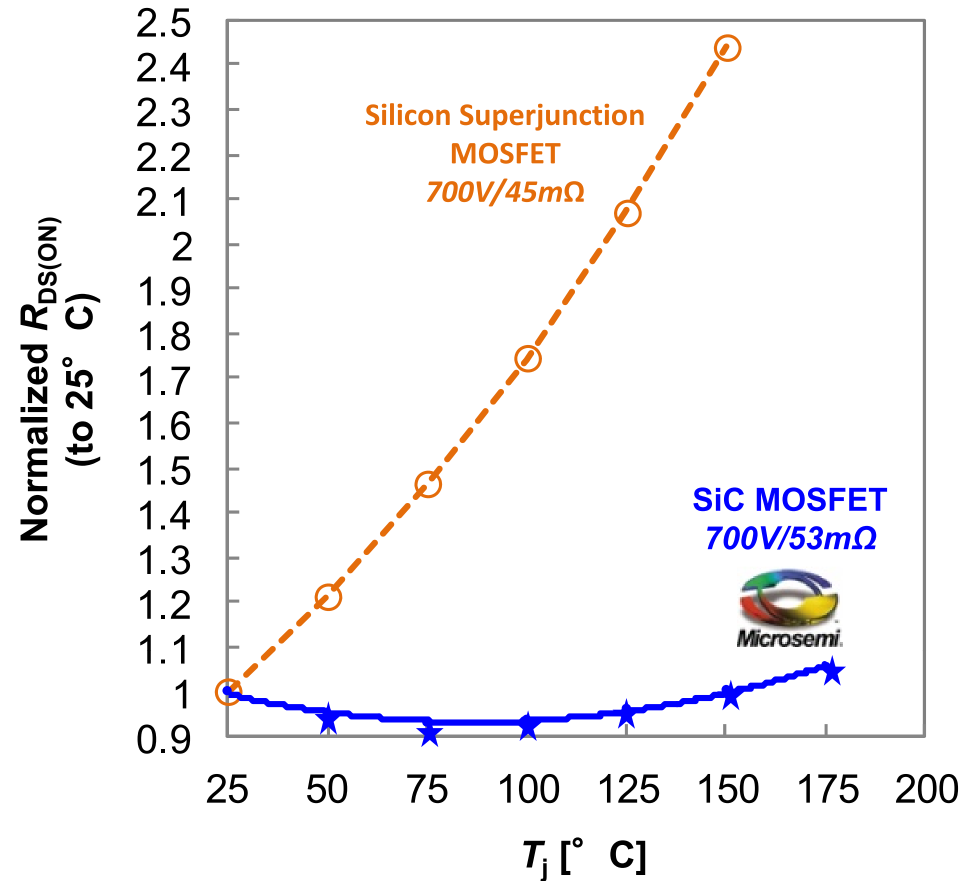
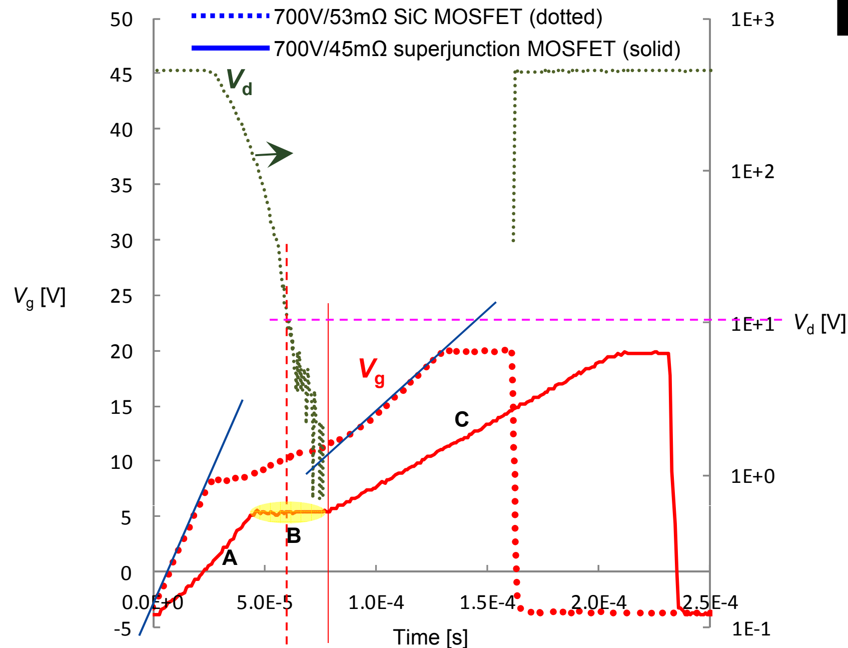
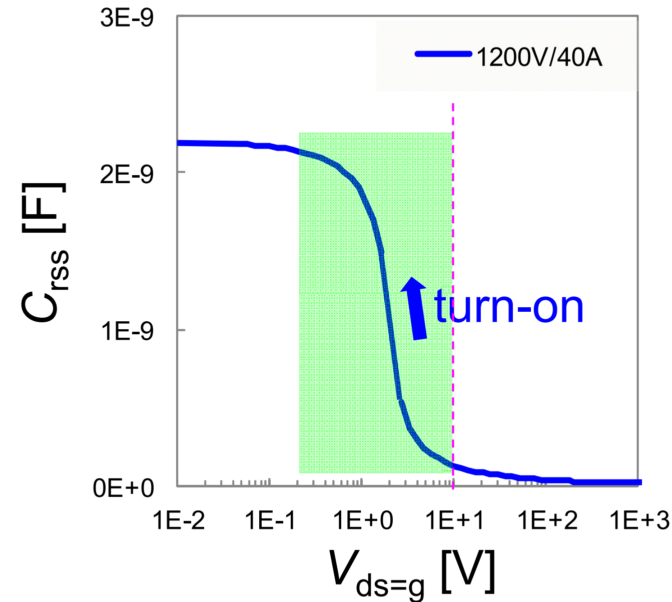
Thermal Friendly SiC MOSFET



- For silicon superjunction MOSFET, conduction loss deteriorates rapidly with temperature while SiC MOSFET remains temperature insensitive.
- Switching/conduction loss deteriorates at high current/temperature due to saturation

Silicon Superjunction MOSFET Q_g ~ 1.5 ×





- Plateau V_g → silicon superjunction MOSFET lower → stronger g_m (μ_n, die size)
- Slope of V_g in region A
  - SiC MOSFET steeper → lower input capacitance C_{iss} in region A (V_{th})
  - SiC breakdown field 7.3 × → Allows heavier doping for a given breakdown voltage
  - For a given breakdown voltage and $R_{DS(ON)}$ → SiC MOSFET has a smaller die size
  - Silicon superjunction MOSFET die size 1.67 ×
- Flatness of Miller plateau (region B)
  - Flat for silicon superjunction MOSFET → More saturation
  - Never flat for SiC MOSFET → Much less saturation → More current capability
- Region C slope of V_g post Miller plateau (C_{gg} of V_g>V_{th}) → No contribution to loss

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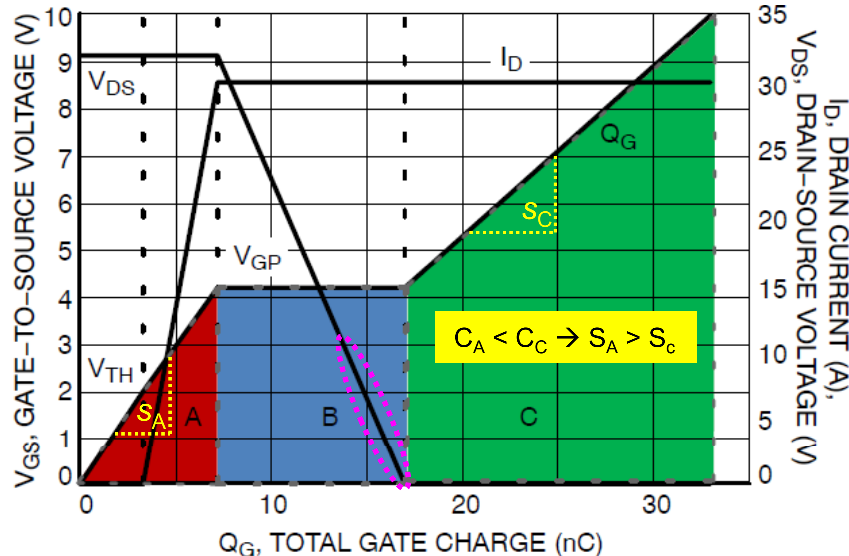
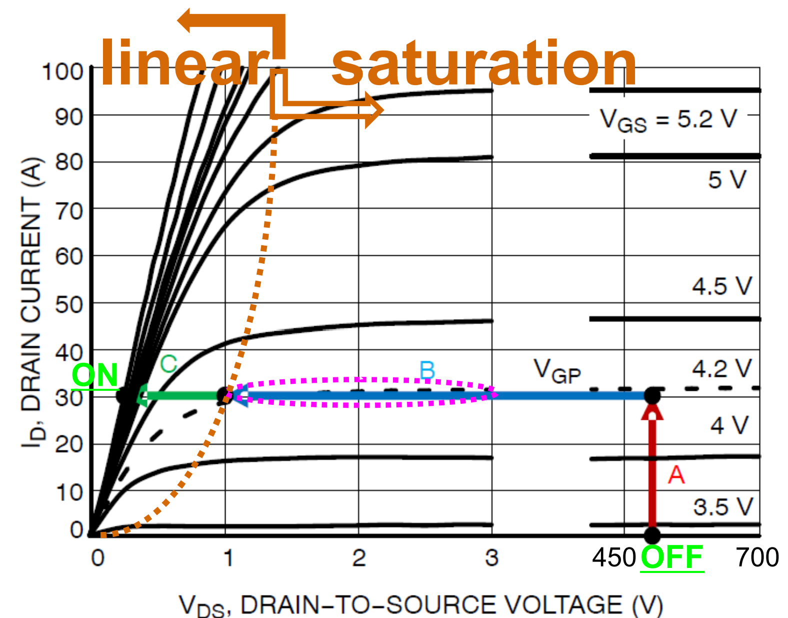
Q_g Characteristic Summary

	Features in gate charge characteristic	Switching performance implication	SiC MOSFET	Silicon superjunction MOSFET
g_m	plateau voltage	turn-on loss	-	+ (die size, mobility)
Input capacitance	slope(V_g)	switching loss	+ (die size, integration, layout)	-
Miller capacitance	duration of Miller plateau (till V_d falls sufficiently)	switching loss	(+) (die size, integration, layout)	-
Saturation	flatness of plateau	switching current, temperature capability	+	-





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SiC MOSFET Module Product Roadmap

- The SiC MOSFET Module product range is based upon:
  - Two die sizes S5F04 and S5F05
  - Two voltage ratings (700V and 1200V)
  - APT70SM70D (700V /53 mOhms typ, 60 mOhms max)
  - APT40SM120D (1200V/80 mOhms typ, 100 mOhms max)
  - APT140SM70D (700V/30 mOhms typ, 35 mOhms max)
  - APT80SM120D (1200V/40 mOhms typ, 55 mOhms max)

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SiC MOSFET Module Product Roadmap

- Electrical configurations
  - Boost Chopper
  - Buck Chopper
  - Single switch
  - Phase leg
  - Full bridge
  - Triple phase leg

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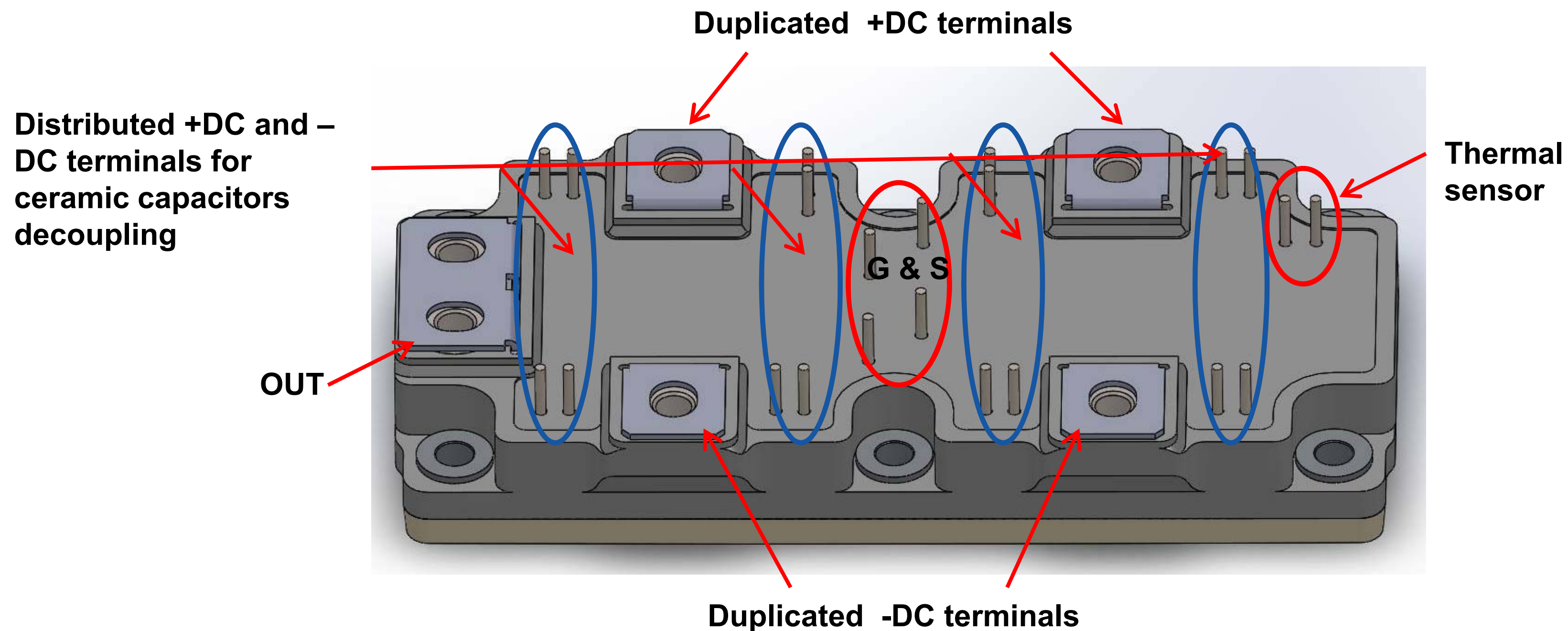
Packaging and power density

- To achieve the best switching performance and highest integration level a custom approach totally dedicated to the application efficiency target and mechanical constraints is the ultimate solution



Example of a high current, high frequency, high voltage SiC MOSFET phase leg

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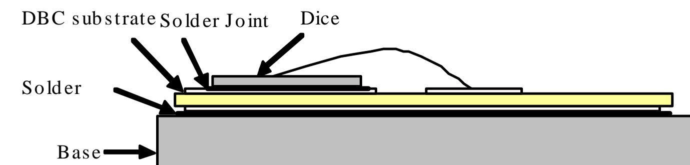
Packaging and Power Density

Module performance and reliability depend on assembly material choice

	Material	CTE (ppm/K)	Thermal conductivity (W/m.K)	Density (g/cc)
Base	CuW	6.5	190	17
	AlSiC	7	170	2.9
	Cu	17	390	8.9
Substrate	Al_2O_3	7	25	-
	AlN	5	170	-
	Si_3N_4	3	60	-
Die	Si	4	136	-
	SiC	2.6	370	-

	CTE (ppm/K)	Thermal conductivity (W/m.K)	Rthjc (K/W)
Silicon Die (120 mm^2) or SiC Die (40mm2)	4	136	
Cu/Al_2O_3	17/7	390/25	0.35
$AlSiC/Al_2O_3$	7/7	170/25	0.385
Cu/AlN	17/5	390/170	0.28
AlSiC/AlN	7/5	170/170	0.31
$AlSiC/Si_3N_4$	7/3	170/60	0.31



More closely matched TCEs of materials increases module lifetime.

Higher thermal conductivity maximizes thermal performance

Engineered materials such as AlSiC provide substantial weight reductions (up to 50%) over traditional copper material.

- AlSiC and Alumina offer best CTE matching
- AlN and Si3N4 on AlSiC offer higher thermal performance with good CTE matching

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Packaging and Power Density

- All full SiC Mosfet modules from Microsemi are built with Aluminium Nitride (AlN) substrate for best thermal performance
- Si_3N_4 substrates is offered as an option
- Any full SiC power module can be converted from a standard copper base plate to an AlSiC base plate for extended operating temperature range and higher temperature cycling capability

Packaging and Power Density

- SiC technology is capable of high temperature operation
- All Microsemi SiC MOSFET modules use high temperature solder alloy for die attach as a standard to allow maximum junction temperature operation
- As SiC technology will improve, high temperature solder alloy will become a limitation for extreme junction temperatures operation
- Ag sintering technology is the future for SiC devices assembly

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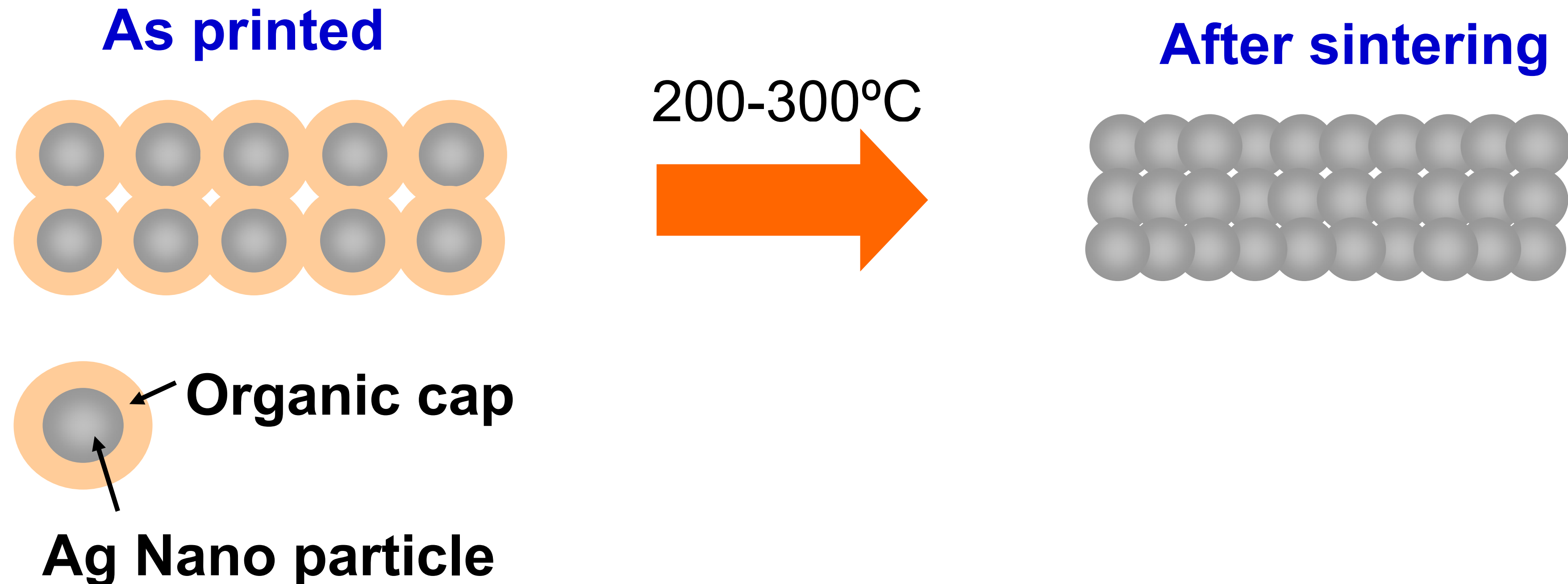
Packaging and Power Density

Basic Ag sintering process



- During Sintering process solvents and organic cap escape, exposing pure silver core to allow particles to coalesce and form solid conductive Ag structure

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Packaging and Power Density

Ag is an ideal Die Attach Material

	Melting range	Density	CTE	Tensile strength	Modulus	Thermal conductivity	Electrical resistivity
Material	°C	g/cm³	ppm/°C	MPa	GPa	W/m.K	µΩcm
Silver	**962**	**10.5**	**20**	**140**	**76**	**419**	**1.6**
92.5Pb5Sn2.5Ag	**287-296**	**11**	**29**	**29**	**-**	**27**	**8.5**
80Au20Sn	**280**	**14.5**	**16**	**276**	**59**	**57**	**16**
96.5Sn3.5Ag	**221**	**7.4**	**30**	**38**	**50**	**58**	**12.5**

- Ag paste is processed at 250°C – 300°C under pressure to form pure Ag interface
- After processing , Ag paste acts as bulk Ag with a melting point of 962°C
- Density (85 to 90%)
  - Thermal conductivity: 200 – 300 W/m.K
  - Electrical resistivity: 2 – 2.5 µΩcm
  - No intermettallic phases formed
- Ag paste allows highest thermal performance and reliability

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Thank You

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