‘Review’ of the machine protection system in the SPS

J. Wenninger BE-OP

MPS Organization

All SPS Machine Protection issues are handled together with the LHC in the (LHC) Machine Protection Panel (MPP).

>> Coherent approach, same solutions etc..

Any person making modification to the SPS ring and TLs that possibly requires new interlocks or modifications to the interlocks should contact the MPP (or me) as soon as possible.

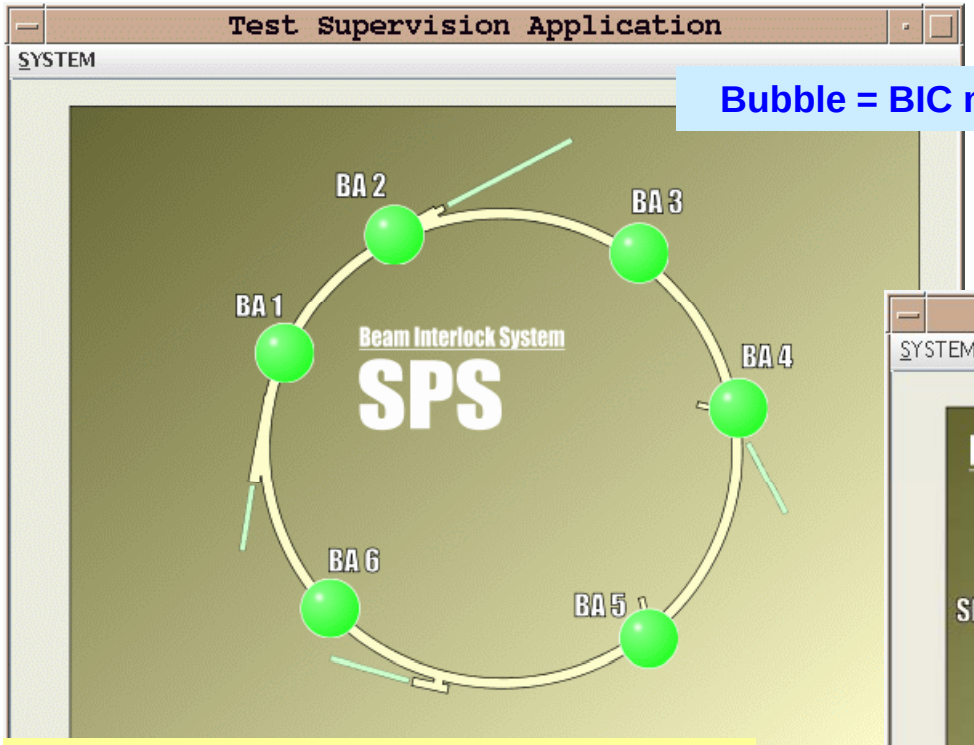
Beam interlocks also need some planning !

SPS Hardware Interlock Systems

- Since 2007 the SPS hardware interlock systems are **standardized with the same hardware that is also used at the LHC**, with so-called BICs (Beam Interlock Controllers) connected in a loop (ring) or in daisy-chain (extractions).
- Components of the SPS interlock system hardware:
  - 1 ring beam permit loop.
  - 2 extraction interlock systems.
  - 16 BIC modules, 2 special BIC ‘masters’ for fast extractions.
- All interlock signals (BLMs, vacuum etc etc) are connected to the beam dump kicker or extraction kickers through the BIC modules using standardized connection boxes (CIBUs).

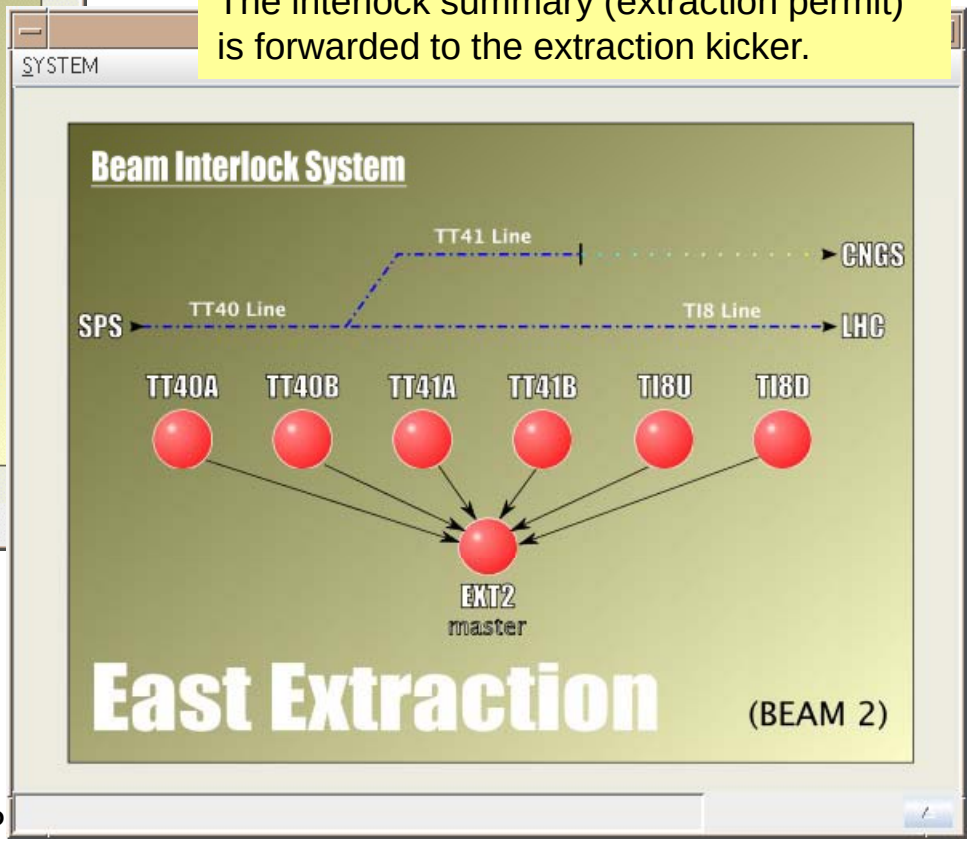
>> Experience with the new interlock hardware is excellent !

BIS Architectures



Bubble = BIC module

Clients (= interlock providers) are connect according to the transfer line.
The interlock summary (extraction permit) is forwarded to the extraction kicker.



Clients (= interlock providers) connect in each BA.
The interlock summary (beam permit) is carried over a loop to the beam dump system in BA1.

SPS Software Interlock System

- Since 2007 a new Software Interlock System (SIS) is used at the SPS.
- Very robust and reliable in house design by CO-AP.
- Role of the SIS is to:
  - *Fill 'cracks' in the hardware interlock system.*
  - *Provide advance warning for some dangerous situations.*
  - *Ensure consistency of beam modes and machine state.*
  - *Play 'Big Brother' for operations and experts (general settings and interlock settings surveillance).*
  - *Interact with the timing system to stop beams at the source.*
- Interlock logic is configured by SPS-OP (2 persons), digitally signed and protected.
- There are **~ 1000 interlocks** in SIS, **updated once per cycle**.

>> Experience with SIS is excellent !!

>> SIS is essential for SPS operations !!

CNGS & LHC transfer lines MPS

- The MPS for CNGS and LHC transfer line was designed ‘from scratch’ and was backed by failure simulations to define the requirements.
- Roughly 50% of the SPS hardware interlocks are concentrated in those TLs.
- The interlock providers are either new systems (CNGS BPMs, TL BLMs, FMCMs…) or existing systems (PC currents, beam position at extraction).

  For existing systems had to live with their ‘limitations’ (reaction time).

  I thank all colleagues who spend some of their time and budget to help build the protection for the lines!
- Present status:
  - *Interlock coverage is very good, but not ‘crack-free’. Work ongoing to fill remaining cracks.*
  - *Non-negligible risk comes from MDs & expert mistakes (interlock settings).*

    - 2 near-misses on CNGS in 2008 during expert intervention.

>> Situation for the CNGS & LHC TLs is very good !!

Ring and North Transfer line

- Main systems that provide interlocks for the SPS ring & TT20 TL:
  - *Vacuum (valve closure).*
  - *Main power supplies and sextupoles.*
  - *Kickers (local mode & failures).*
  - *BLMs.*
  - *Fast position interlock (hor. plane, **turn-by-turn**).*

- Protection against uncontrolled beam loss is relying on the BLMs. The fast horizontal position interlock provides a precious and very fast second line of defense in certain situations.

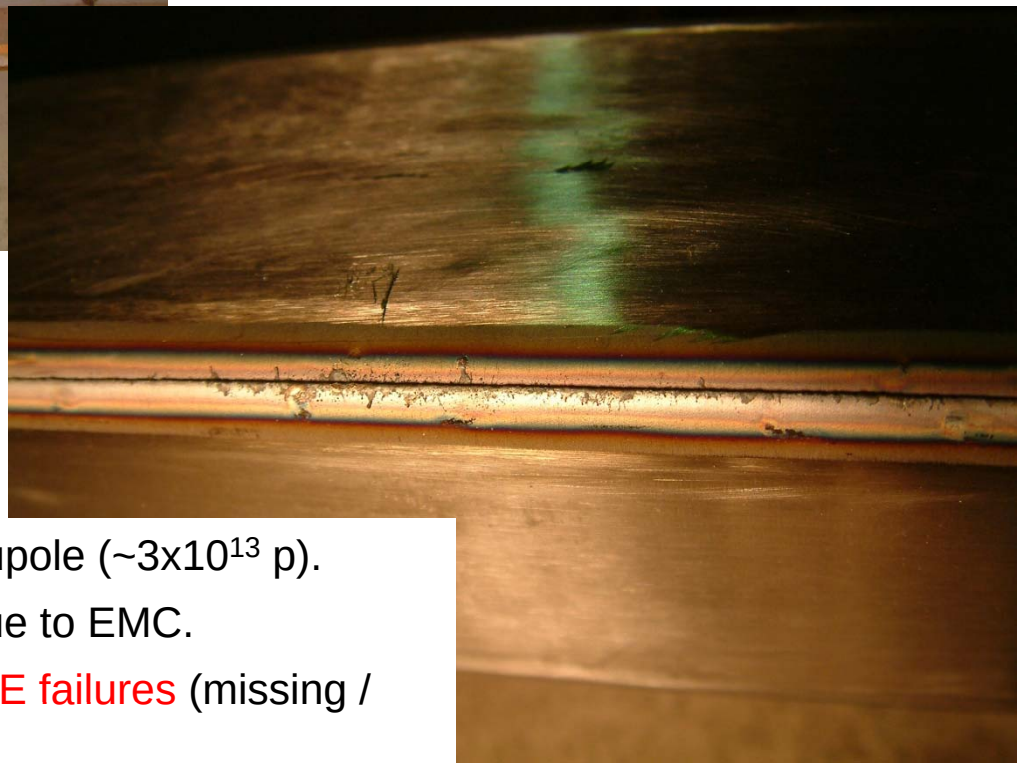
Beam Loss Monitors

- SPS BLM system is based on ionization chambers.
- BLM electronics/interlocking comes in 3 types:
  - Ring type (BLRING):
    - *Interlock logic in FEC software, every 20 ms.*
    - ***Reaction time ≤ 20 ms. Not possible to reduce (CPU).***
    - *SPS ring and North transfer line.*
  - Extraction type (BLD):
    - *Interlock logic in hardware.*
    - ***reaction time ~ some μs.***
    - *LSS1, LSS2, LSS4 and LSS6 extractions channels.*
  - CNGS and LHC transfer line type (BLMI):
    - *Interlock logic in software.*
    - ***Reacts after the extraction → can only stop further extractions.***
    - *TT40, TI8, TT41, TT60 and TI2 transfer lines.*

BLRING reaction time is not fast enough for severe failures (mains etc) that are faster than 20 ms !

Only the fast beam position interlock provides protection against the fast failures… in the horizontal plane.

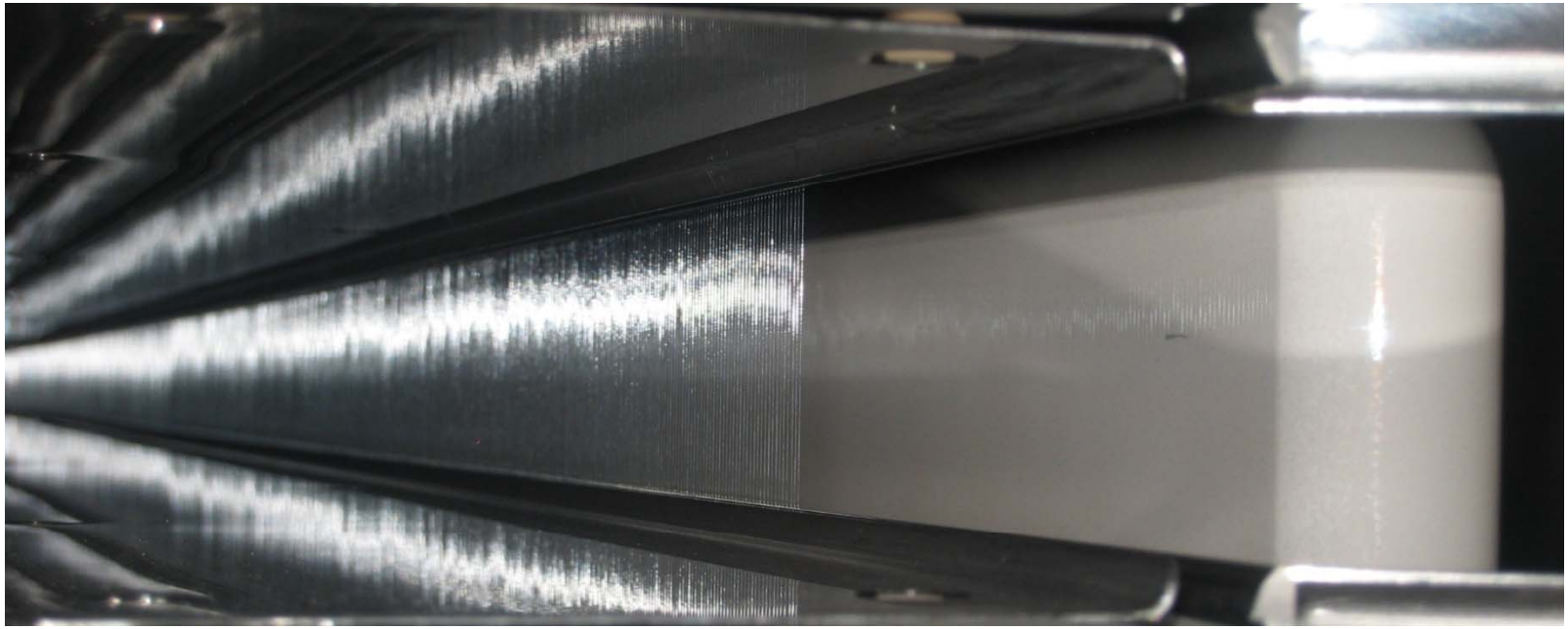
TT40 Ripper / 2004



Extracted LHC beam lost in TT40 quadrupole (~3×10^{13} p).

- Cause: Extraction septum (MSE) fault due to EMC.
- MPS issue: Insufficient protection for MSE failures (missing / too slow interlocks).
- Action: Fast PC interlocks, FMCMs, etc – **problem is solved**.
- See AB-Note-2005-014.

ZS Ripper / 2007

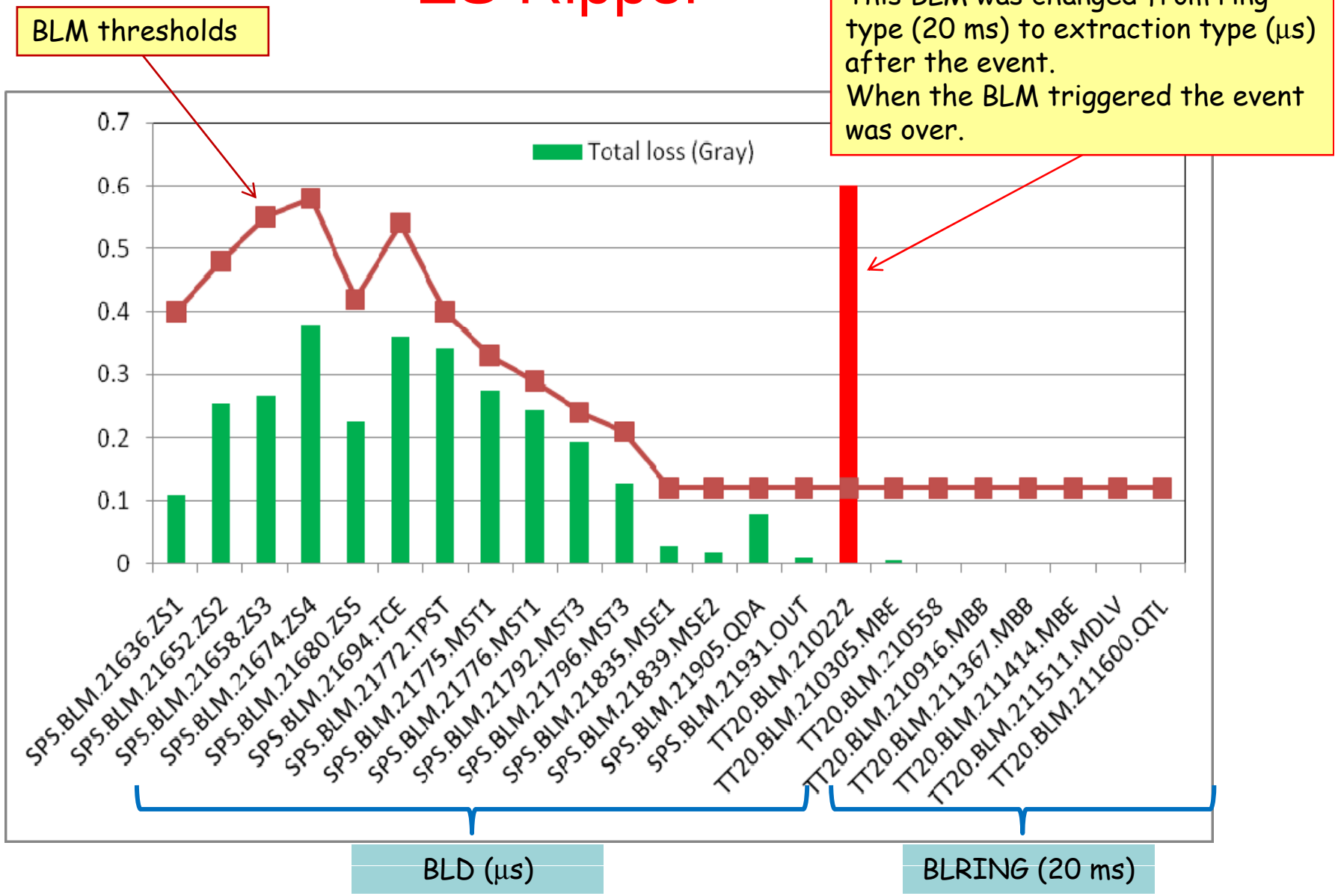


Electrostatic septum (ZS1) wires cut by slow extracted beam (~9×10^{12} p).

- Cause: controls 'problem' turned a slow into a fast-slow extraction.
- MPS issue: BLMs too slow / threshold too high (slow extraction).
- Action:
  - control system protections (limitations) and SIS.
  - one BLM: reaction time of 20 ms to few μs.
- See AB-Note-2008-003.

Partial solution

ZS Ripper


BLM thresholds
This BLM was changed from ring type (20 ms) to extraction type (μs) after the event.
When the BLM triggered the event was over.
Total loss (Gray)
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
SPS.BLM.21636.ZS1
SPS.BLM.21652.ZS2
SPS.BLM.21658.ZS3
SPS.BLM.21674.ZS4
SPS.BLM.21680.ZS5
SPS.BLM.21694.TCE
SPS.BLM.21772.TPST
SPS.BLM.21775.MST1
SPS.BLM.21776.MST1
SPS.BLM.21792.MST3
SPS.BLM.21796.MST3
SPS.BLM.21835.MSE1
SPS.BLM.21839.MSE2
SPS.BLM.21905.QDA
SPS.BLM.21931.OUT
TT20.BLM.210222
TT20.BLM.210305.MBE
TT20.BLM.210558
TT20.BLM.210916.MBB
TT20.BLM.211367.MBB
TT20.BLM.211414.MBE
TT20.BLM.211511.MDLV
TT20.BLM.211600.QTL
BLD (μs)
BLRING (20 ms)

CNGS Ripper 27th June 2008

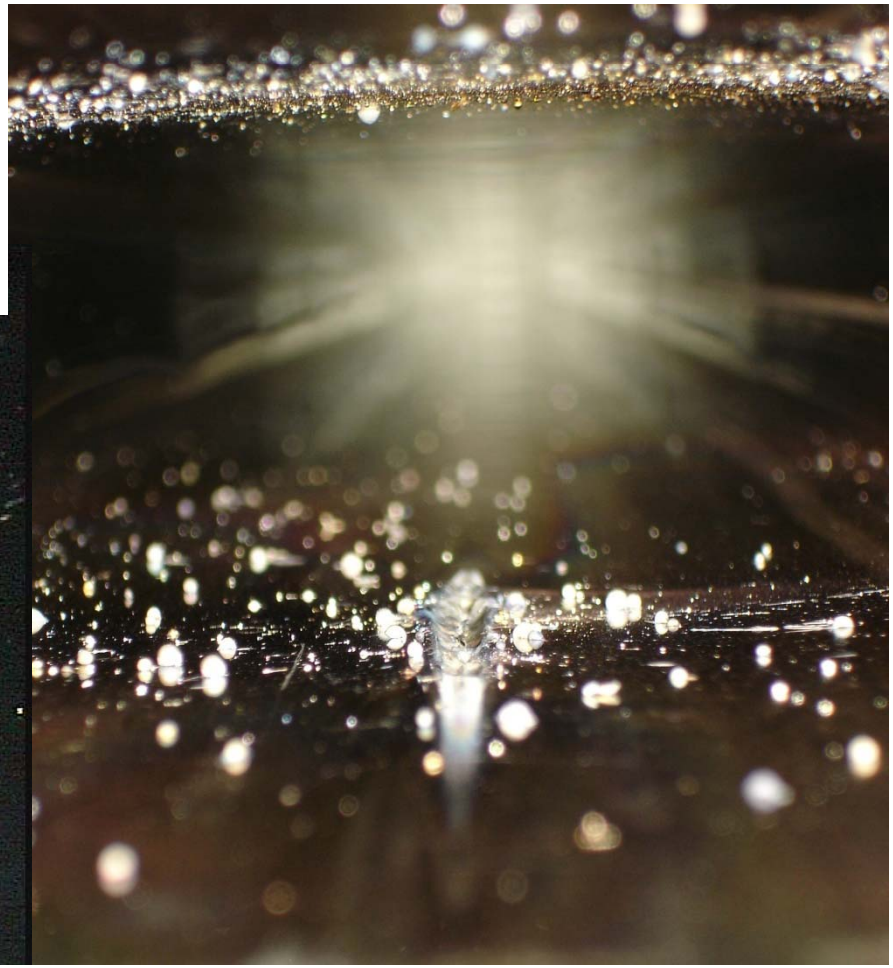
Beam impact in MBB.12530 of CNGS beam – vac. chamber ripped open (~3×10^{13} p).

- Cause: timing system problem ('freeze'), end of cycle dump not executed.
- MPS issue: BLMs too slow/thresholds too high, no fast position interlock in vertical plane.

- Action:
  - 3 protection layers against such timing failures.
  - New fast position interlock system in V plane for 2009 (needs testing !).

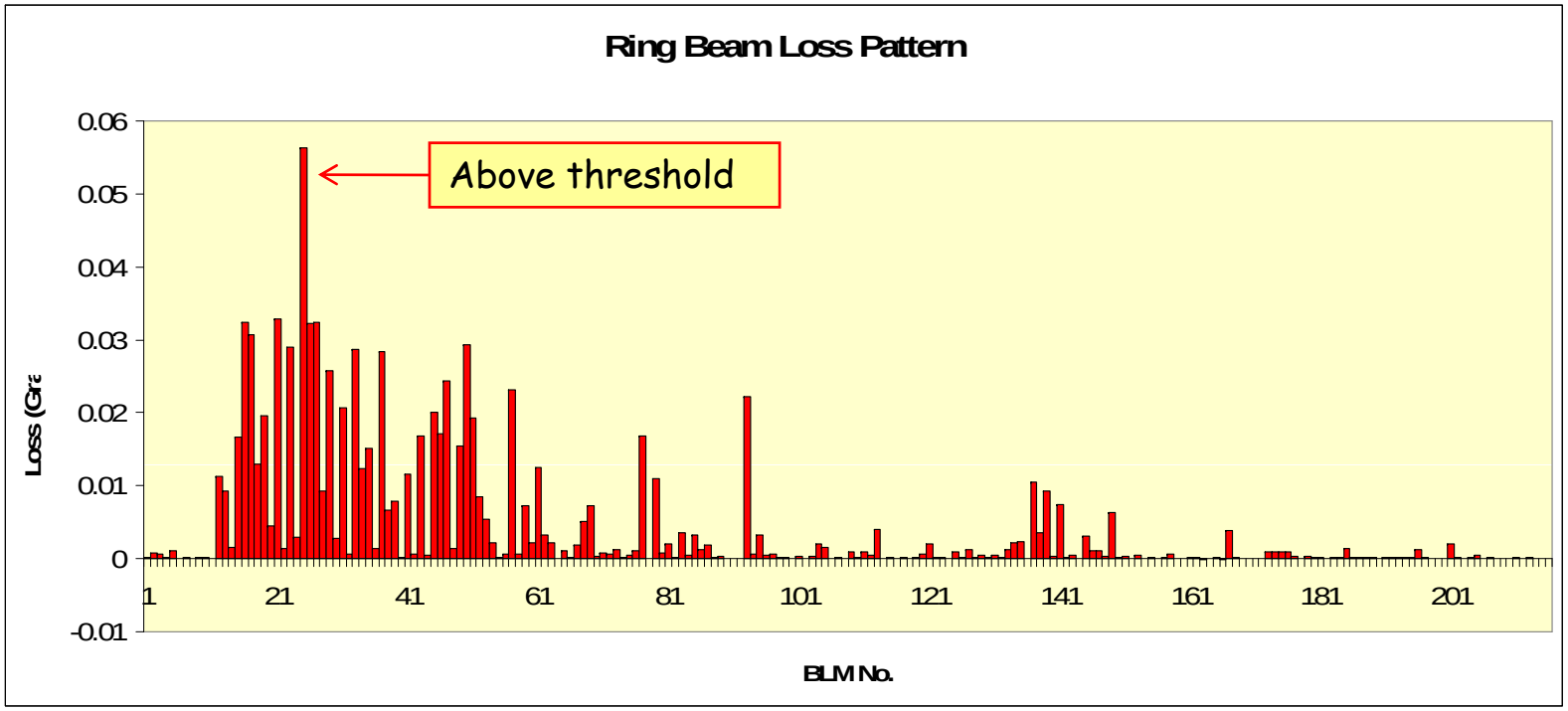
Partial solution

- See BE-Note-2009-003.



CNGS Ripper Beam Loss

- In the ring the beam loss was distributed over a large area, but only one monitor exceeded the threshold (lowest ~ 40 mGray).



Cures…

- New BLM electronics that:
  - *is faster (~ turn-by-turn).*
  - *has 2 or 3 thresholds that apply to different time scales (some μs - 1 ms, 10 ms and cycle).*

  >> in the pipeline for 201x, based on LHC design.
- New BLMs to improve coverage?
  - *I'm talking here about at least a factor … 2 !*

  >> must be backed by simulations.
- New beam position interlock system that provides redundancy wrt BLMs:
  - *turn-by-turn.*
  - *cover both horizontal and the vertical plane.*

  >> test a new system in 2009 for the vertical plane (BIC connection ready).

Conclusions

- The BIS hardware at the SPS is ‘state-of-the-(CERN)-art’.
  - *Excellent performance and very good diagnostics.*
- The CNGS and LHC transfer lines are very well protected.
  - *In the process of closing one small crack after the other…*
- To significantly improve protection of the ring and TT20:
  - *New BLM electronics (faster & multiple integration times and thresholds).*
  - *Additional BLMs (twice as many?) to improve coverage.*
  - *Fast position interlock for both planes – hopefully in 2009.*

    >> will reduce the burden from SIS
- Simulations and possibly beam tests are required to specify more coherently the needs (BLM integration times…).