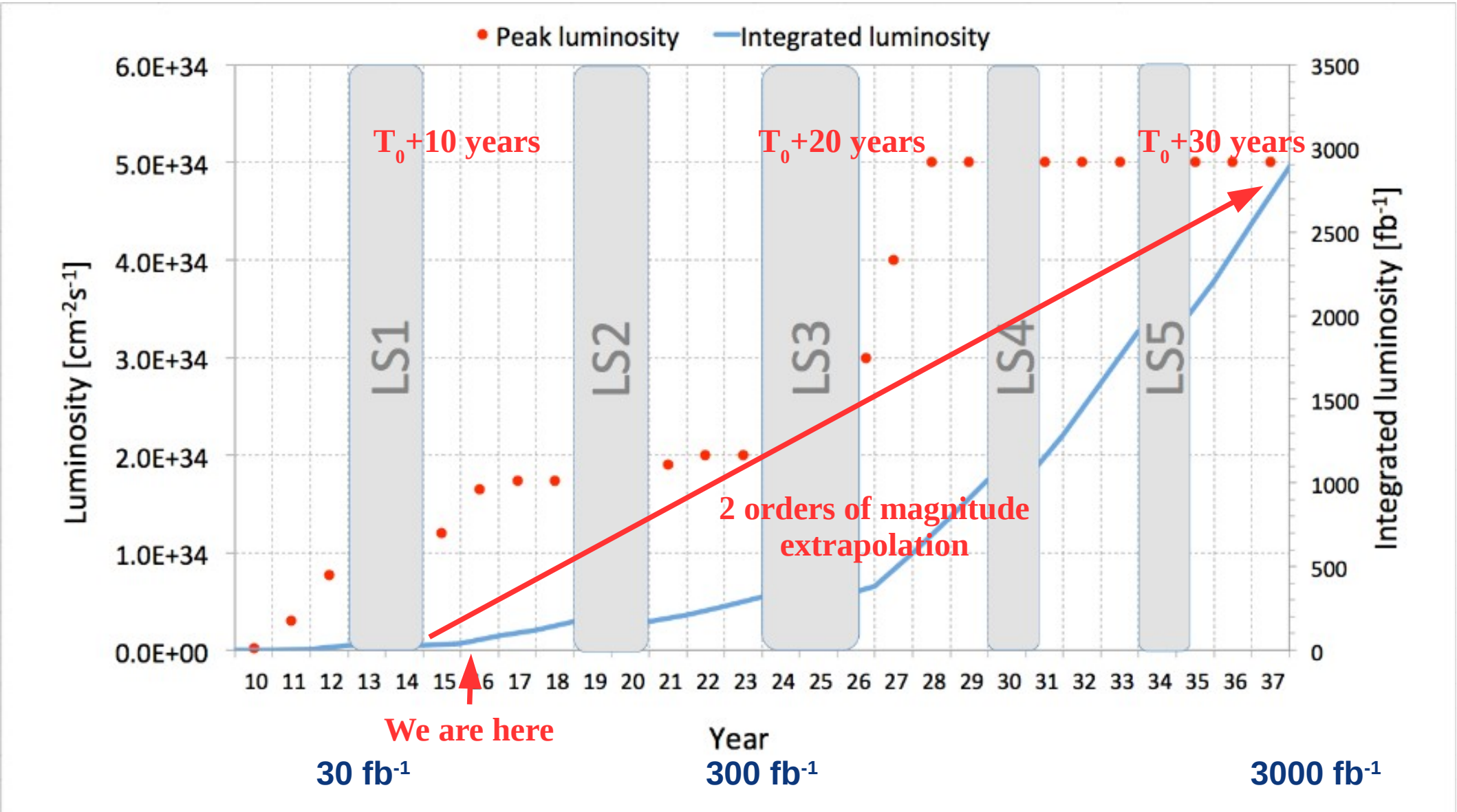
ECAL EB electronics upgrade

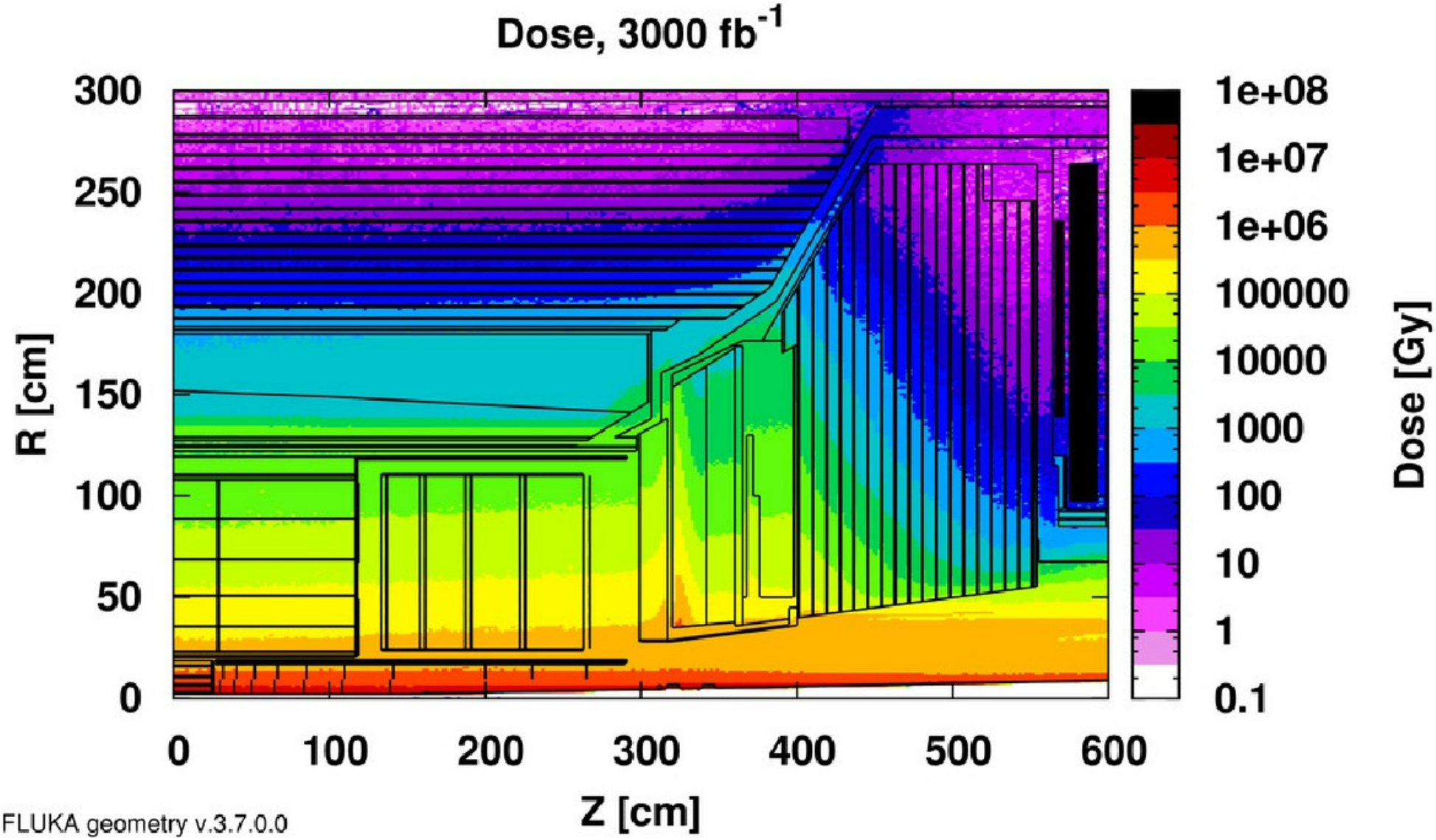
Overview of requirements for VFE part
List of questions to be answered

HL-LHC

- **Luminosity**



- **Radiation**

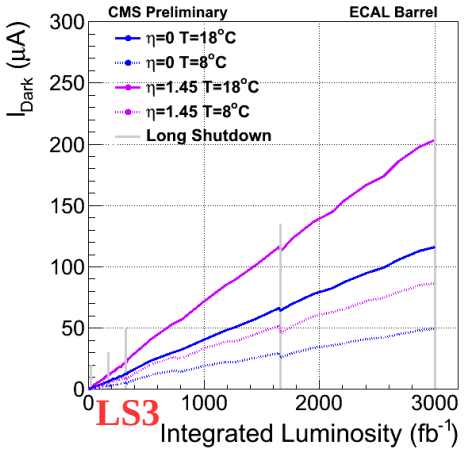

Dose, 3000 fb-1
R [cm]
Z [cm]
Dose [Gy]
0
50
100
150
200
250
300
0
100
200
300
400
500
600
1e+08
1e+07
1e+06
100000
10000
1000
100
10
1
0.1
CMS FLUKA geometry v.3.7.0.0

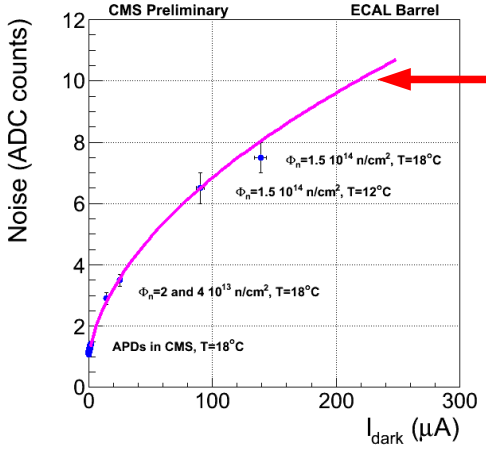
ECAL Barrel VFE challenges

- **Reminder : Goal of ECAL is energy measurement !**
- **Radiation hardness of electronics**
  - **Is it really a problem ?**
- **Mitigate APD leakage current increase : up to 200 µA**
  - **Effect on electronic noise**
    - ► **Effect on ECAL resolution**
    - ► **Effect on spike rejection**
  - **Effect on APD temperature**
- **Mitigate spike events :**
  - **At L1**
  - **In offline analysis**
- **Mitigate events pileup : up to 200 P.U./crossing**
  - **In-time pileup**
  - **Out-of-time pileup**

Energy measurement

- **Restore resolution or mitigate degradation due to APD leakage current increase and crystal aging**
- **If no upgrade : > x10 noise increase (in charge) w/r to Run1 in M4**





> 400 MeV/sample

- **Questions :**
  - **Light yield at LS3 ?**
  - **APD leakage current at LS3 ?**
  - **Is it safe to run at 8 °C or below ?**
  - **Signal shapes**
    - ► **Mandatory for designers**

Simulation session

TB session

Energy measurement : Analog

- **Options up to now**
  - **MGPA++**
  - **TIA**
  - **QIE++**
- **Questions:**
  - **Maximum noise level affordable**
  - **Dynamics**
  - **Number of output gains**
  - **Linearity**
  - **Performances on noise, spike tagging, PU mitigation**
  - **Calibrated charge injection**
- **To be defined:**
  - **Case studies for comparison**

VFE asic session

Energy measurement : Digital

- **ADC characteristics**
  - Number of bits
  - lsb value
  - Sampling frequency
  - Digital Compression
  - Linearity
  - Technology
  - Home made or IP from industry ?
  - Integration with P.A ?
  - How many channel per chip ?

ADC session

Ancillary services

- **Power supplies**
  - Question : If existing DC-DC converter satisfactory for our need (extra filtering) ?
  - Question : What is our power budget ?
- **Environmental measurements**
  - Temperature: APD, Boards
  - LV, HV
  - APD leakage current
  - Which dynamics and precision for each ?
- **Clock distribution**
  - Which jitter, which tuning step, which modularity
- **Connection with FE and OD**
  - What is our ultimate data volume budget ?

LVR session

Timing session

FE session

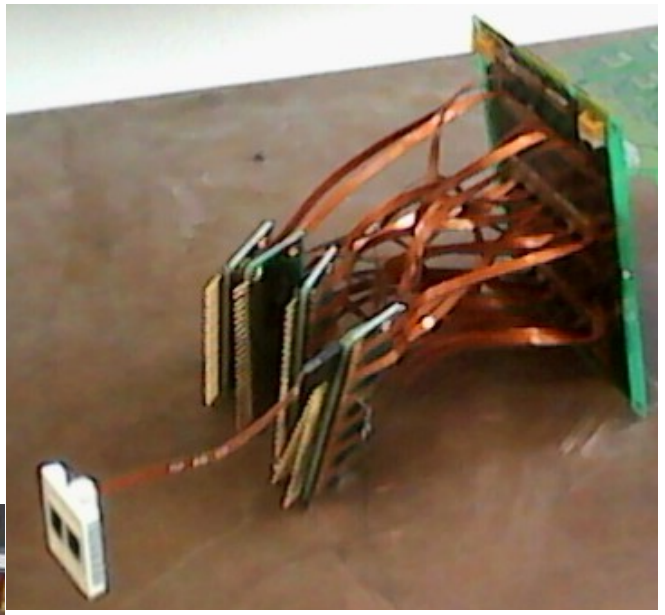
Technology and architecture

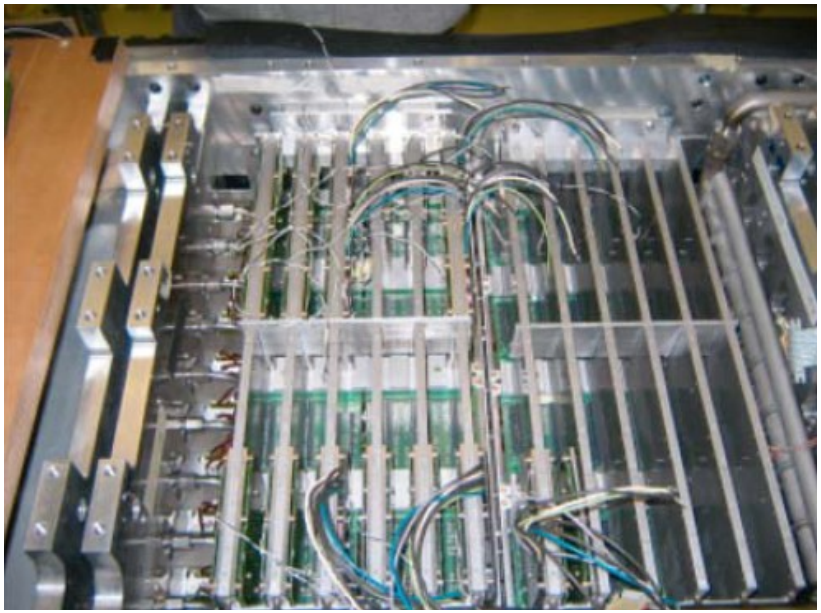
- **Need to define the technology**
  - **TSMC 130 nm / Other ?**
  - **Do we really need 130 nm ? What about 250 nm ?**
  - **If we go with QIE, need bi-cmos techno. Does it exists ?**
- **Need to define chips bounds and modularity**
  - **How many channels/chip ? separate ADC ?**
  - **What are the available IP blocks (PLL, I2C, ADC, ...)**
- **Board**
  - **Past experience showed that this item is very tricky to maintain performances with increasing size, from single channel to SM.**
  - **More complicated here since the degrees of freedom are less**
  - **EMC studies/simulation**
- **System**
  - **Use APD-MB connection characteristics at early stage of preamp design.**

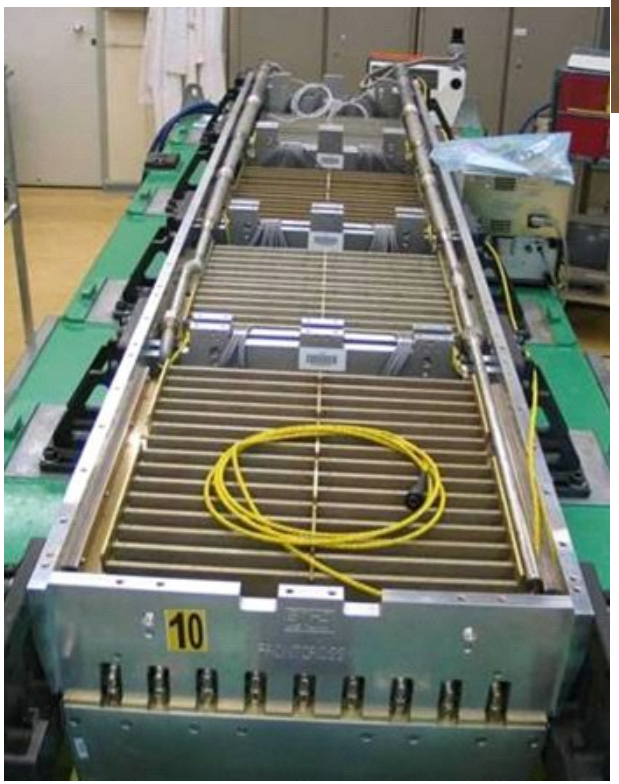
Engineering session

Physical

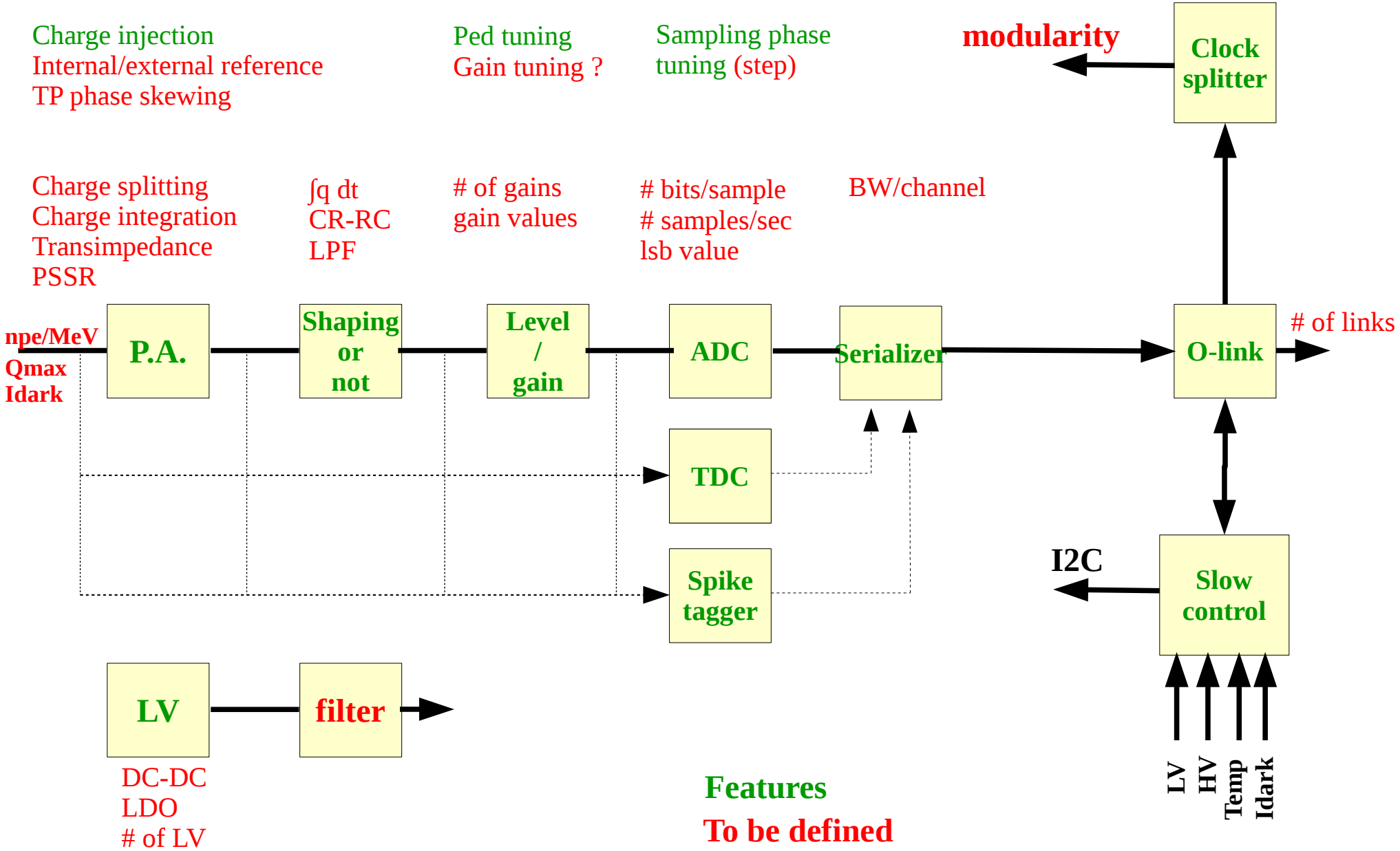
- **Should fit in existing SM mechanics**
  - **Cooling bars**
  - **Mother boards**
    - ► **No access bellow !**
    - ► **No crystal dismount**







All in 1 sketch



Conclusion

- **Lot of questions !**
- **Now, place for answers**
- **I expect to replace some/lot “red” sentences by the end of the workshop**
  - **Lot of parameters have to be fixed before engineering process start**
  - **Lot of knowledge/numbers already known and presented ere and there. Will be summarized in the forthcoming presentations.**