CMS HL-LHC
EM Calorimeter Upgrade

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ECAL barrel Phase 2 Upgrade
Requirements

- Trigger rate up to 750 kHz
  - Legacy max ~150 kHz
- Trigger latency up to 12.5 us
  - Legacy max ~5 us
- Full installation during LHC Long Shutdown 3
- Maintained or improved reliability and availability
- Improved ECAL spike detection and mitigation
- Front End specific
  - Magnetic field tolerant (4T)
  - Radiation tolerant ~5Mrad (1 Mrad expected)

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High on the wish list

- **Re-optimize front end ASIC parameters in order to maintain performance despite crystal and APD degradation due to radiation damage**
- **Decrease the physical volume required for services on YB0**
  - **E.g. by decreasing the Low Voltage Current delivered to the Front End and thus use thinner or less cables**
  - **E.g. by decreasing power consumption in the front end and thus use thinner cooling lines**
- **Review front end grounding and shielding scheme in order to make the system less sensitive to EMI**
- **Solid failure mitigation scheme**
  - **E.g. avoid dependence between neighbours**

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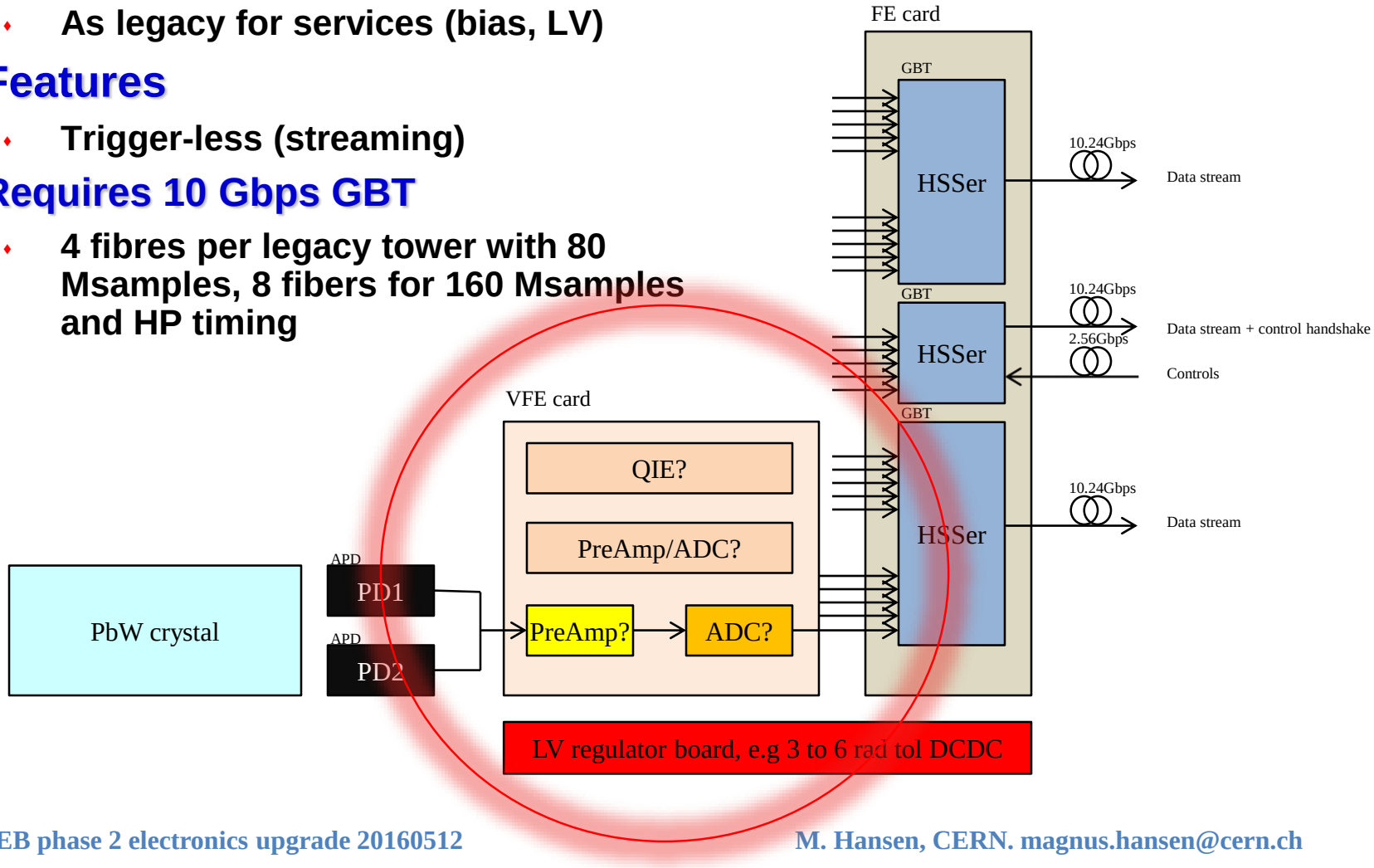
Phase 2 ECAL Barrel FE electronics system - Design idea

- **Modularity**
  - 1 channel for readout and trigger
  - As legacy for services (bias, LV)
- **Features**
  - Trigger-less (streaming)
- **Requires 10 Gbps GBT**
  - 4 fibres per legacy tower with 80 Msamples, 8 fibers for 160 Msamples and HP timing



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External constraints

- **YB0 and YE1+- services will be completely removed early in LS3**
  - **Cables, fibres and pipes cut in 1m pieces by a team without silk gloves and discarded**
- **As a consequence essentially all cables between UXC55 and USC55 will have to be replaced**
  - **Essentially fibers and HV cables for the EB**
- **One full year for 36 Supermodule removal, re-work, and re-installation**

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Internal constraints

- **Modularity**
  - 25 readout channels organized as 5 phi strips
  - APD and low voltage connectors fully defined
- **VFE and LVRB form factor known**
  - 3D limits including hard connection to cooling system
  - Motherboard (APD) connector fully defined
  - Need good reasons to change the FE connector
- **FE form factor known**
  - 2D limits
  - Again, need good reasons to change the VFE connector
- **Power budget within legacy limits, essentially 2W per channel; Goal perfectly within reach is 1W per channel**

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External aid

- **Applicable and useful common developments**
  - **lpGBT @ 10.24 / 2.56 Gbps**
    - ➔ Development ongoing, cost estimated to 35 CHF
  - **Versatile link +**
    - ➔ Development ongoing, cost estimated to 100 USD per connection (rad hard optics plus fiber, OD parts excluded)
  - **Low voltage regulator**
    - ➔ Radiation and magnetic field tolerant DCDC converter in production, development of enhanced ASIC ongoing, module available for 35 CHF
  - **Radiation tolerance qualified tool kit for TSMC 130nm and 65nm available**
    - ➔ Including e.g. eLink macros for ADC – GBT integration

- **CMS ECAL may want to contribute to these multi-institutional / multi-national projects**

Development Timeline

- **Kick-off about a year ago**
- **This workshop**
  - **Essentially about VFE specification and strategy for technology selection**
- **Comprehensive review June 2016**
  - **Essentially a report from this workshop and current actions**
- **December 2016**
  - **Baseline VFE design**
  - **Demonstration of FE DCDC power feasibility**
- **September 2017**
  - **TDR**
  - **Here we have to demonstrate that we know what we need, what to do and that the resources are sufficient to deliver the project on time**

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LpGBT

- **Down-link: 2.56 Gb/s (64 –bit frame)**
  - **User bandwidth with FEC12: 1.44 Gb/s or 36 bits / 40MHz clock**
- **Up-link: 10.24 Gb/s (256 –bit frame)**
  - **User bandwidth**
    - ➔ **FEC12: 8 Gb/s**
    - ➔ **FEC5: 9.13 Gb/s**
- **Phase/Frequency programmable clocks**
  - **4 independent clocks with 50ps phase resolution**
  - **Frequencies: 40 / 80 / 160 / 320 / 640 / 1280 MHz**

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LpGBT

- **ASIC control: IC channel: 80 Mb/s**
  - **I2C interface**
    - ➔ **LpGLD control:I2C master**
- **Experiment control: EC channel: 80 Mb/s**
  - **Two I2C masters**
  - **Programmable parallel port:16 x DIO**
  - **Environmental parameters monitoring**
    - ➔ **10-bit ADC with 8 inputs**
    - ➔ **Temperature sensor on chip**
    - ➔ **Programmable current source to drive an external temperature sensor**
- **Replaces the current GBT-SCA**

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Link and bit counts

- **eLinks FEC5 @ 10.24 Gb/s**
  - **Bandwidth: 320 / 640 / 1280 Mb/s**
    - ➔ 8 / 16 / 32 bits per 40 MHz clock
  - **# eLinks*: 28 / 14 / 7**
- **eLinks FEC12 @ 10.24 Gb/s**
  - **Bandwidth: 320 / 640 / 1280 Mb/s**
    - ➔ 8 / 16 / 32 bits per 40 MHz clock
  - **# eLinks*: 24 / 12 / 6**
- **eLink Macro exists for TSMC 130nm and 65nm**

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Link and bit counts

- **Three 10 Gbit up-links would allow 24 (26) bits per channel**
  - Three 320 Mbit Elinks
  - 11 (12) bits ADC plus gain flag @ 80MHz. Enough?
  - Requires e.g. one 3+1 versatile link+ module per FE (foreseen)
- **Four 10 Gbit up-links would allow 32 (34) bits per channel**
  - Four 320 Mbit or two 640 Mbit or one 1280 Mbit Elinks
  - 15 (16) bits ADC plus gain flag @ 80MHz. Better?
  - Requires e.g. one 4+1 versatile link+ module per FE (foreseen)
- **Six 10 Gbit up-links would allow 48 (52) bits per channel**
  - Six 320 Mbit or three 640 Mbit Elinks
  - 11 (12) bits ADC plus gain flag @ 160MHz.
  - 15 (16) bits ADC plus gain flag @ 120MHz.
  - Requires e.g. two 3+1 versatile link+ module per FE
    - ➔ Only one FE control link would be used; the other receiver used for precision sampling clock?

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VFE to FE Data transmission

- **Implement a number of eLinks in every ADC / QIE for data streaming**
  - **A few idle characters required in order to word-align at reception in the off detector electronics**
    - ➔ **E.g. upon BC0 reception; note that the arrival time of the BC0 needs to be skewed together with the clock or at least dealt with**
    - ➔ **Imagine e.g. an all zeros – all ones – all zeros transition as ADC response to the BC0**

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LVRB replacement

- **A radiation and magnetic field tolerant ACDC power module has been developed which meets, a priori, our electrical requirements**
  - **Investigate noise levels with an initial demonstrator; essentially done**
  - **Verify behavior in radiation and magnetic field; started**
  - **Develop LVRB respecting the mechanical requirements; first version essentially ready**

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Bulk power system

- Essentially all LHC upgrade projects are planning to use DCDC POL converters in or close to the front end system
- The DCDC converters developed to date allow up to 12V input, essentially non-regulated.
- A common project, similar to the legacy, is started in order to investigate the feasibility of operating COTS bulk power supplies
  - In the service cavern
    - ➔ Radiation level as essentially zero
    - ➔ Magnetic field 50 – 100 Gauss
  - In the experimental cavern, e.g. X0
    - ➔ Radiation level as essentially as in service cavern
    - ➔ Magnetic field 200 – 400 Gauss; balconies essentially excluded: up to 1200 Gauss

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Bias (HV) power system

- **Essentially, the requirements have not changed, thus the HV power system can be maintained.**
  - **The key word is “maintained” rather than “kept”**
  - **The complete system will very likely need to be renewed purely due to age**
- **Profit from the complete YB0 de-installation to review the grounding and shielding implementation in order to become less sensitive to EMI**

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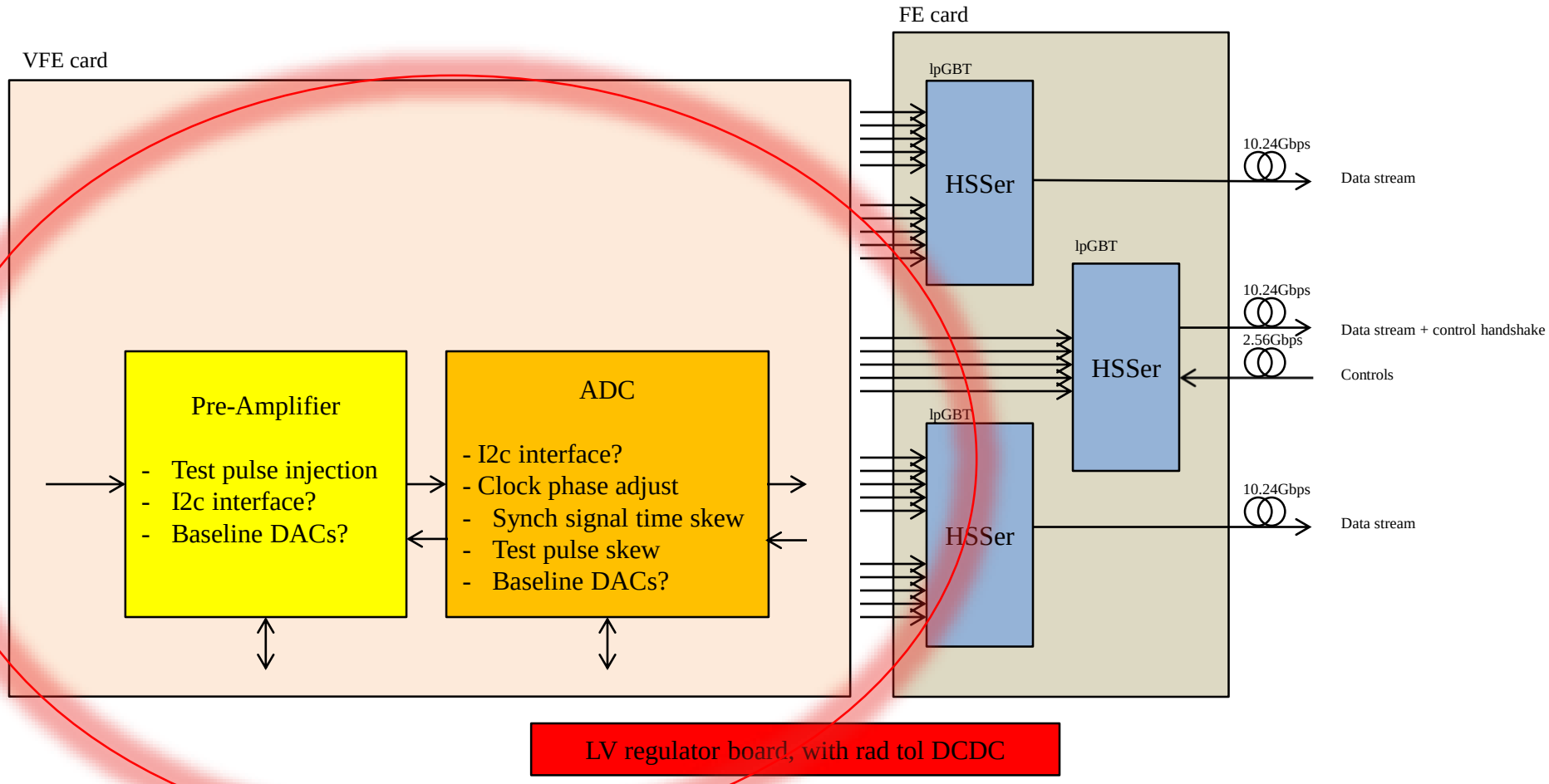
Phase 2 ECAL Barrel FE electronics system



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End

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Backup

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FE clock distribution

- **Option 1**
  - **Use the (non-skewable) eLink clocks as the only clock in the ADC / QIE (sampling, internally multiplied for eLink transmission)**
  - **Implement a clock skew function in each ADC in order to align sampling to beam**
    - ➔ **Requires a control interface, e.g. i2c**
- **Option 2**
  - **Develop a clock fan-out chip with a clock skew function for each output**
    - ➔ **Here, the ADC is somewhat (but not much) simpler but an additional ASIC is required**
- **Option 1 appears attractive as it safely solves essentially all problems with a smaller number of ASICs**

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