VFE asic considerations

Saclay's Upgrade Workshop

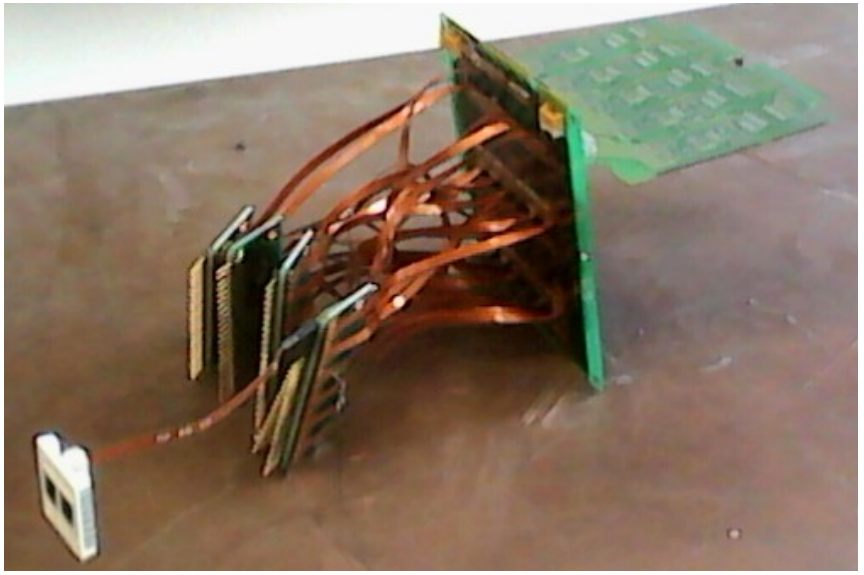
Marc Dejardin
CEA-Saclay Irfu/SPP

Reminder

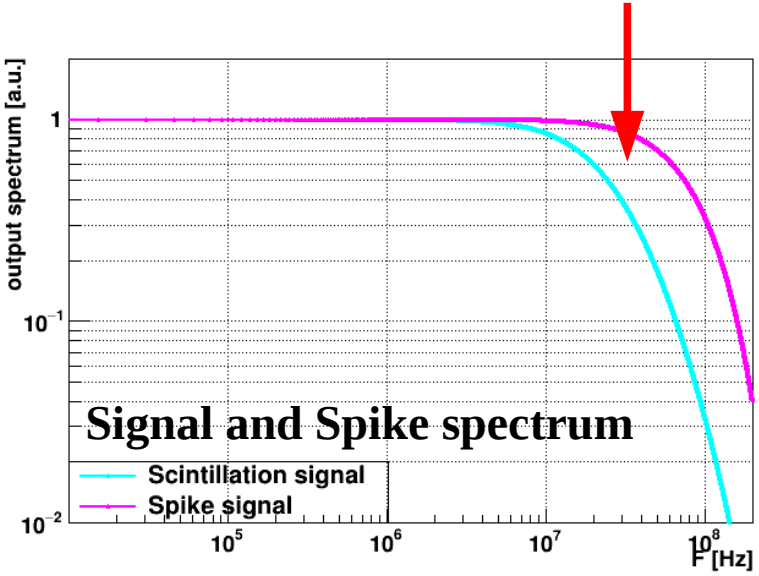
- **For HL-LHC upgrades**
  - **Keep energy measurement as good as possible**
  - **Improve spike tagging**
  - **Mitigate APD leakage current increase**
  - **Mitigate OOT pileup**
  - **Mitigate IT pileup**
- **Guidelines**
  - **Get shaping time as short as possible**
    - ► **OOT pileup, leakage current induced noise**
  - **Get amplification chain BW as high as possible**
    - ► **Increase signal information**
      - **Spike tagging, timing information**

Integration in existing system

- Mother board kaptons (d = 130 mm)
  - R_{MB} = 53 mΩ/cm
  - L_{MB} = 4.5 nH/cm
  - C_{MB} = 2.4 pF/cm
- APD capsule kaptons (d from 70 to 165 mm)
  - R_{APD} = 35 mΩ/cm
  - L_{APD} = 2.4 nH/cm
  - C_{APD} = 1.7 pF/cm
- LC resonator with APD capacitance (160 pF)
  - Resonance frequency ~40 MHz
  - Electronic Bandwidth upper limit
- Ultimate performances limited by the system



The discriminating information is there

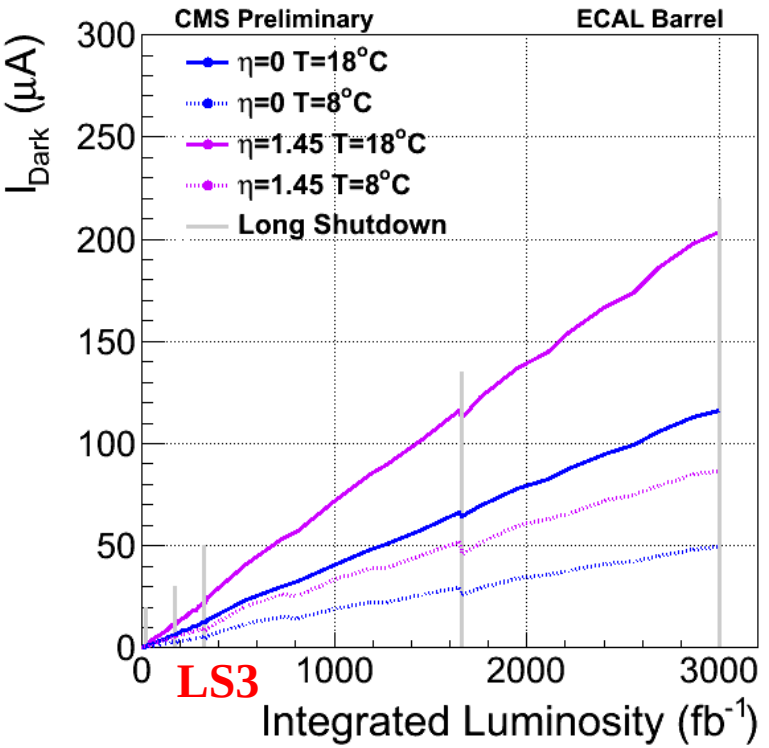


APD considerations

- **APD: reverse biased diode**
  - **Current source**
  - **Signal: photon induced variation of reverse current**
  - **Noise: random variation of reverse current = f(I_{leak})**
    - $\tilde{i}_{APD} = 5.4 \sqrt{I_{leak}}$ [pA/√Hz] (I_{leak} in uA, M=50, F=2)
    - Equivalent of noise generated by $R_{eq} = 525/I_{leak}$ Ω
  - **Bandwidth: unknown but large**
    - Well above connection cutoff frequency
  - **Capacitance: ~160 pF**
  - **Connection line (kapton):**
    - C_{kapton} = 40-60 pF from M1 to M4
    - L_{kapton} = 75-100 nH from M1 to M4

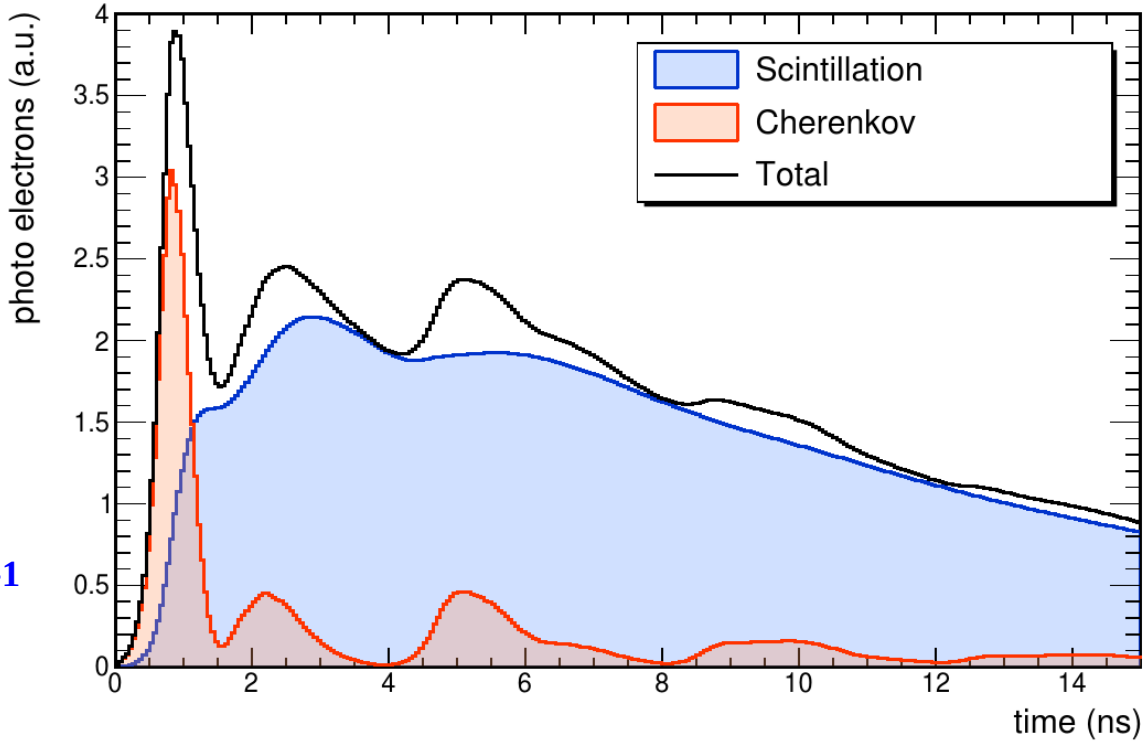
Leakage current

- **HL_LHC start (300 fb-1):**
  - **10-20 uA (18°C) 5-10 uA (8°C)**
- **HL_LHC end (3000 fb-1):**
  - **100-200 uA (18°C) 50-110 uA (8°C)**
- **VFE should be efficient for all scenarios**
  - **First year of HL-LHC perhaps not at full lumi...**



Signal shapes and level

- **Spike: Dirac energy deposition in APD core**
  - **~ isolated crystal**
  - **In time and out-of-time wrt LHC collisions**
- **Scintillation: Follows photon arrival on APD**
  - **4.5 p.e/MeV w.o. loss**
  - **3.5 p.e./MeV @ 300 fb^{-1}**
  - **2.8 p.e./MeV @ 3000 fb^{-1}**
  - **+30 % @ 8°C !**



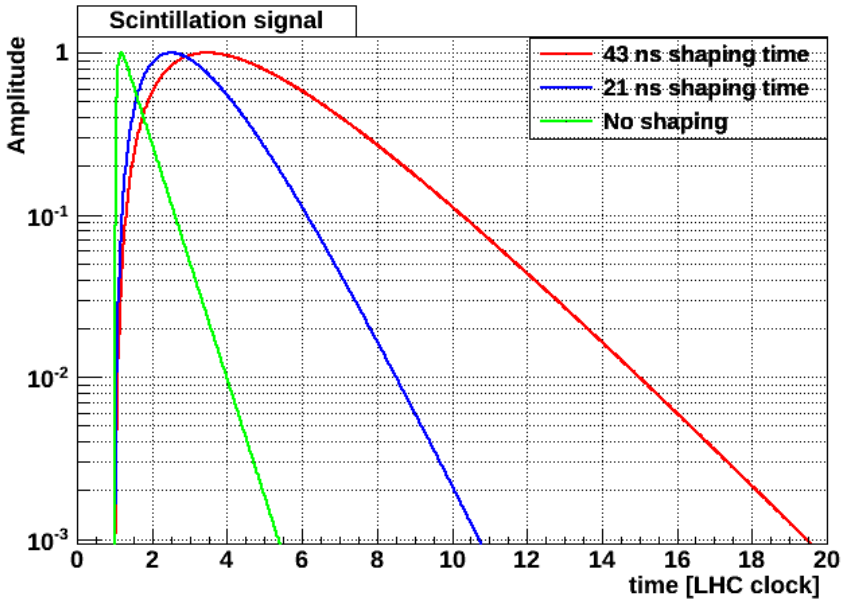
- **Shape analysis to discriminate**
  - **On analog signal**
  - **On sampled signal**

VFE asic requirements

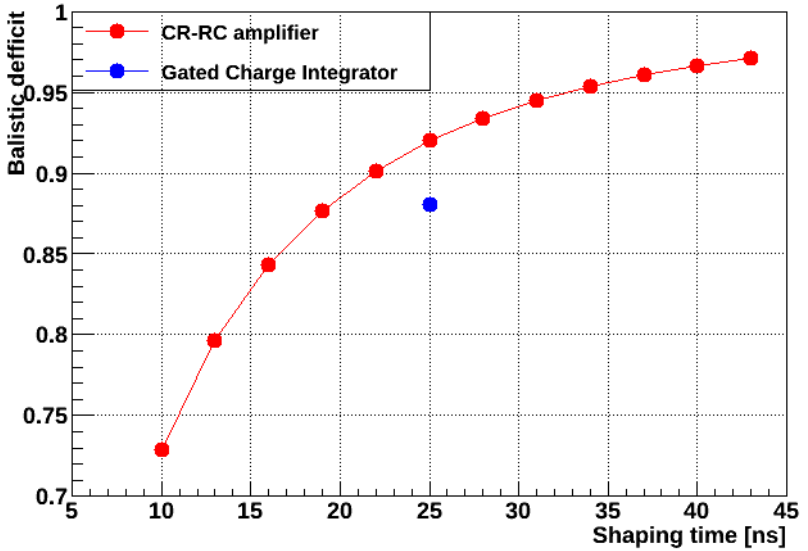
- **Dynamics:**
  - From APD induced noise (100 MeV ?)
  - Up to 2 TeV
    - ► 14.3 bits
- **Number of gains**
  - Depends on ADC choice
  - 2 gains (x10, x1) seems enough (with 12 bits ADC)
- **Linearity**
  - No real constraint but present MGPA is quite good
    - ► Could be taken as reference: +- 0.1 %
- **Shape stability (with time, with amplitude)**
  - Should be good enough for
    - ► Multifit performances and timing measurements
    - ► To be quantified

Shaping time

- **Shorter**
  - **Less OOT contamination**
  - **Less integration of leakage current fluctuations**
    - ► **Less noise**



  - **But less integration of signal charge**
    - ► **Less mV/fC**
    - ► **Not relevant for TIA**

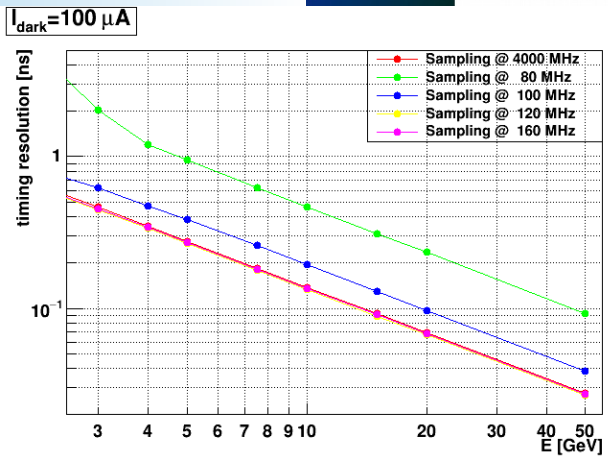


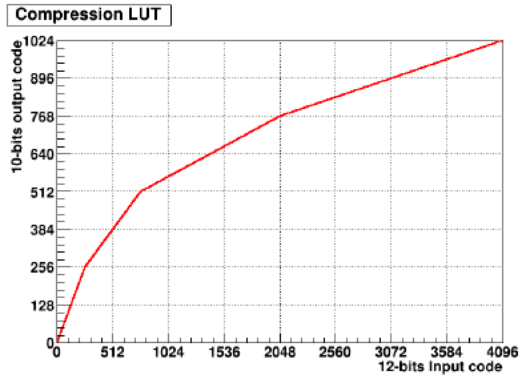
VFE options

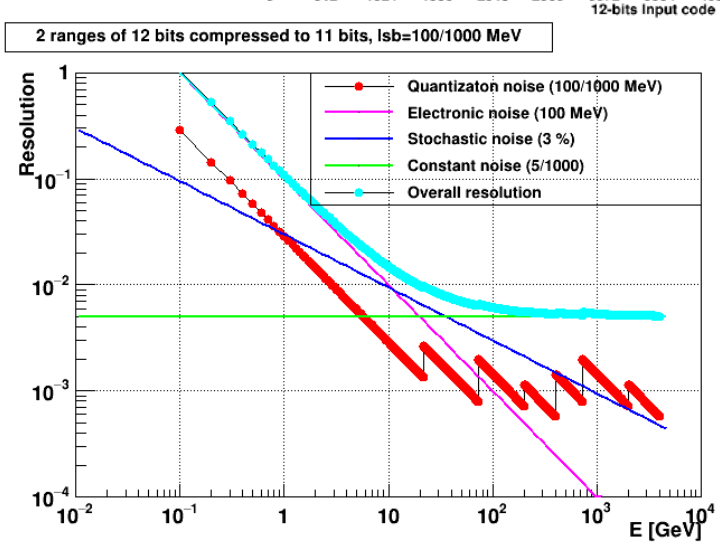
- **MGPA++ : MGPA evolution**
  - **New technology**
  - **Reduce shaping time**
  - **Extra features (spike tagging)**
- **TIA**
  - **Image of APD current, BW limited (~35 MHz)**
  - **TSMC 130nm technology**
  - **Extra features done in OD (spike tagging, TDC, filtering)**
- **QIE++ : QIE evolution**
  - **Gated charge integrator, gate width to be defined**
  - **Bi-cmos technology**
  - **Enhanced ADC wrt QIE13**
  - **Extra features (tdc)**

ADC options

- With shorter shaping
  - Oversampling mandatory
    - For OOT pileup mitigation (multifit over-constraining)
    - For shape analysis (spike tagging)
    - For IT pileup mitigation (timing)
    - 80, 160 MHz ?
  - Drawback : More data to transmit
- Digitization noise should be negligible wrt other contributions
- Should include extra feature for versatility
  - Output look-up table for compression
  - Gain switching behavior
  - Sampling phase tuning
- Architecture à-la ADC41240 has proven its robustness
  - Could be taken as baseline design







VFE options comparison

- **Define case studies for comparison**
  - **@ 300 fb^{-1}, 1000 fb^{-1}, 3000 fb^{-1} and 5000 fb^{-1}**
  - **With 0, 100, 200 PU**
- **Electronics performances**
  - **Noise**
  - **Spike tagging efficiency**
  - **Timing resolution**
  - **Data volume**
  - **Development risk**
- **Options**
  - **Sampling rate**
- **Inputs and tools**
  - **Shapes and PU from toyMC (tuned with TB results)**
  - **APD noise model from measurements**
  - **Electronic noise from simulation**
- **Physics performances ?**
  - **Hgg with PU**
  - **gg vertexing**
  - **X(750)gg**

Conclusion

- **Still lot of questions and options**
- **Let's hear more details on various options**