Trans-**I**mpedance **A**mplifier solution for VFE upgrade

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Outline

- TIA solution
- TIA architecture
- Performances
- Status & Planning
- Conclusion

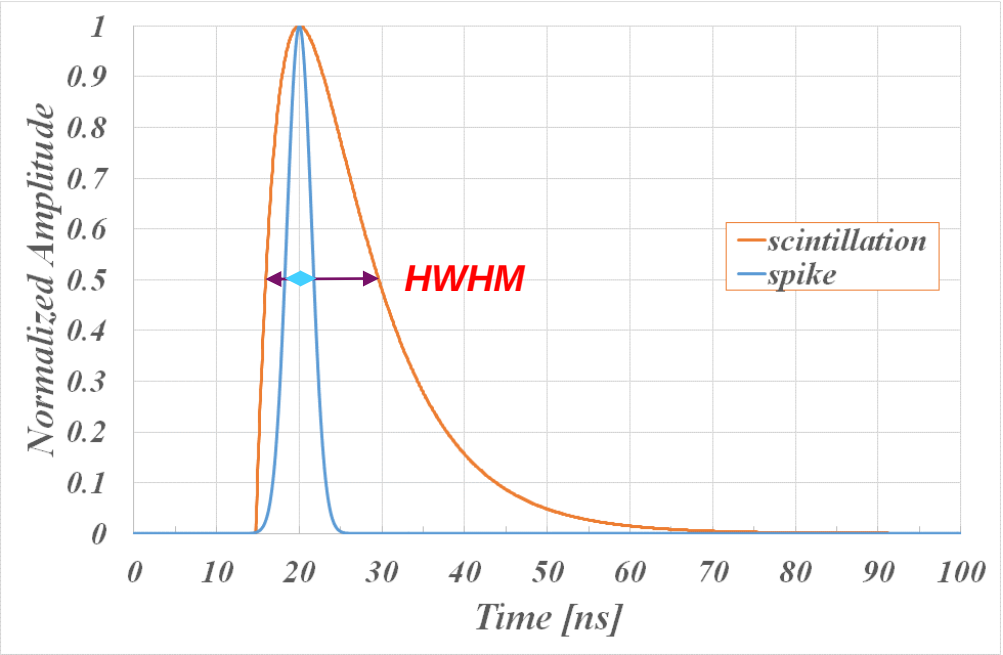
TIA solution

TIA solution comes from Marc Dejardin works

- Work on the APD signal shape which provide the best information to cope the upgrade requirements:

  TIA + BW 50 MHz + 12-bit ADC at 120/160 MHz

- Online spike tagging by shape analysis (***HWHM****)
- Offline energy reconstruction with Pileup
- Allows best timing resolution



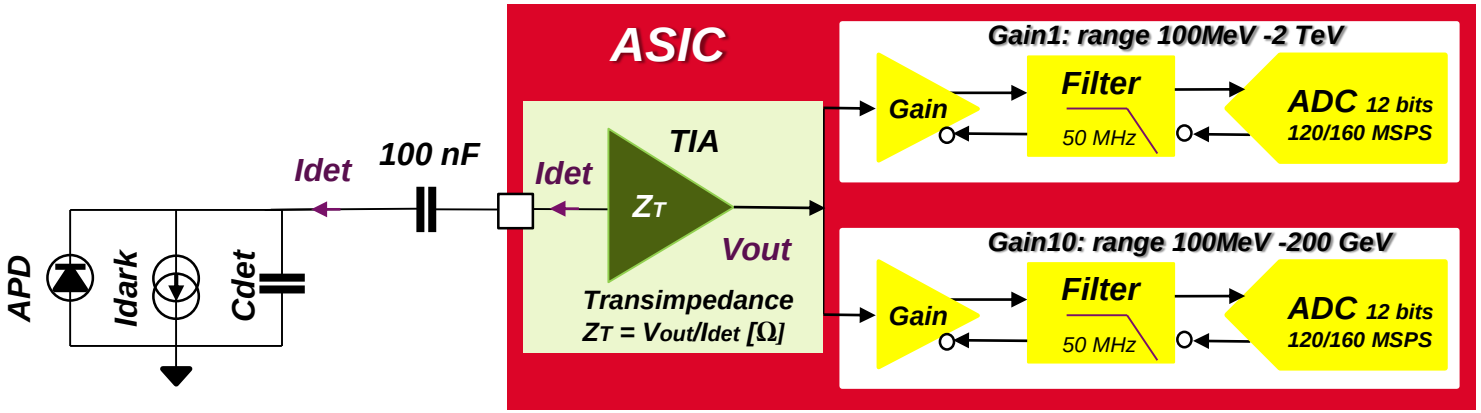
Freedom to tune algorithm to follow detector aging & unforeseen “features”

*Half Width at Half Maximum

ASIC architecture

TIA ASIC architecture

- 1 TIA for 2 Gains called G1 & G10
- ***G1***: 100MeV – 2 TeV; ***G10***: 100 MeV – 200 GeV
- 1 Gain: gain + Filter [50 MHz] + 12-bit ADC 120/160 MSPS



Detector

- Cdet = 200 pF
- Ileak from 10 µA to 100 µA
- Crystal: 4.5 p.e/MeV; APD gain: 50 => $Qin_{max.}$ = 72 pC

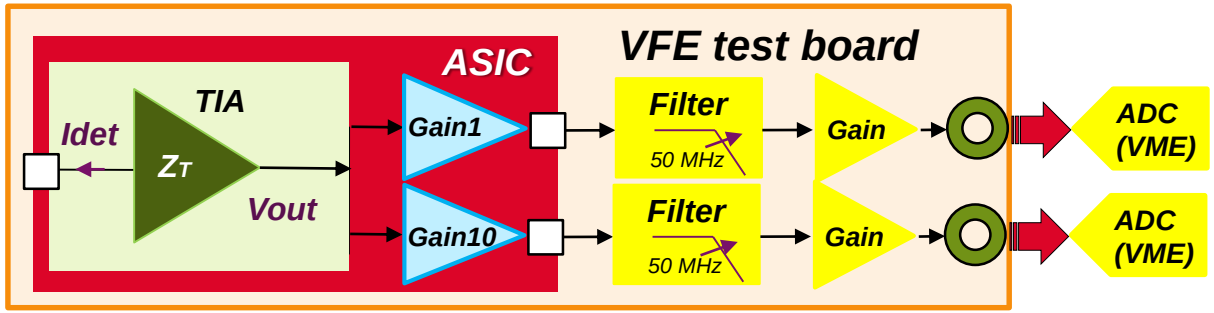
Technology

- TSMC 130 nm [1.2V Core Voltage / 2,5V I/O Voltage]

Prototype architecture

Prototype

- 5 channels: 1 TIA + 2 Gains G1 & G10
- Filtering & Gain on VFE test board
- External ADC: 50 MHz

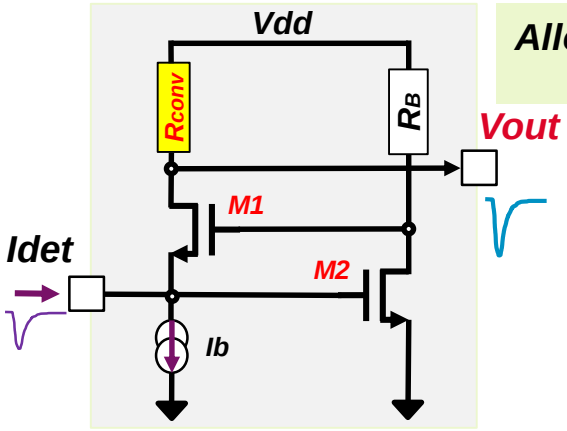


Additional functionalities

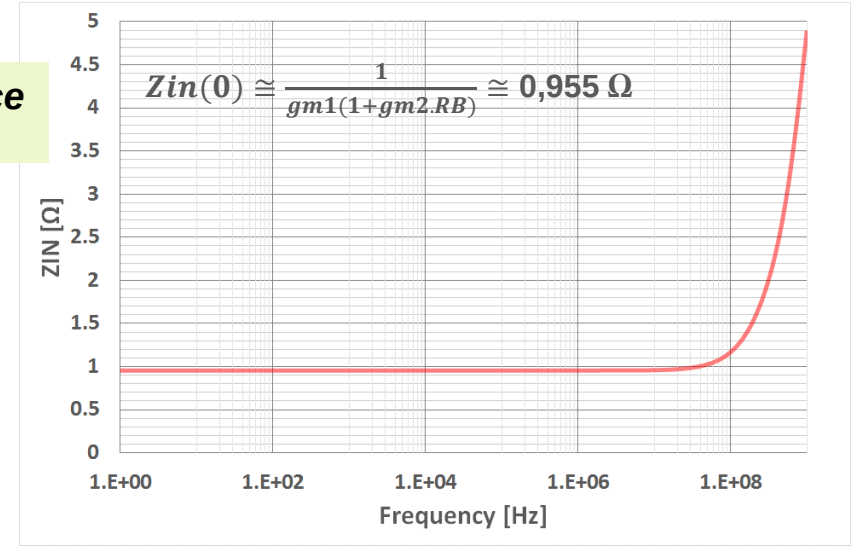
- Additional blocks for technology studies:
  TIA with different gain,
  Gain stage,
  CSA,
  test cells ..

TIA architecture and performances (sim.)

Regulated common-gate

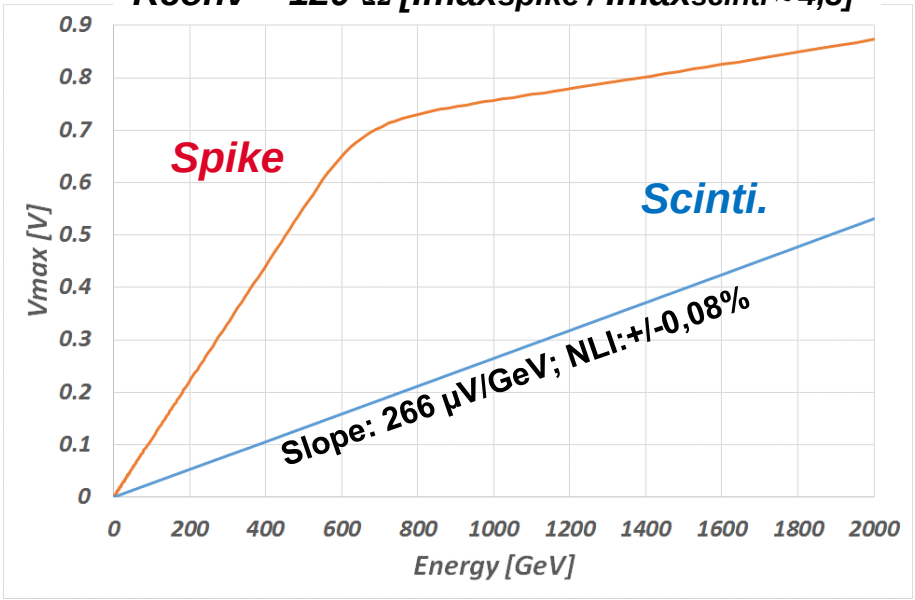


Allows a low input impedance
[Cdet = 200 pF for 50 MHz BW]

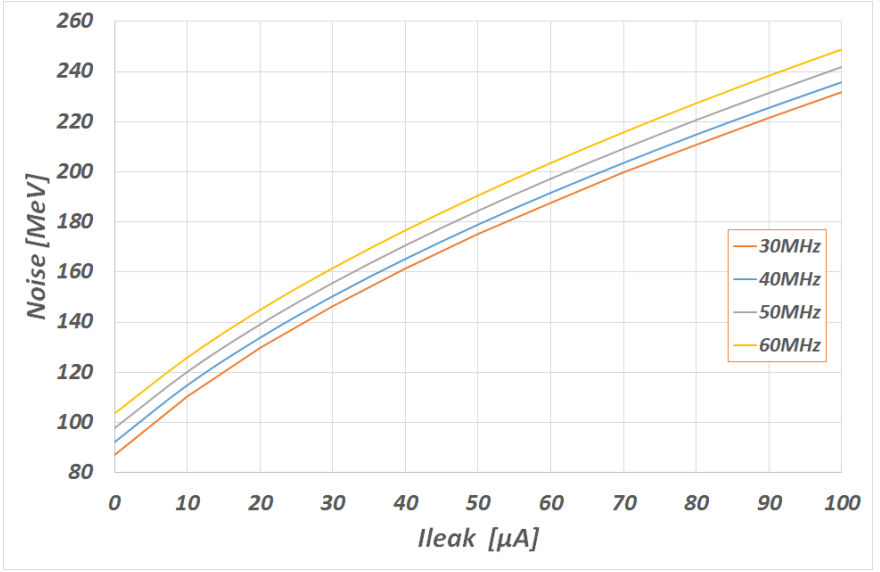


Gain

Rconv = 120 Ω [Imax spike / Imax scinti ≈ 4,3]

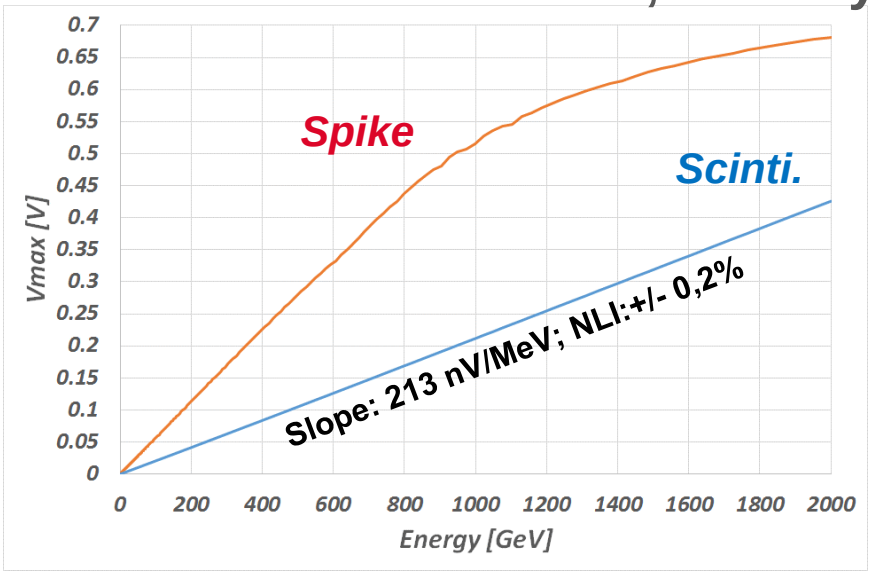


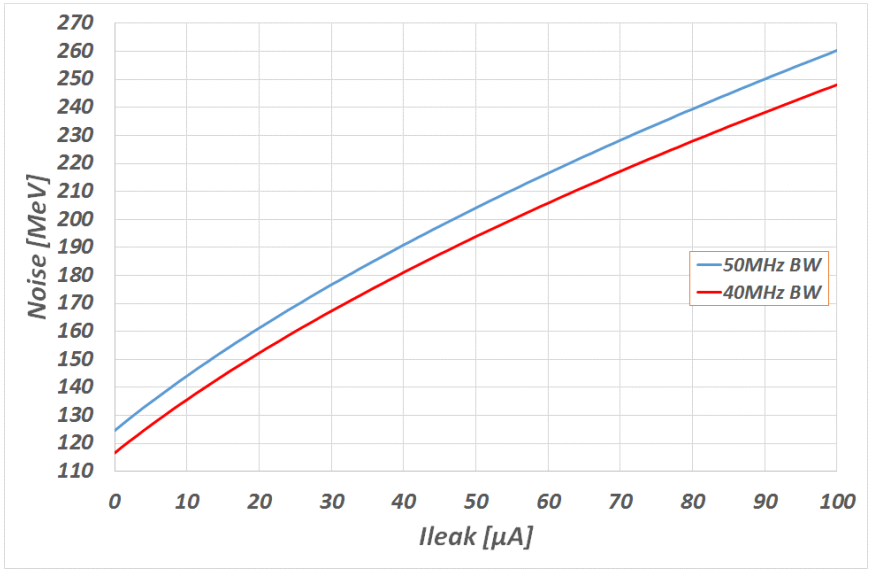
Noise ❑ *Cdet = 200 pF*



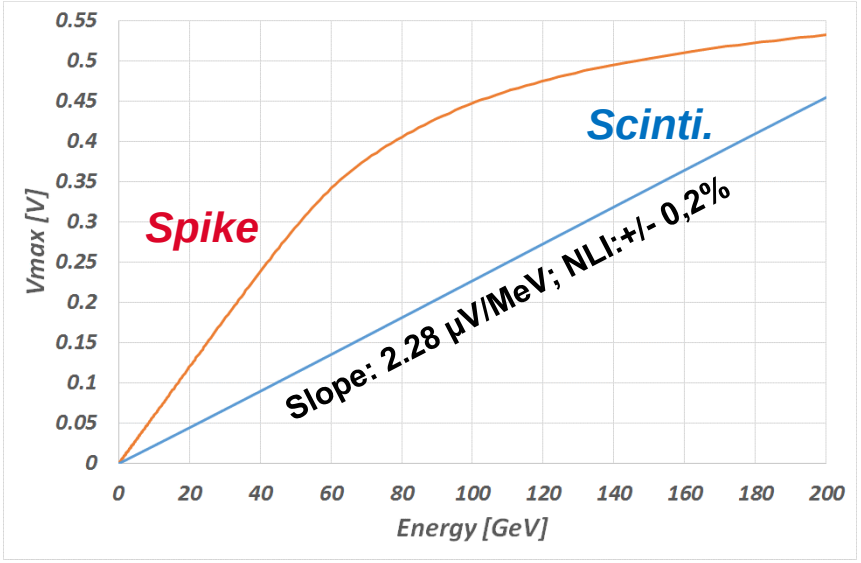
G1 and G10 outputs performances (sim)

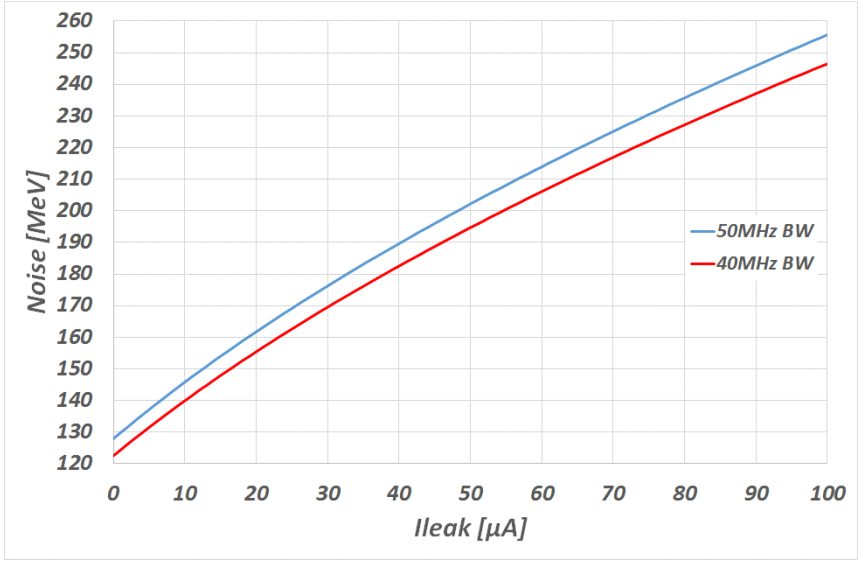
G1: Transfer function, linearity & Noise





G10: Transfer function, linearity & Noise

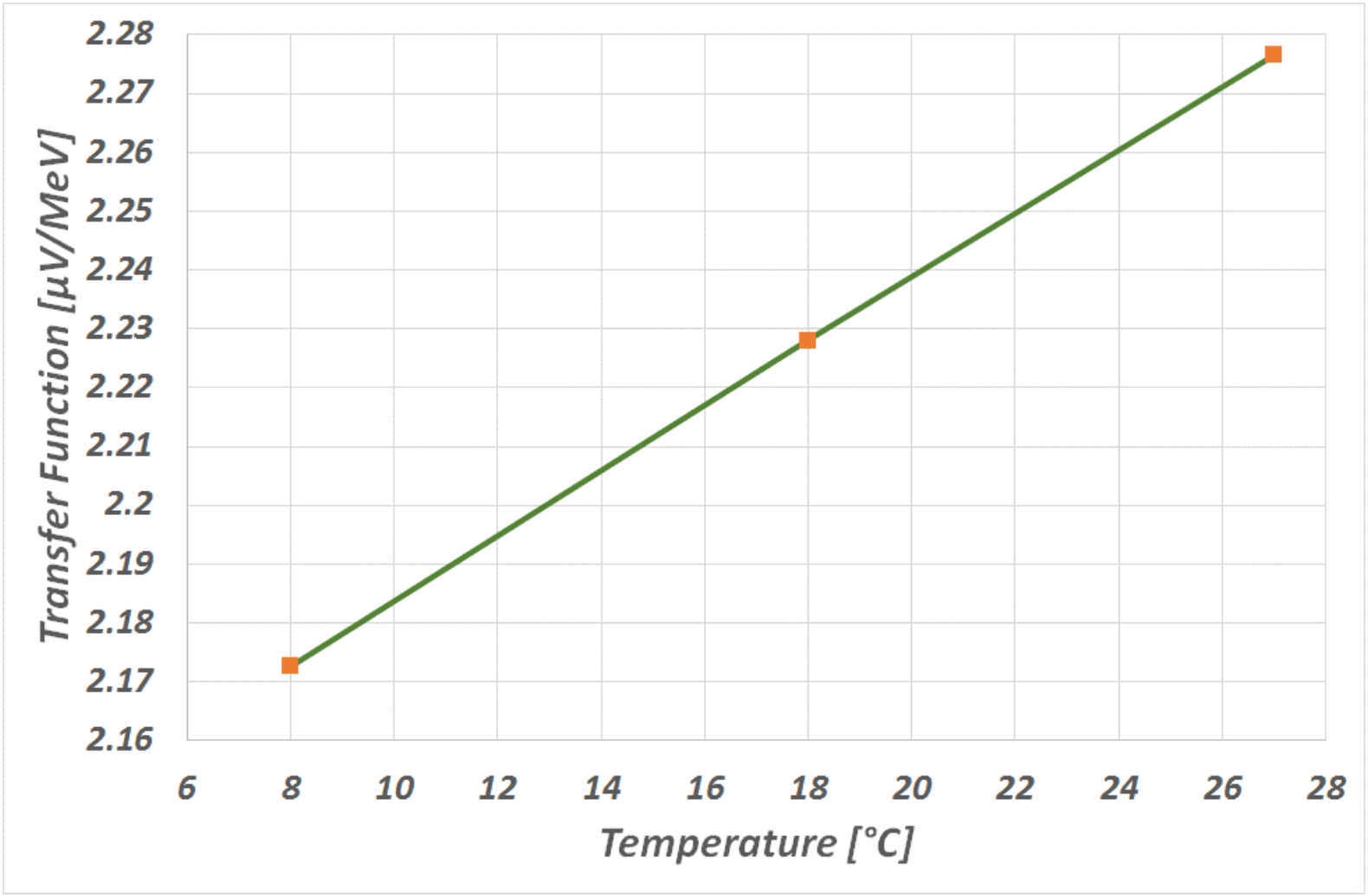




G10 performances (sim.)

Transfer function versus Temperature

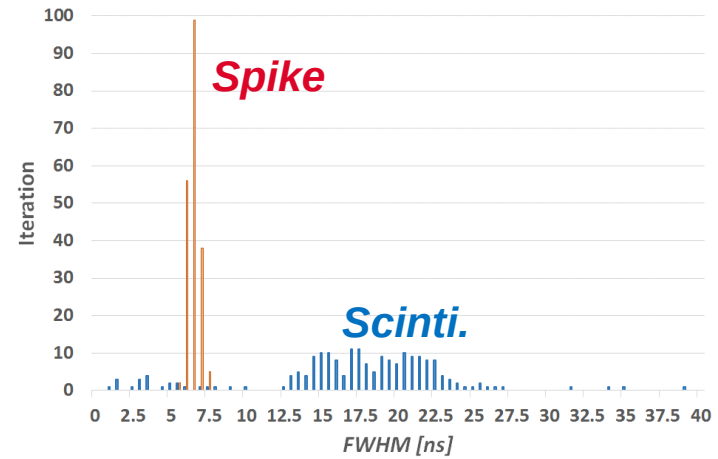
❑ ***Gain vs Temperature:*** *+ 0.23% /°C [APD: - 2(3)% /°C]*



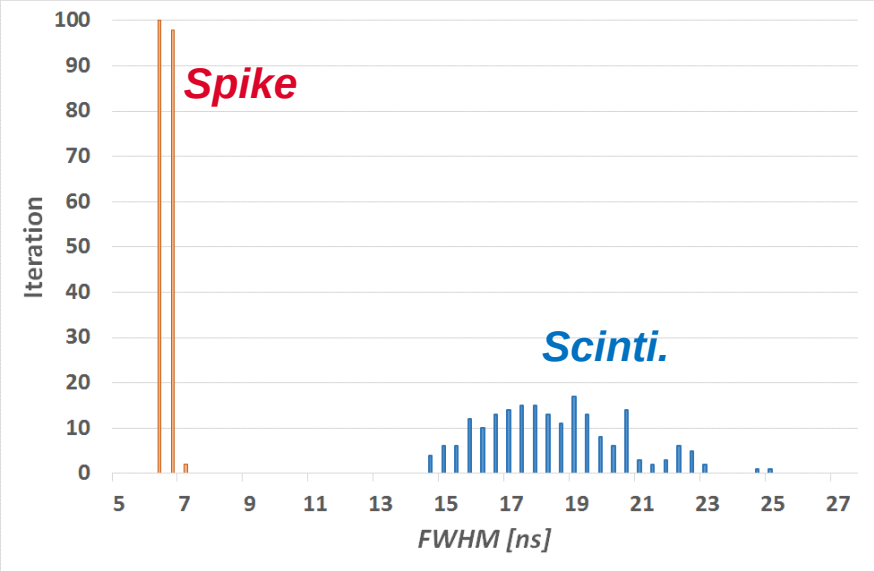
G10 performances (sim.)

- **Spike rejection: Ileak = 100 µA; Cdet = 200 pF**

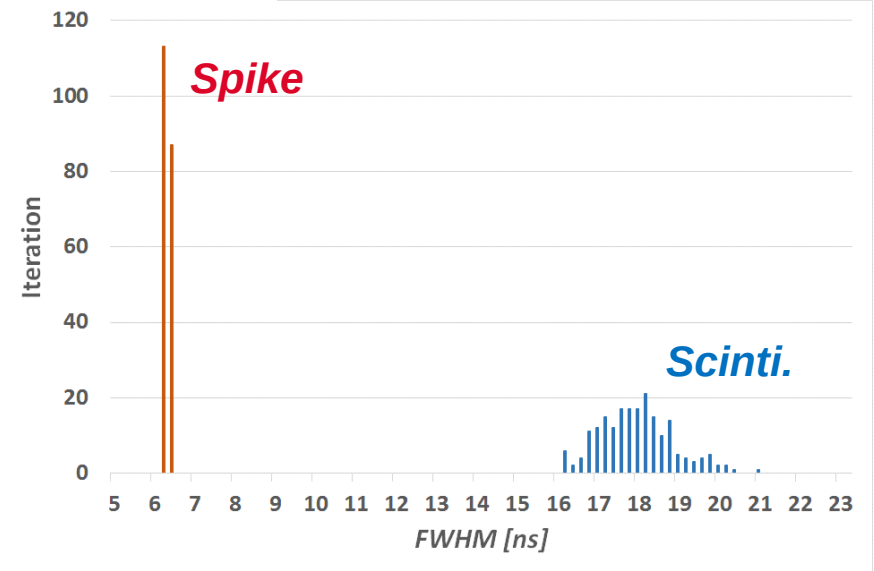
❑ ***E = 1 GeV***



❑ ***E = 2 GeV***

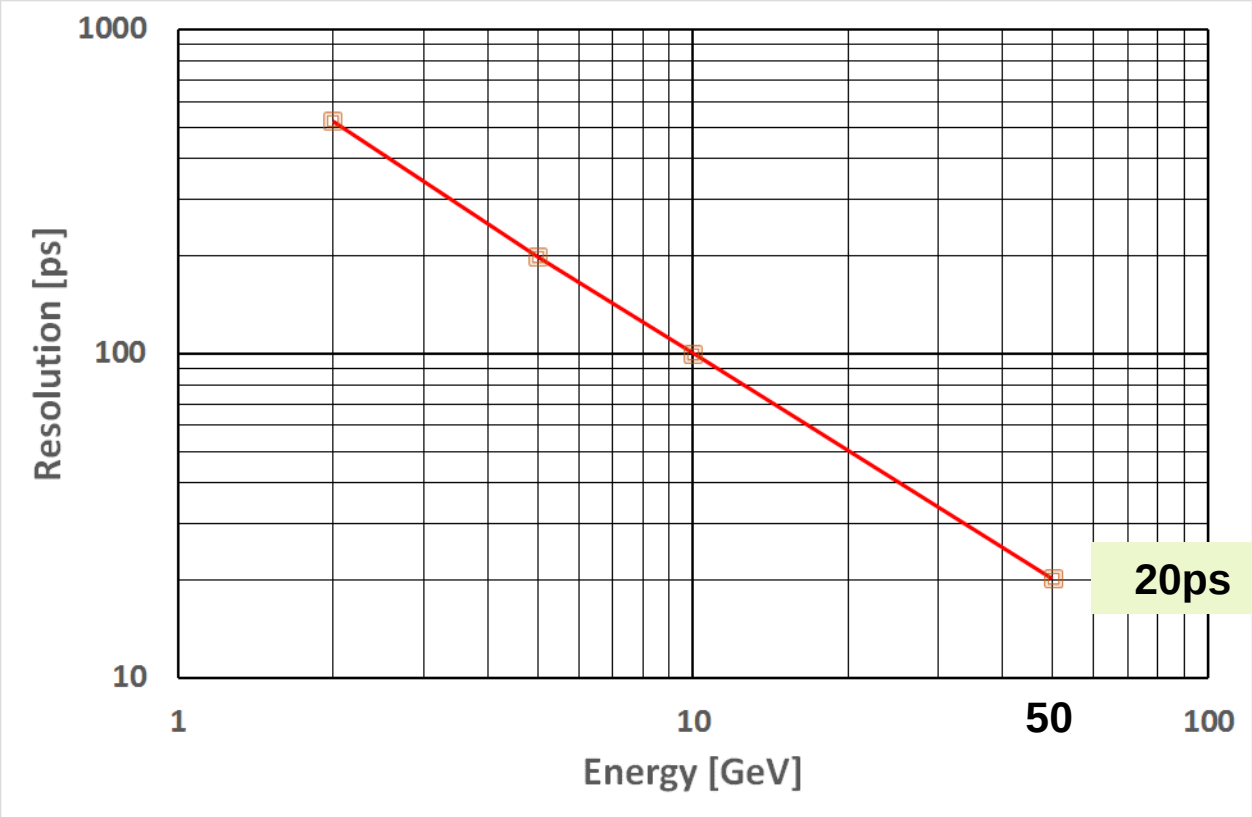


❑ ***E = 5 GeV***



G10 performances (sim.)

- Time resolution: Ileak = 100 µA; Cdet = 200 pF

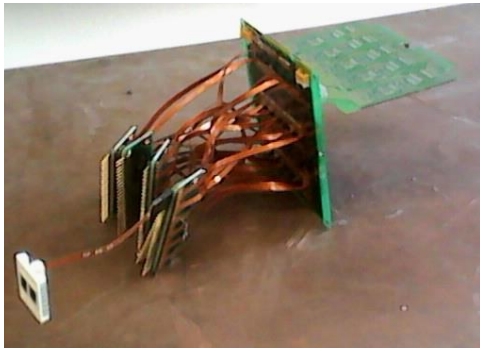


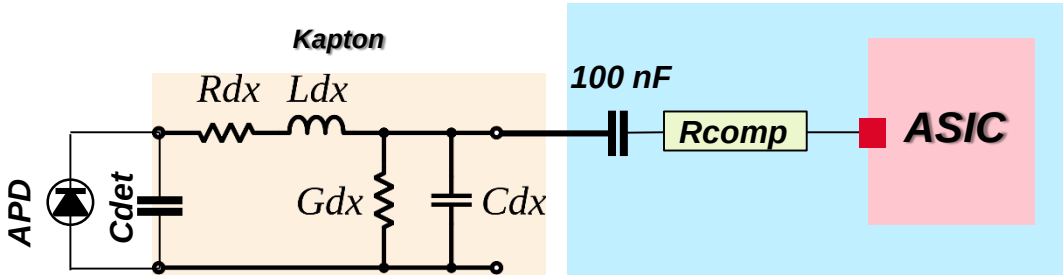
- Power consumption: 63mW (1.2V)

TIA (46mW); G1 (7.9mW); G10 (9.1mW)

System performances (sim.)

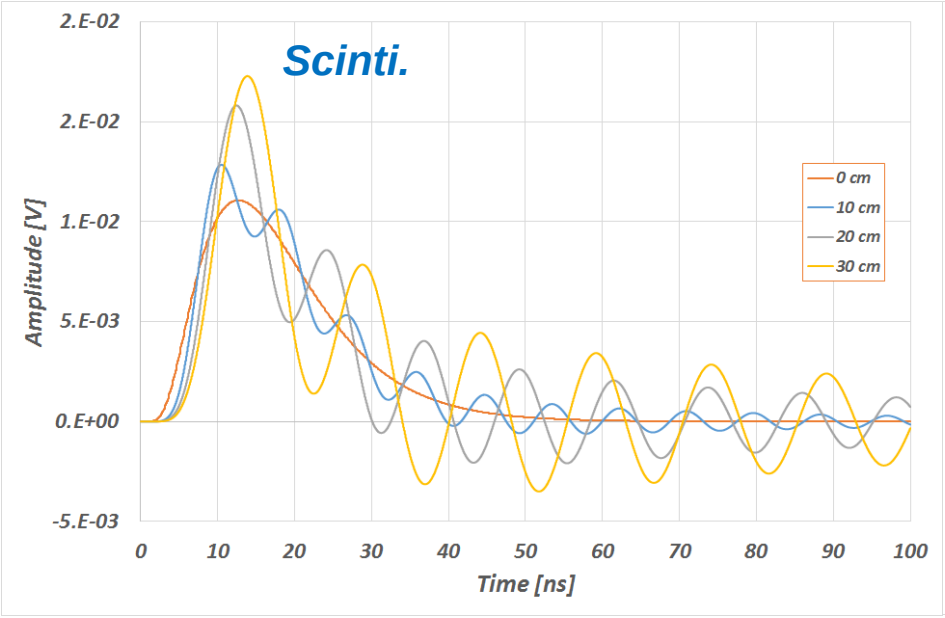
Interface APD – TIA: strip lines

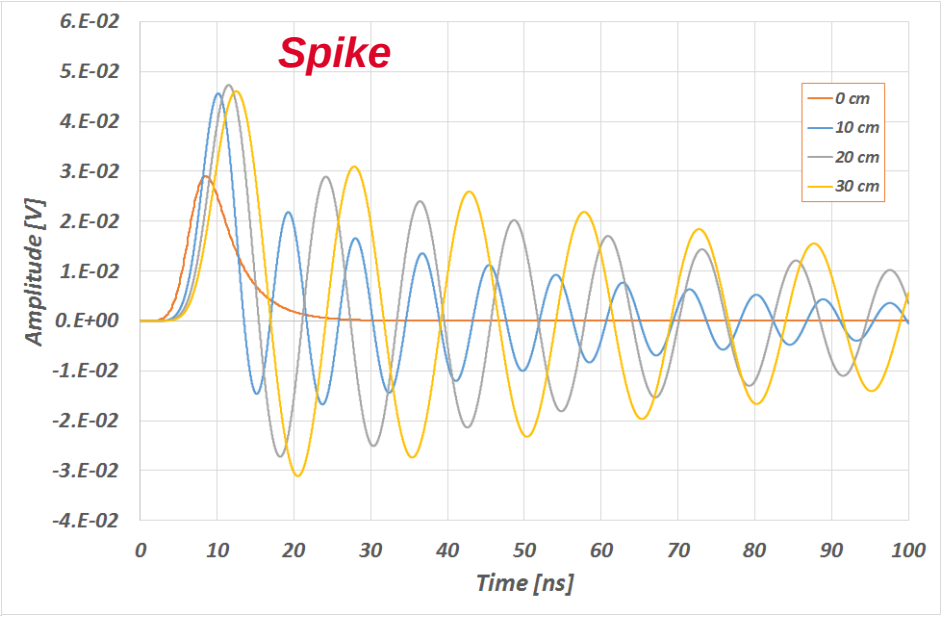




- ***Measured parameters: L = 3,75 nH/cm; R = 0,05 Ω/cm; C = 2,4 pF/cm***
- ***Length 20 – 30 cm => 75 – 100 nH !!***

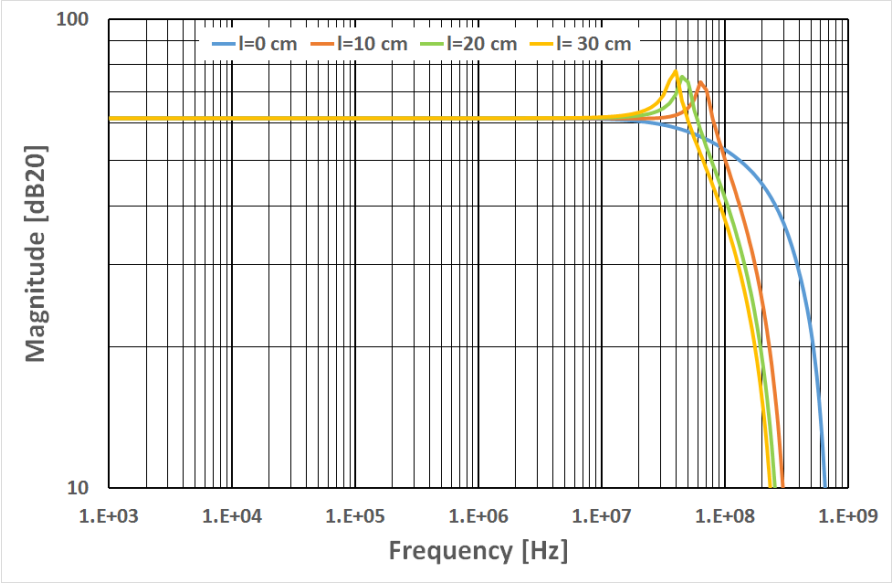
Effect of the length: *Signal E=5GeV*

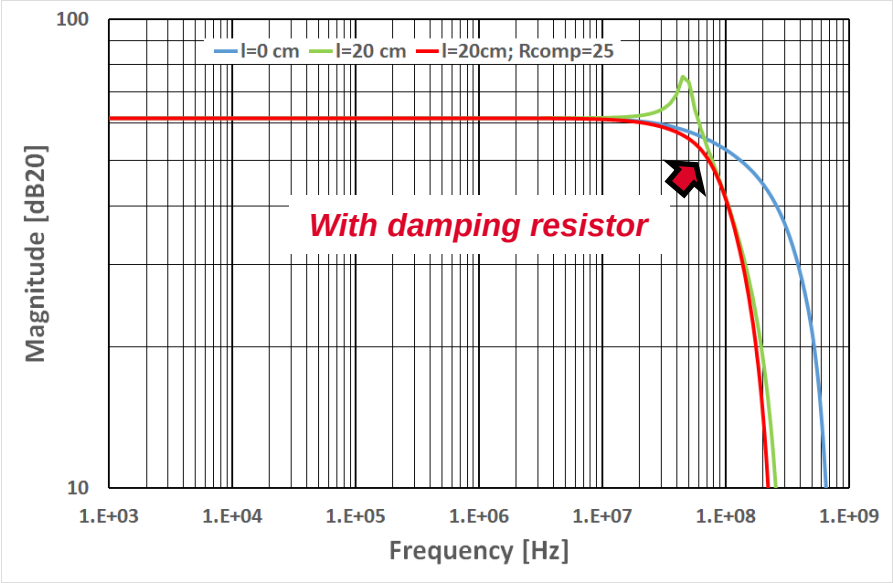




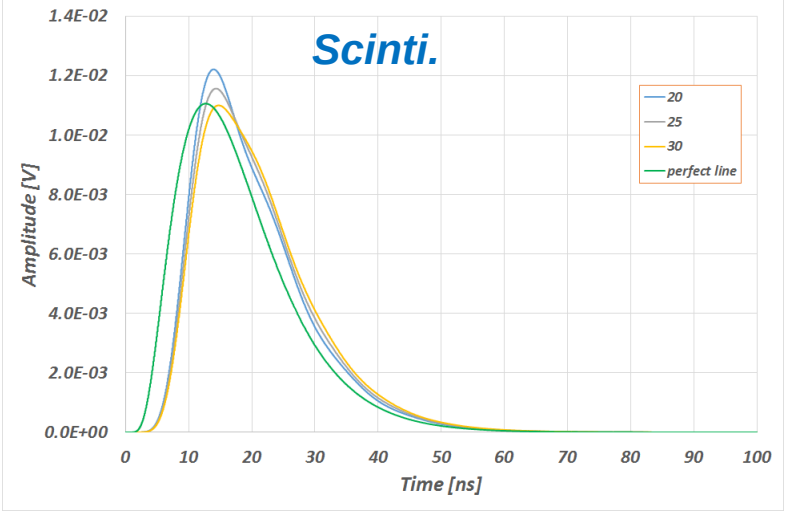
System performances

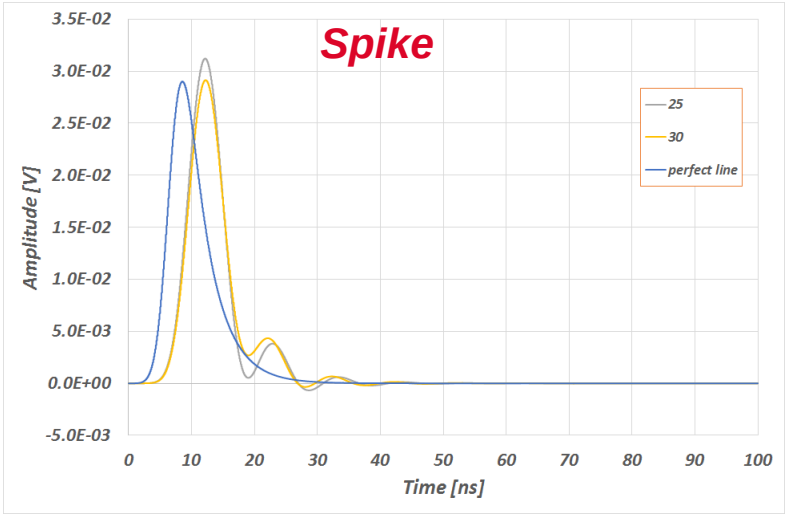
Needs damping resistor Rcomp





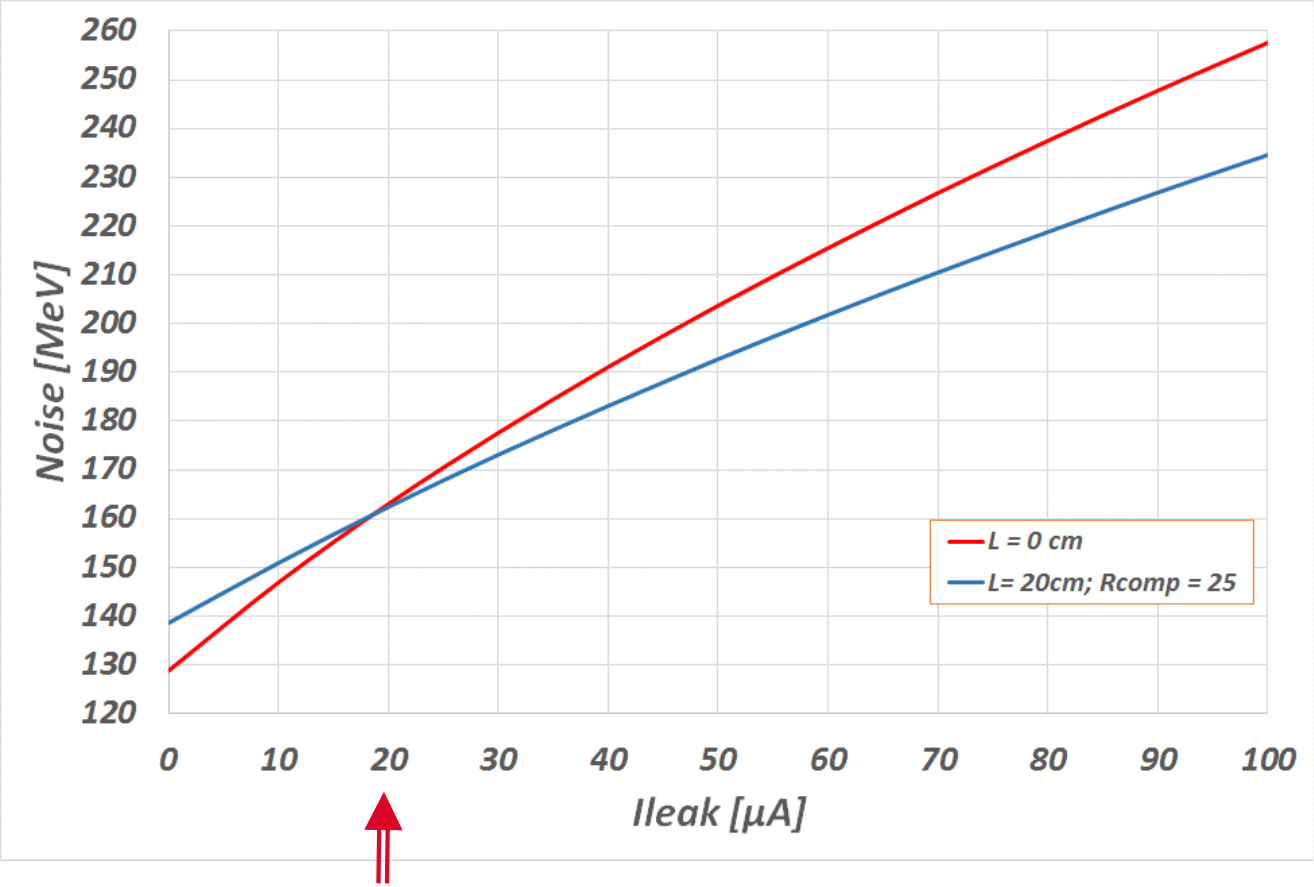
Length: 20 cm





System performances

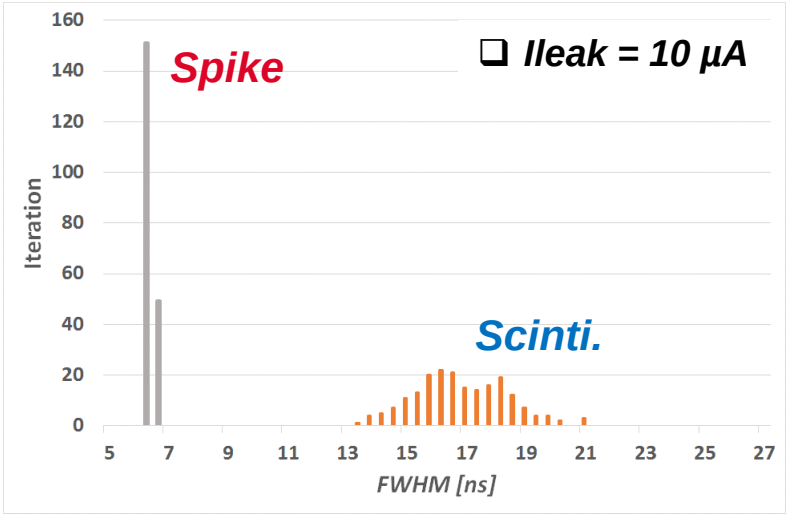
- **Kapton & damping resistor Rcomp**
  - Drawback: Noise ↑ (@ Ileak = 0 µA); Bandwidth ↓ => Timing ↓
- **Charge resolution (G10)**

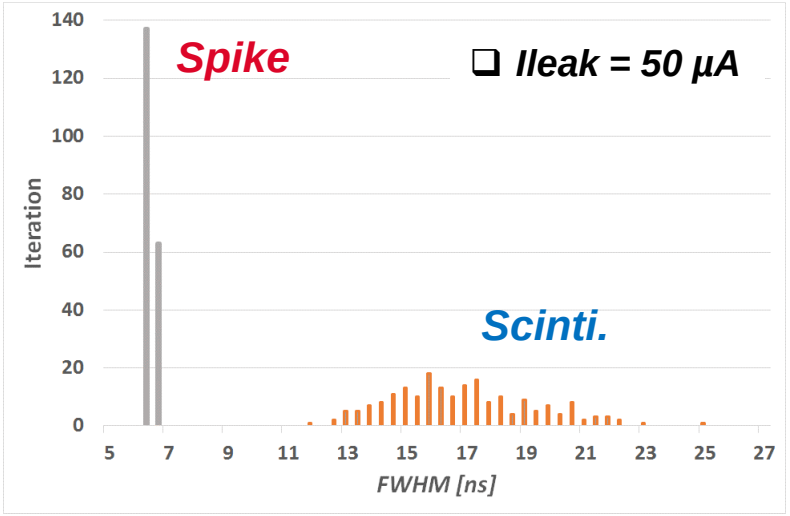


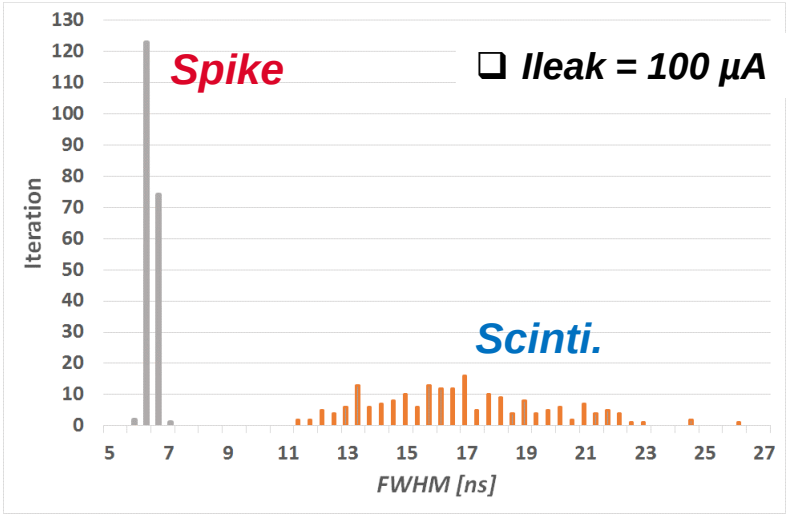
In fact, the Noise ↓ (Ileak > 10-20 µA) since the Bandwith ↓

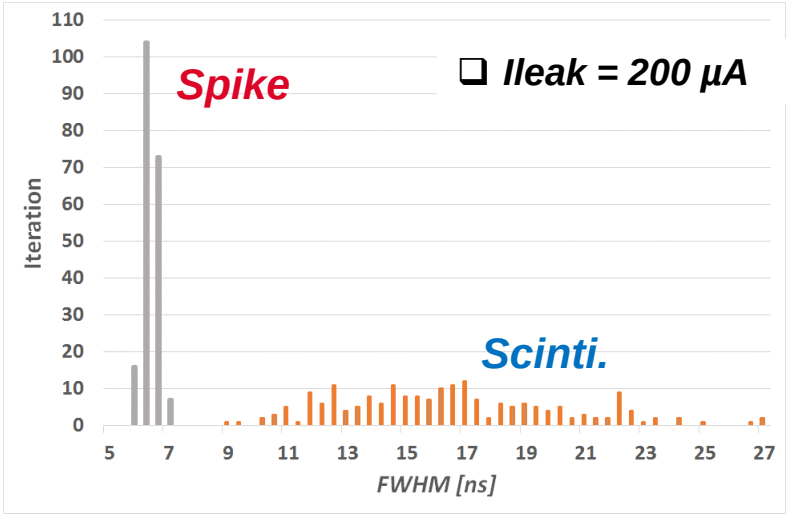
System performances (sim.)

Spike/Scinti separation @ 2 GeV for L = 20 cm & Rcomp = 25 Ω





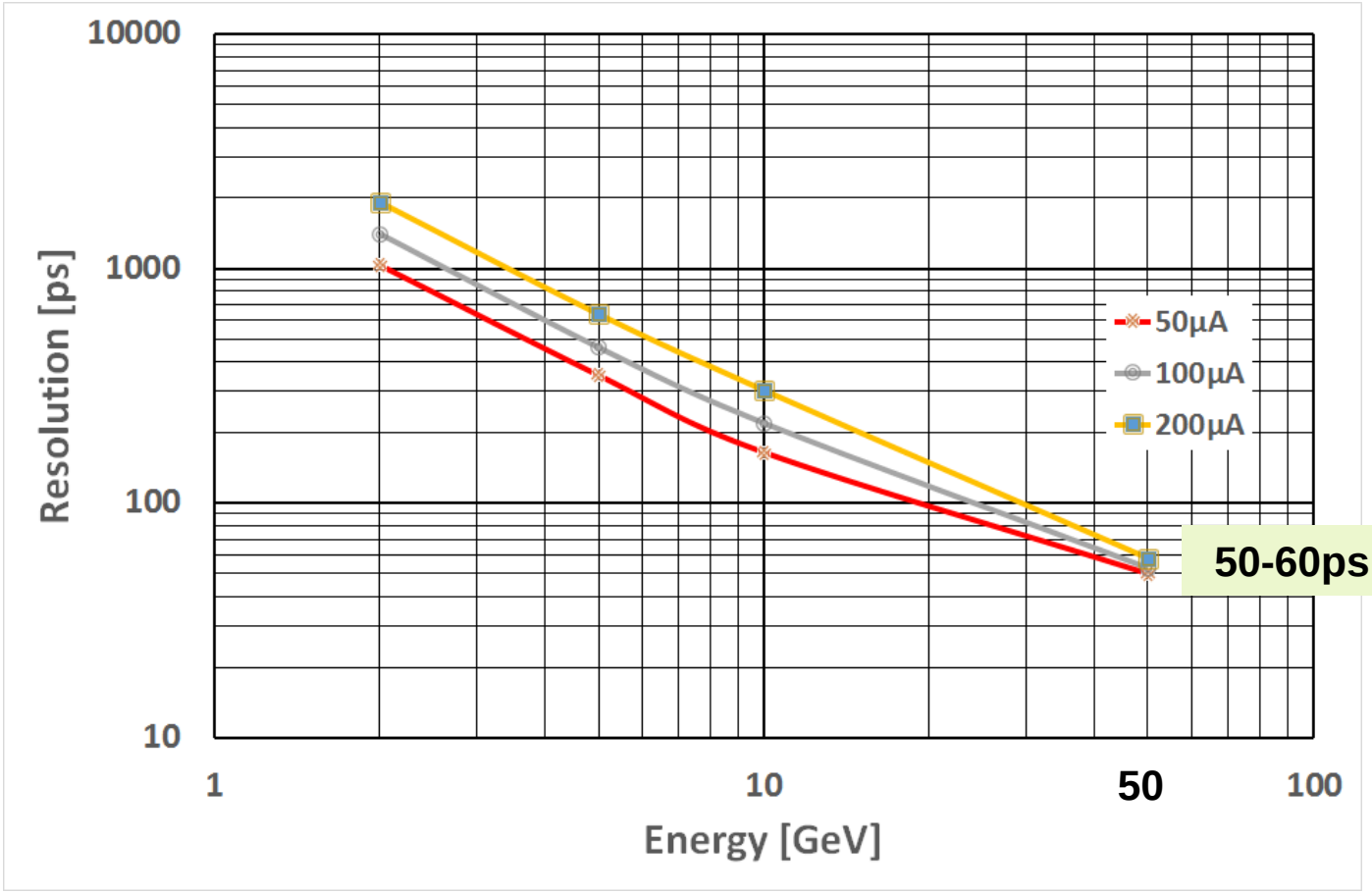




❑ Spike/Scinti separation remains still valid

System performances (sim.)

- **Timing resolution** (L = 20 cm & Rcomp = 25 Ω)

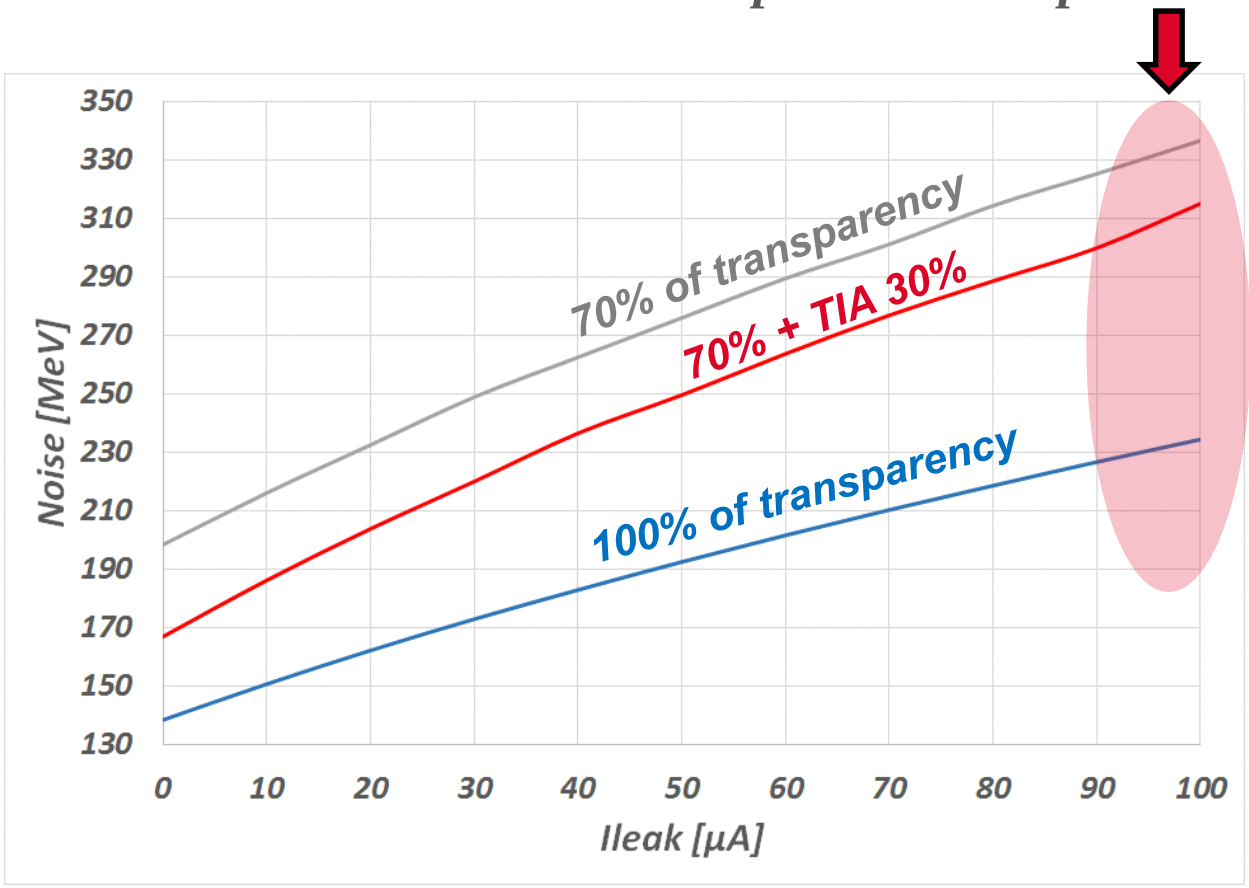


System performances (sim.)

Crystal transparency loss

❑ **Radiation damage to PbWO4 crystals:**

4.5 p.e /MeV to 3 p.e/MeV (- 30%)



❑ **Energy resolution can be improved by increasing Rconv (+ 30%)**

Status & Planning

- The schematic of the global chip is finished at 98%
- The layout has started but we are always waiting the agreement from TMC to have access to the TSMC Mixed-Signal Design Kit of the CERN

  [process started since 19 November 2015..]
- Planning: 15 June / 27 July

TSMC	J	F	M	A	M	J	J	A	S	O	N	D
TSMC 0.18 CMOS Logic or Mixed-Signal/RF, General	6	3,24	9,30	13,27	11,28	8,29	6,27	3,24	7,28	5,26	2,30	7
TSMC 0.18 CMOS High Voltage Mixed-Signal (CV018LD 1.8/3.3/32V)		9	30		4			3				
TSMC 0.18 CMOS High Voltage BCD Gen 2 (1.8V/5V...70V)		24			4		6		7		9	
TSMC 0.13 CMOS Logic or Mixed-Signal/RF, General or Low Power (8-inch)		9	16		11	15	27		7		9	7
TSMC 0.13 CMOS Logic or Mixed-Signal/RF, General or Low Power (12-inch)	11			13			13		20			

Conclusion

- The TIA ASIC is in layout phase
- The performances obtained by simulation are pretty good
- These performances will be degraded by coupling the electronic to the APD through kapton but spike tagging, charge resolution and timing measurement will remain acceptable
- Submission Planning: 15 June or 27 July