LVR – SLVR overview

CMS ECAL VFE phase II upgrade workshop

CEA-Saclay INSTN

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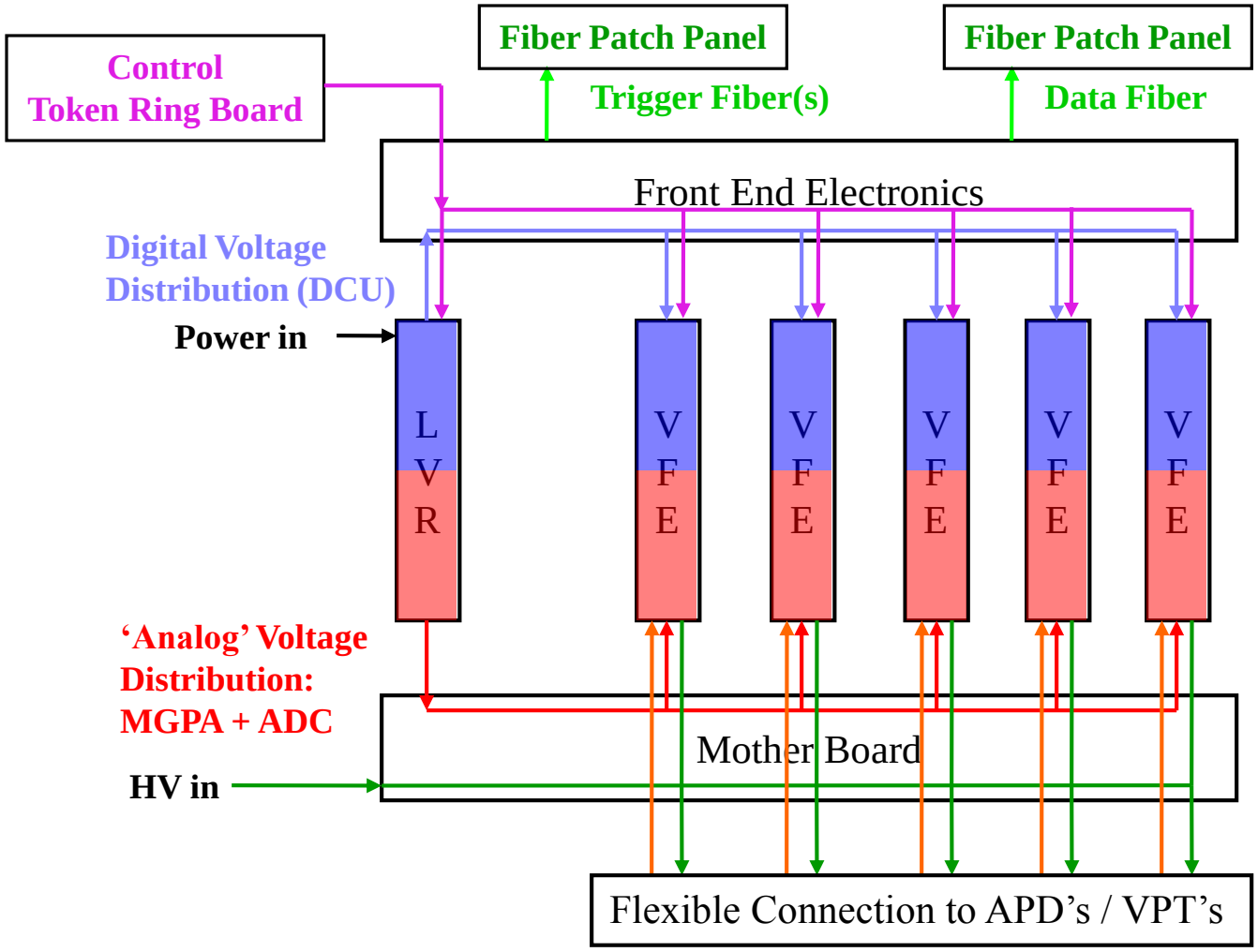
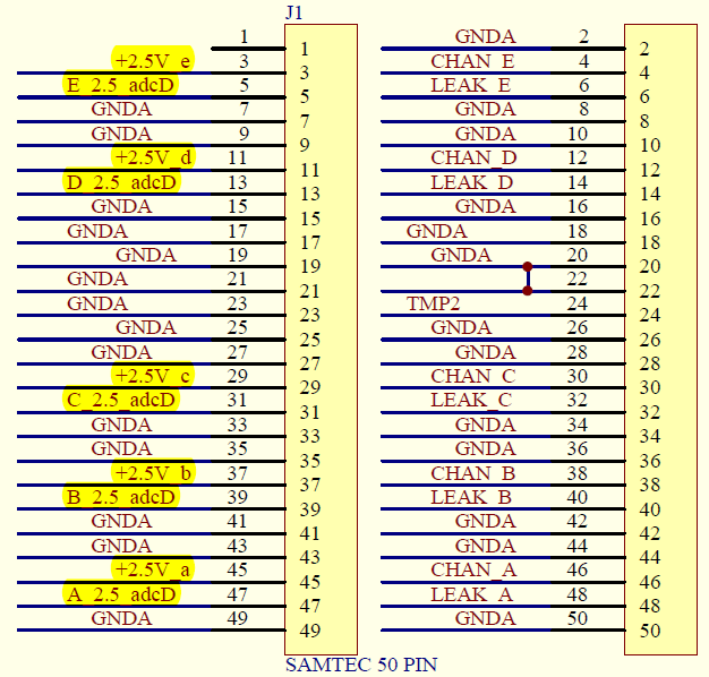
Present front electronics

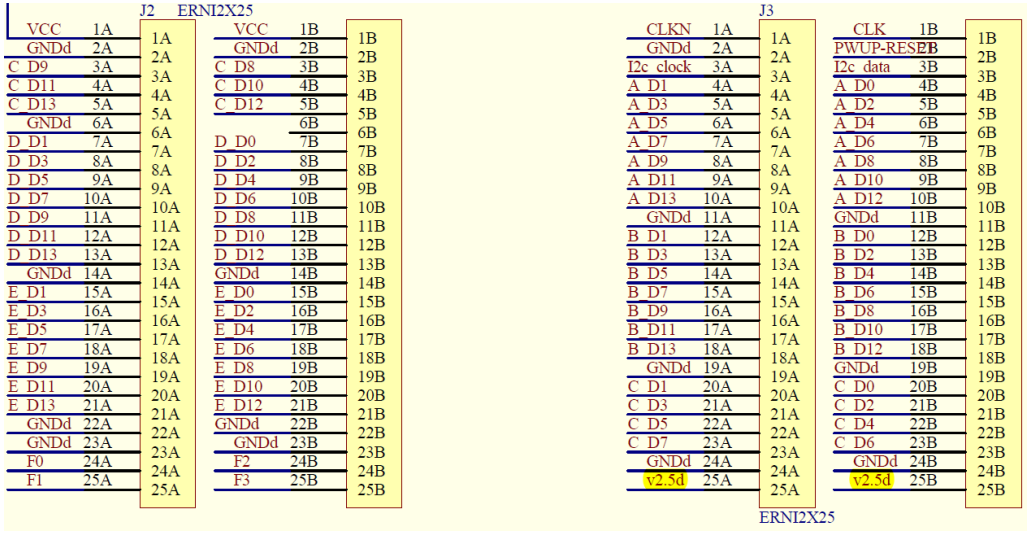


VFE power nets

VFE has 11 power nets:
5 x 2.5 V analog (MGPA)
5 x 2.5 V digital (ADC)
1 x 2.5 V digital (DCU)

10 of the power nets arrive via the MB
1 is connected to the FE card

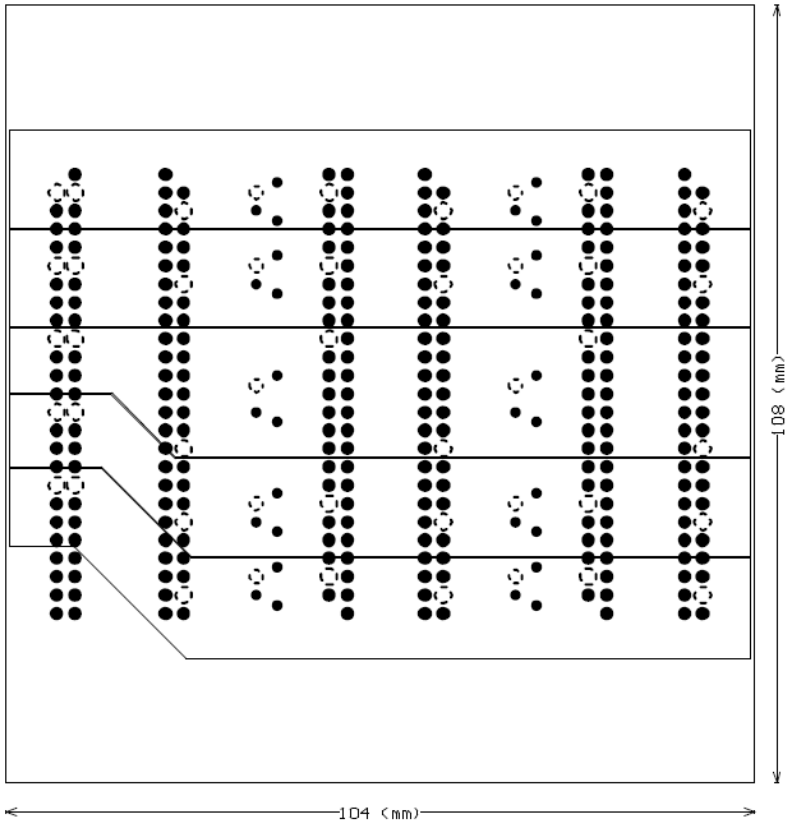




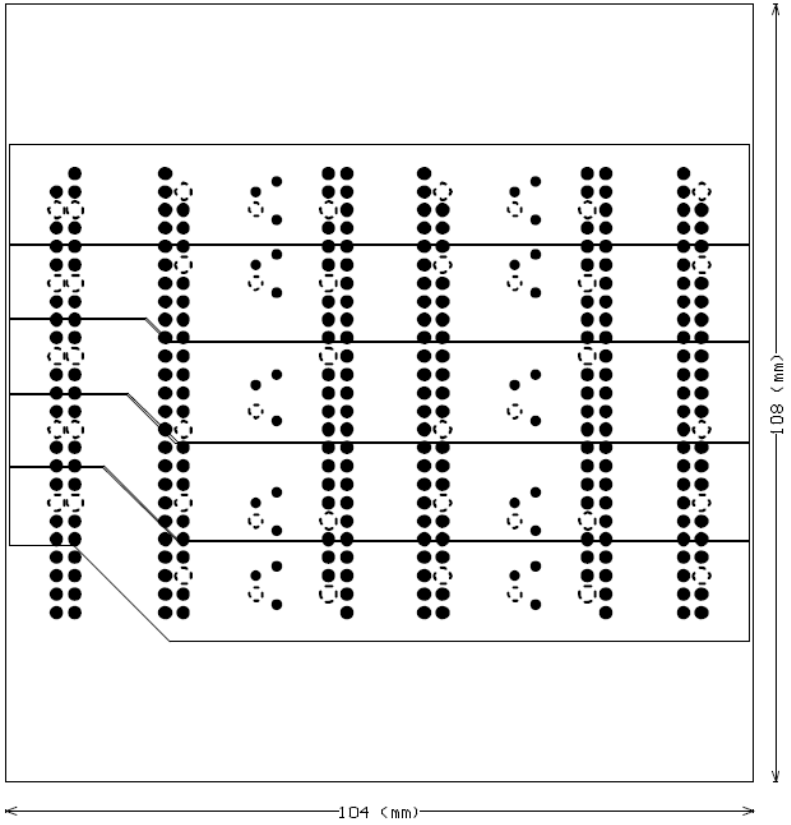
Power nets in the motherboard

Motherboard internal power planes

2.5 V digital



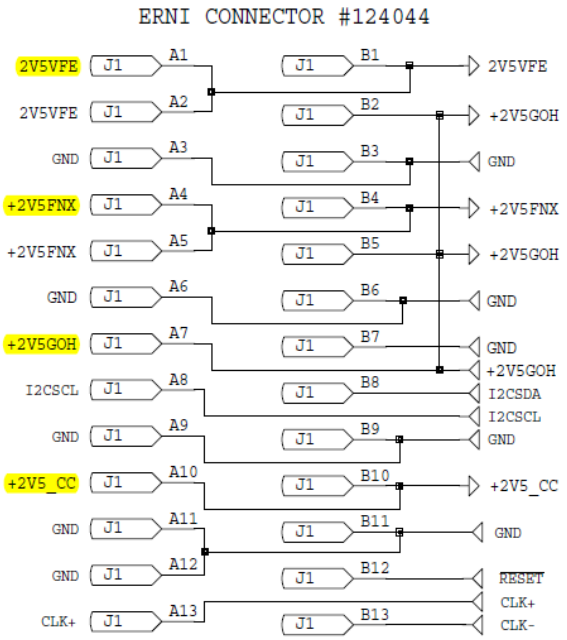
2.5 V analog

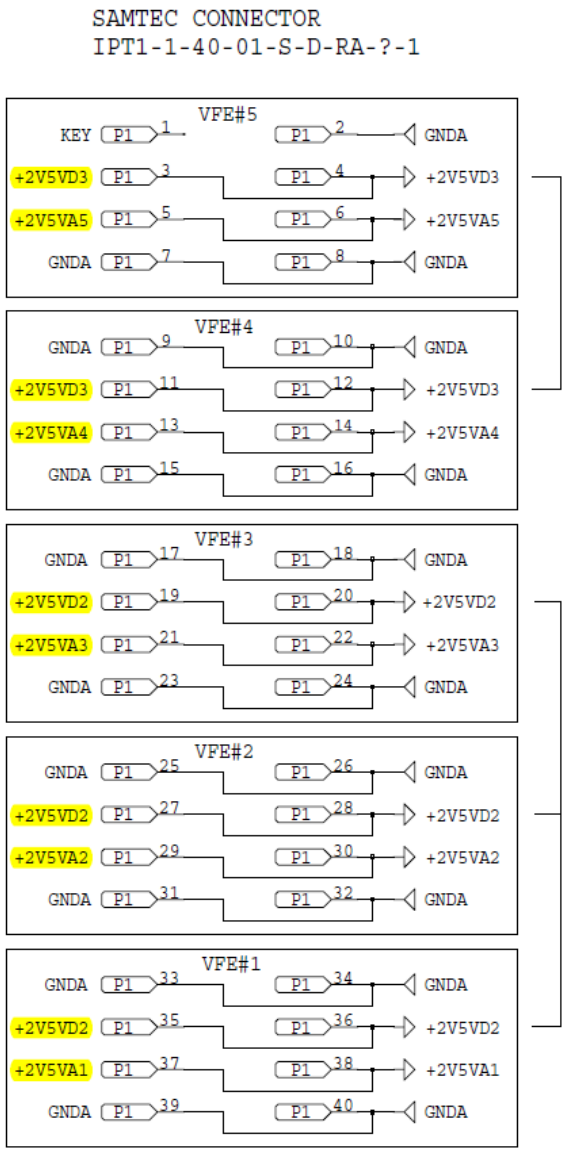


Power nets in the LVR

LVR hosts 11 linear regulators providing:

- 4 digital voltages to the FE:
  - 3 voltages for the FE
  - 1 voltage for the DCUs on the VFE
- 7 voltages to the mother VFE:
  - 5 x 2.5 V for the MGPAs
  - 2 x 2.5 V for the ADCs

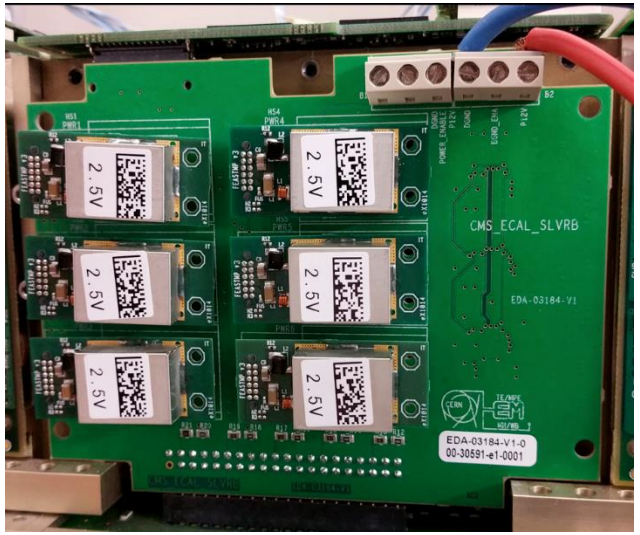




SLVR with FEASTMP_CLP

First version designed by Magnus
- 6 power nets == FEASTMP_CLP:
  - 5 x 2.5 V for the VFE
  - 1 x 2.5 V for the FE

- Tested in TT setup: B. Betev
- Tested at Virginia University



Design and layout iteration: make it fit into super-modules:
- Prototypes are in production

SLVR with FEASTMP_CLP

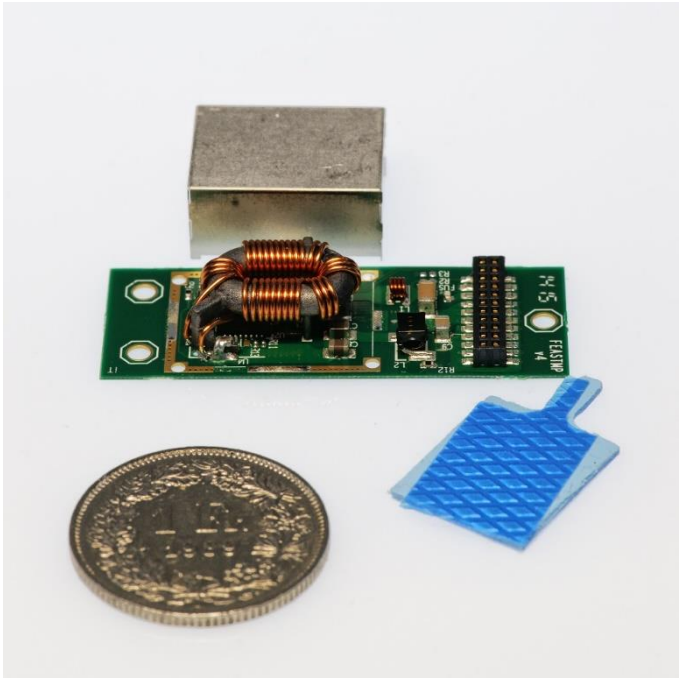
The SLVR becomes an almost passive board, hosting connectors for the FEASTMP_CLP modules and 3 DCU chips for voltage, current and temperature monitoring

➔ Properties and performance are (almost exclusively) determined by the FEASTMP modules

- Developed and fabricated by CERN
- radiation tolerant
- over current protection
- over temperature protection
- under voltage protection

Output voltage variation:

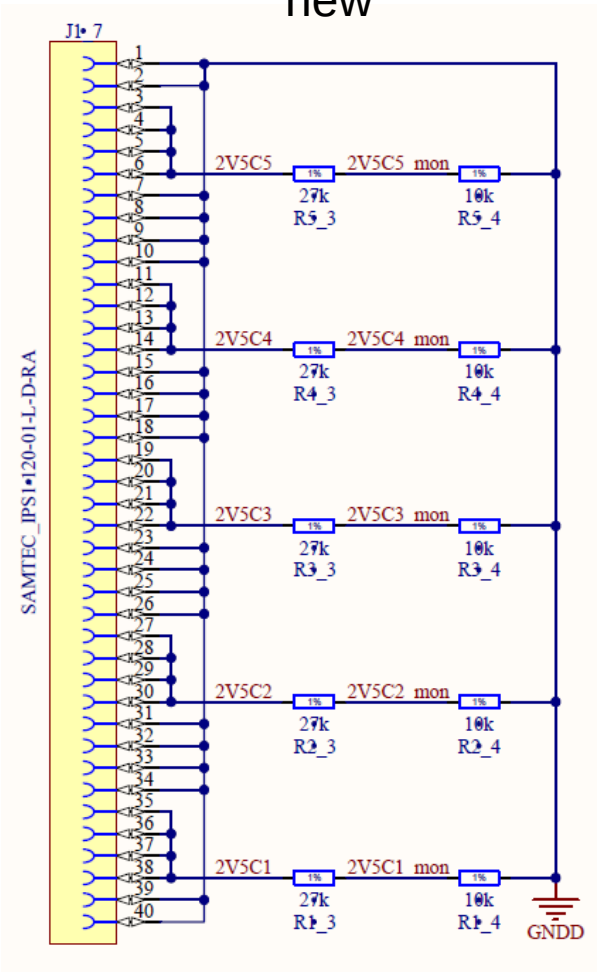
- Load and line regulation
- Spread of output voltages
- Radiation effects
- Temperature effects



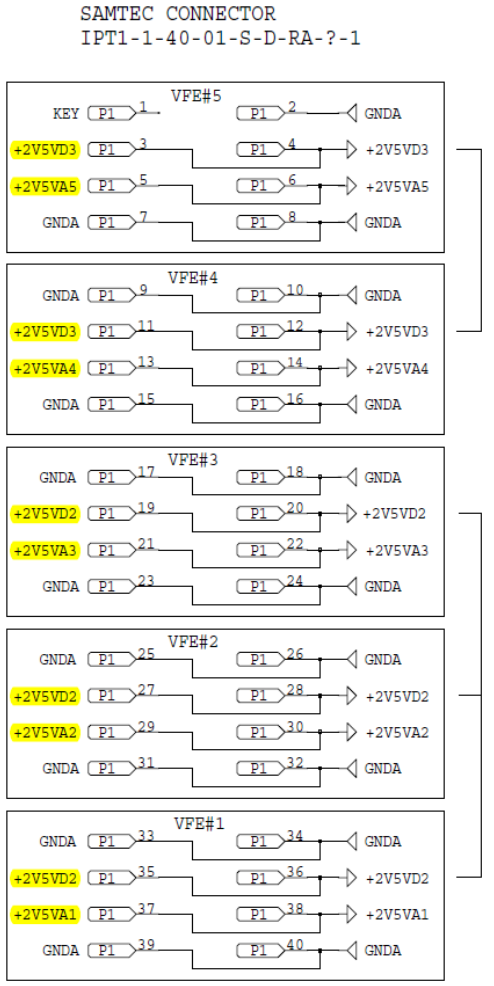
SLVR power interface

- Interface to the MB unchanged
- VFE analog and digital power grouped

new

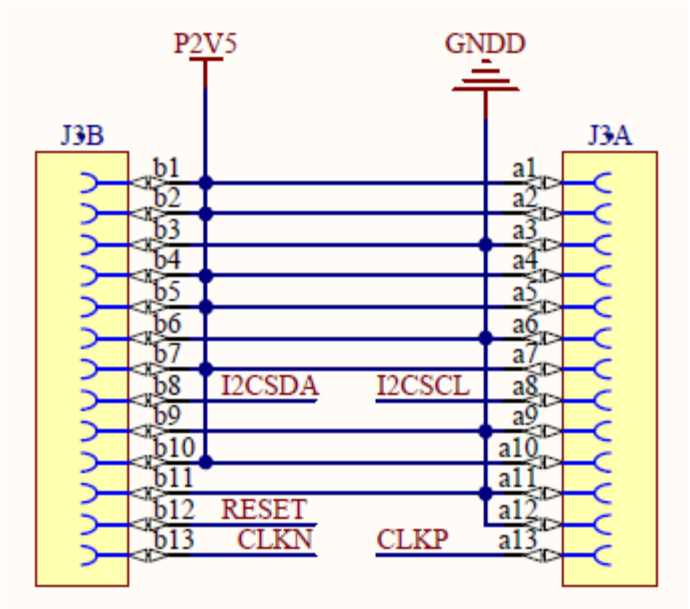


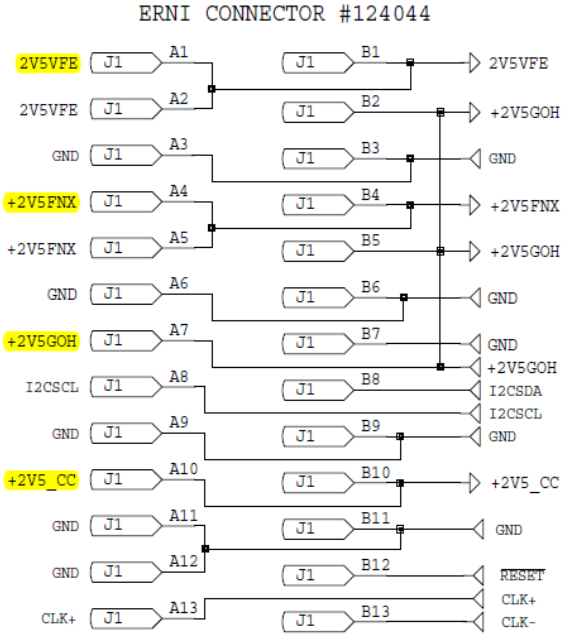
original



SLVR power interface

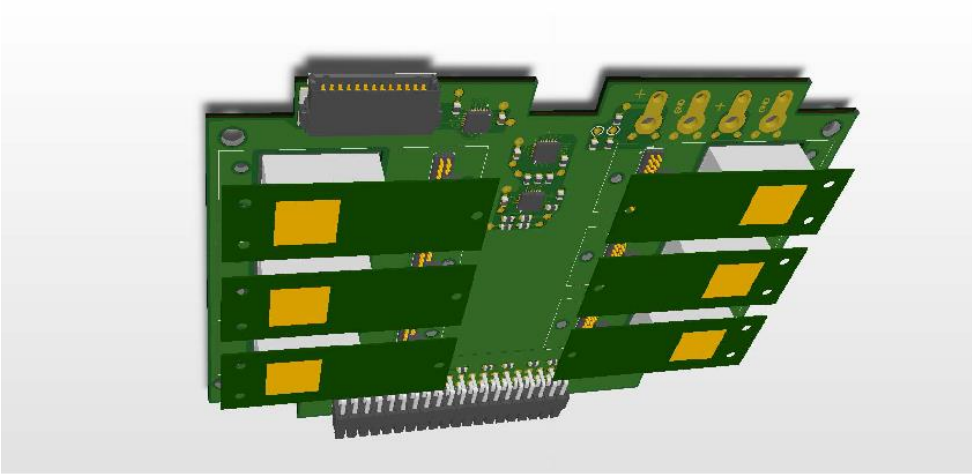
- Interface to the FE unchanged
- All voltages on a single net



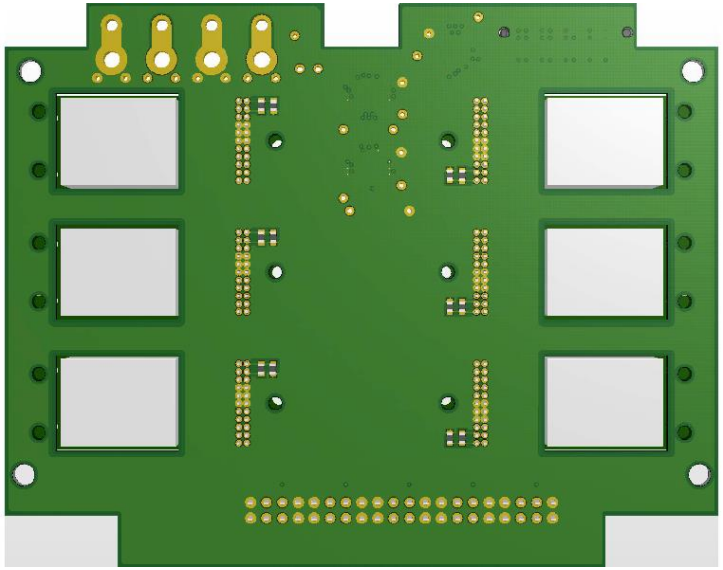


SLVR 3D view

TOP view: will be covered by the housing and coupled to the cooling bar

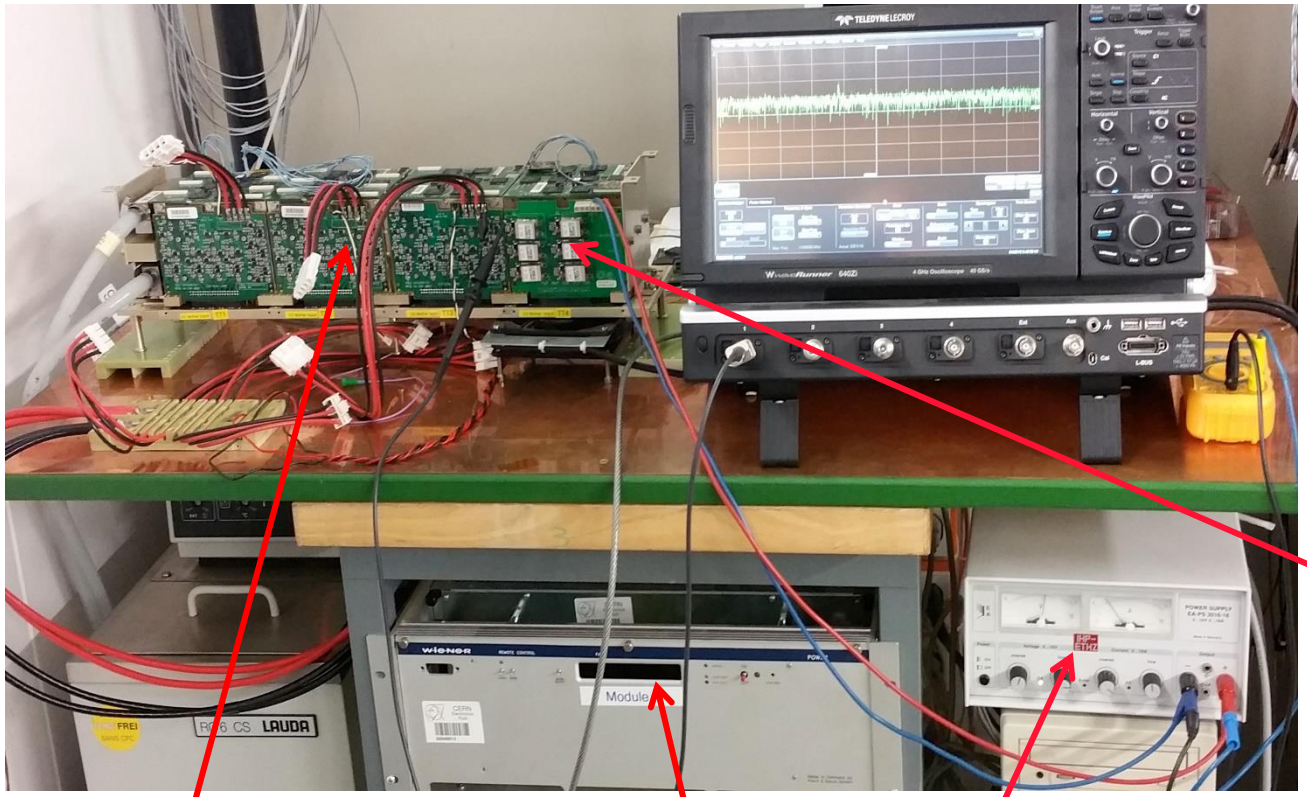


BOTTOM view

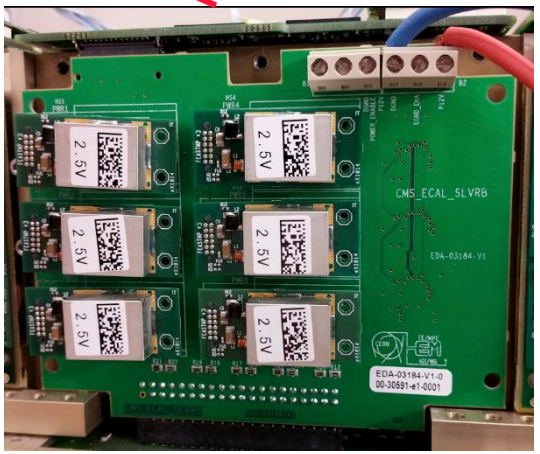


FEASTMP modules plug through the SLVR card

TT testsetup



SLVRB



Trigger Tower Test Setup in B.892. The SLVR Board integrated in TT4 (CCU=6)

Wiener LV power supply for input voltage of TT 1, 2 and 3

Linear LV Power Supply for input voltage of SLVRB (Input voltage = 10 Volts)

TT noise measurements

Pedestal data taken with SLVRB

Ch	Gain 1 Ped	Gain 1 RMS	Gain 6 Ped	Gain 6 RMS	Gain 12 Ped	Gain 12 RMS	St.
106	198.6	.6	196.4	.6	209.4	1	0
107	194.6	.6	207.5	.7	203.3	1	0
108	197.4	.6	206.2	.7	208.7	.9	0
109	209.8	.6	196.7	.7	192.4	.9	0
110	212.2	.5	200.4	.7	196.1	1	0
126	189	.5	208.9	.7	205.5	1	0
127	205	.5	211.7	.7	208.7	.9	0
128	193.9	.6	211.5	.7	210.8	.9	0
129	193	.6	201.4	.7	193	1	0
130	197.4	.5	195.8	.8	207	1	0
146	191	.6	189.7	.7	198	1	0
147	196.7	.6	196.9	.7	205.2	1	0
148	207.5	.6	205.1	.7	205.8	1	0
149	203.1	.6	209.2	.7	206.2	1	0
150	200.1	.7	198.1	.8	196.5	.9	0
166	203.8	.6	199.7	.7	193.4	1	0
167	204.9	.5	208.3	.6	195.6	.9	0
168	190.9	.6	195.8	.7	211.2	1	0
169	197.4	.6	201.1	.7	195.1	.9	0
170	191.6	.6	193.5	.7	197.9	.9	0
186	206.7	.6	188.8	.6	196.8	1	0
187	193.1	.5	202.1	.7	186.2	.9	0
188	185.4	.6	190.4	.7	184.9	.9	0
189	190.5	.6	185.5	.7	197.2	1	0
190	203.8	.6	191.6	.7	182.9	1	0
Mean:	198.3	0.58	199.7	0.70	199.5	0.96	

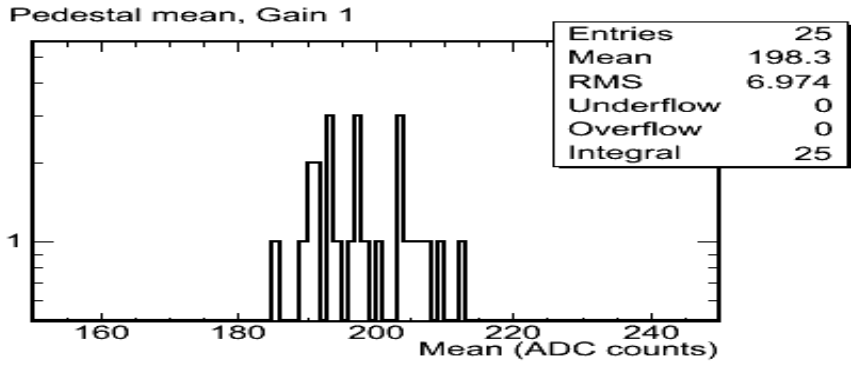
Pedestal data taken with original LVRB

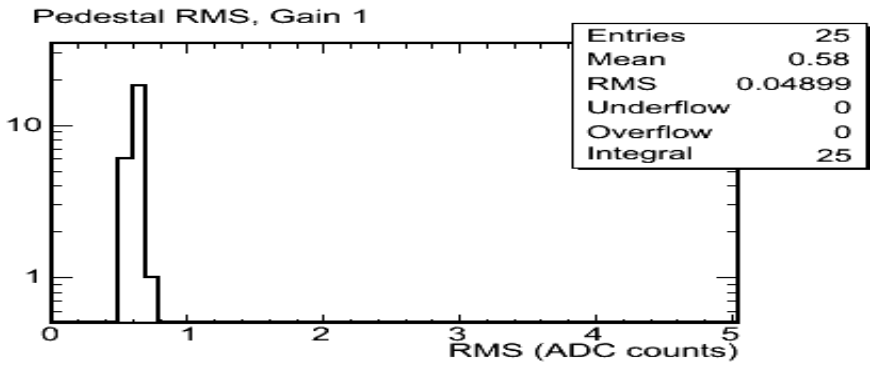
Ch	Gain 1 Ped	Gain 1 RMS	Gain 6 Ped	Gain 6 RMS	Gain 12 Ped	Gain 12 RMS	St.
106	196.5	.6	194.1	.7	208.5	1	0
107	192.2	.6	205.8	.7	202.6	1	0
108	195.1	.5	204	.7	207.7	1	0
109	207.9	.6	195.4	.7	192.1	1	0
110	210	.6	199.3	.7	195.7	1	0
126	190.7	.6	208.9	.6	203.8	1	0
127	206.4	.6	212.3	.7	206.9	.9	0
128	195.7	.6	211	.7	209.8	1	0
129	194	.6	204.6	.7	195.3	1	0
130	198.7	.6	194.9	.7	205.1	.9	0
146	193.2	.6	190.4	.7	196	1	0
147	199.1	.6	198.2	.8	208.2	.9	0
148	208.8	.5	204.5	.7	203.5	1	0
149	204.8	.6	208.9	.7	205.8	1	0
150	202	.6	198.6	.7	192.6	1	0
166	204.4	.6	198.1	.7	190.8	1	0
167	207.5	.5	210.4	.7	195.9	.9	0
168	192.8	.5	196.2	.7	211.5	.9	0
169	198	.5	200.6	.7	191.9	1	0
170	192.8	.6	192.8	.7	197.6	1	0
186	210.5	.6	192.9	.7	200.9	1	0
187	197.7	.6	207.9	.8	192.3	1	0
188	190.3	.6	194.7	.7	190.5	1	0
189	195.2	.6	191.2	.7	203.6	.9	0
190	209.7	.6	197.4	.7	191.4	1	0
Mean:	199.8	0.58	200.5	0.70	200.0	0.98	

LVR → SLVR: Performance remains unchanged

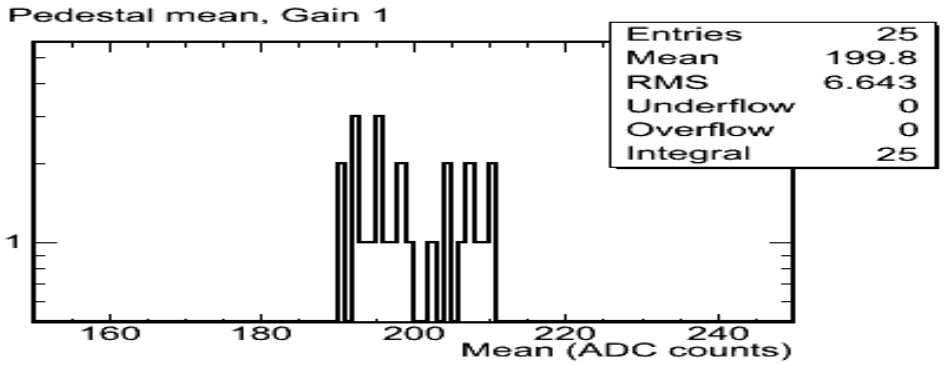
TT testsetup

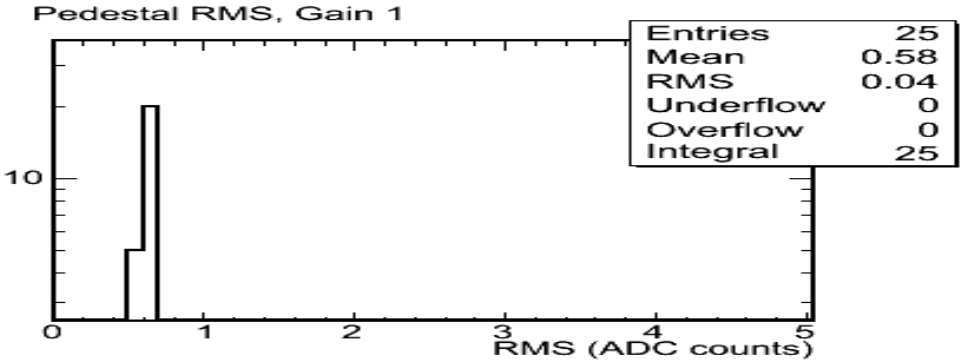
new SLVR





old LVR





LVR → SLVR: no significant difference