# VFE interface to FE

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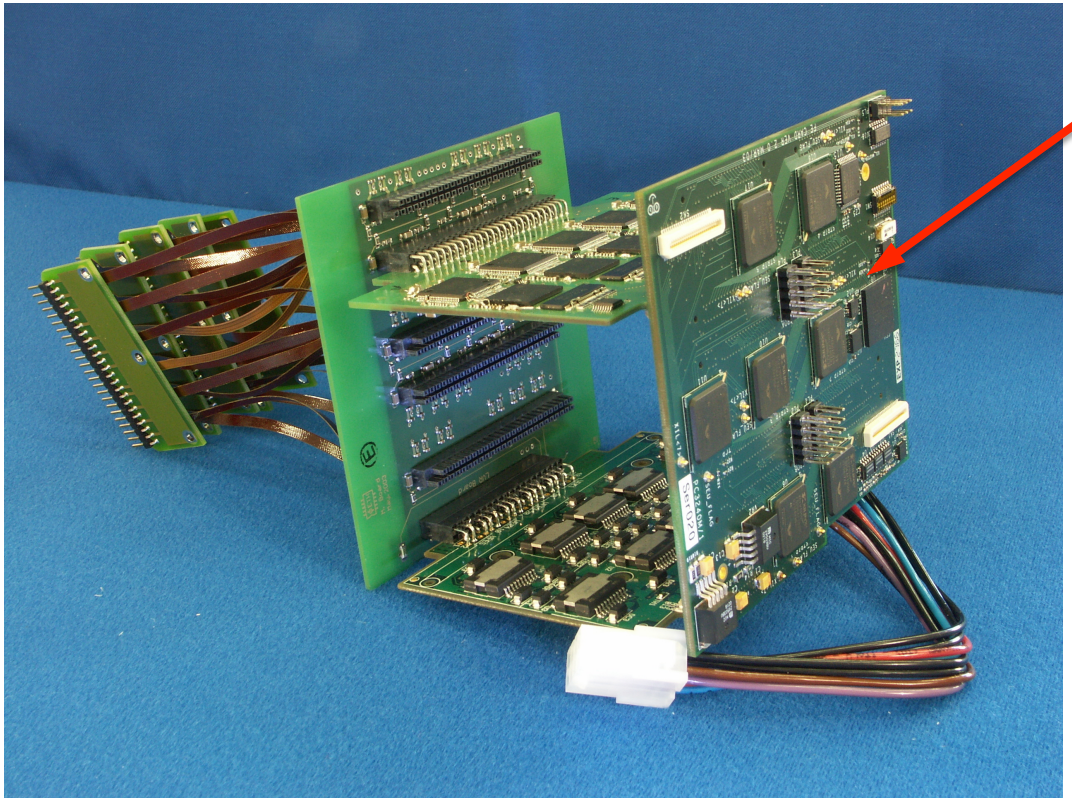
*CMS ECAL VFE phase II upgrade workshop, May 2016*

# Basics: we stay with the Trigger Tower concept



Legacy EB FE card:

- Transmit data from VFE at 2x0.8Gbs
  - Max. transmission capacity: two GOH, max 1.6Gbs each = 3.2Gbs
- Contain buffers and logics to accept Level1 trigger
- Contain CCU connected to Token Ring to deliver clock and control information to VFE

Phase II EB FE card:

- Need >16Gbs
- New clock and control system

# History: data links for LHC experiments

- Three common R&D projects:
  - FERMI
  - Token Ring for Clock & Control
  - GOL
- Key issues – high reliability in radiation hard conditions
  - Choice of technology
  - Rad. Hard design

**Current situation after ~10% of the design fluencies:**

- Observe radiation-induced dark current, thresholds, etc. effects according to the expectation
  - 250nm technology was a good choice
- Observe events which can be interpreted as a SEU, recoverable, rate fit to the expectation
  - Rad. hard design works
- No massive problems with the data corruption
  - 8/10 bit & Glink protocols work well
- No dead channels clearly attributed to the radiation damage (CMS ECAL)

1. **We do observe the radiation induced effects.**
2. **Rad. Damage mitigation is justified and give the expected results.**

# Can we use the off-shelf optical links components?

- 20Gbs per trigger tower is an easy task for the modern data communication industry
  - Off shelf devices, transmit/receive per link
    - 10 Gbs almost obsolete
    - 25 Gbs widely produced
    - 40 Gbs state-of-art, available from many producers
  - Radiation hard technology: 130nm and 65nm
    - Multiple effects, sometimes hard to interpret, different for different processes / producers
    - No definitely rad. hard technology so far

The most reasonable choice for the moment – CERN custom rad. hard design: GBT & lpGBT ,VL & VL+

# Data Link for the upgrade FE

- Reasonable strategy
  - Consider lpGBT @VL+ as a baseline
    - High data transmission rate, allow 80MHz and more sampling
    - Development on-going, failure can not 100% excluded
  - Safe backup solution – currently available GBT + VL
    - Industrial production
    - Marginally sufficient data transmission rate

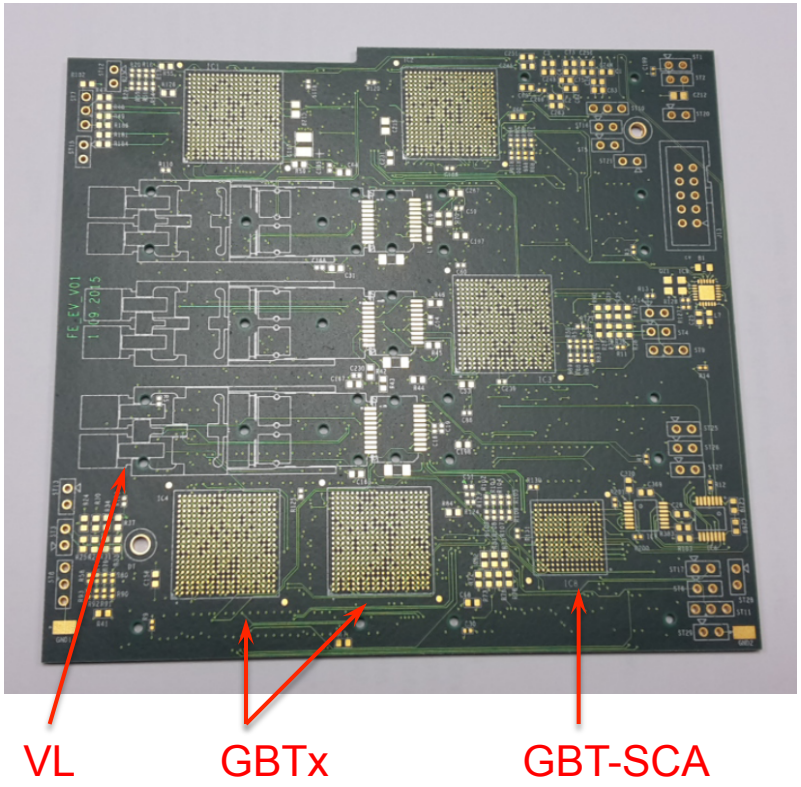
# GBT based FE. Bit/chip count

| | 5xGBTx 8/10bit, 4.48GBs | 3xlpGBT Fec5 9.13Gbs | 4xlpGBT Fec5 9.13Gbs | 5xlpGBT Fec5 9.13Gbs | 6xlpGBT Fec5 9.13Gbs |
|---|---|---|---|---|---|
| Total data transmission rate (per FE) | 22.4 Gbs | 27.39 Gbs | 36.52 Gbs | 45.65 Gbs | 55.8 Gbs |
| Bits per crystal @40MHz | 22 | 27 | 36 | 45 | 55 |
| Bits per crystal @80MHz | 11 | 13 | 18 | 22 | 27 |
| Bits per crystal @160MHz | 5 | 6 | 9 | 11 | 13 |

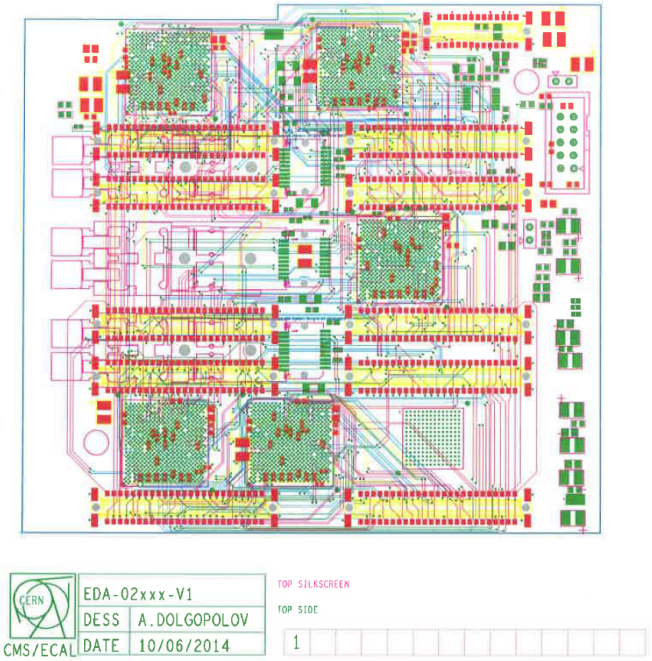
VFE design with the current amount of data (12 + 2 bits per crystal) can run

- @ 40MHz with 5 x GBTx
- @ 80MHz with 4 x lpGBT
- @ 160MHz with 6 x lpGBT

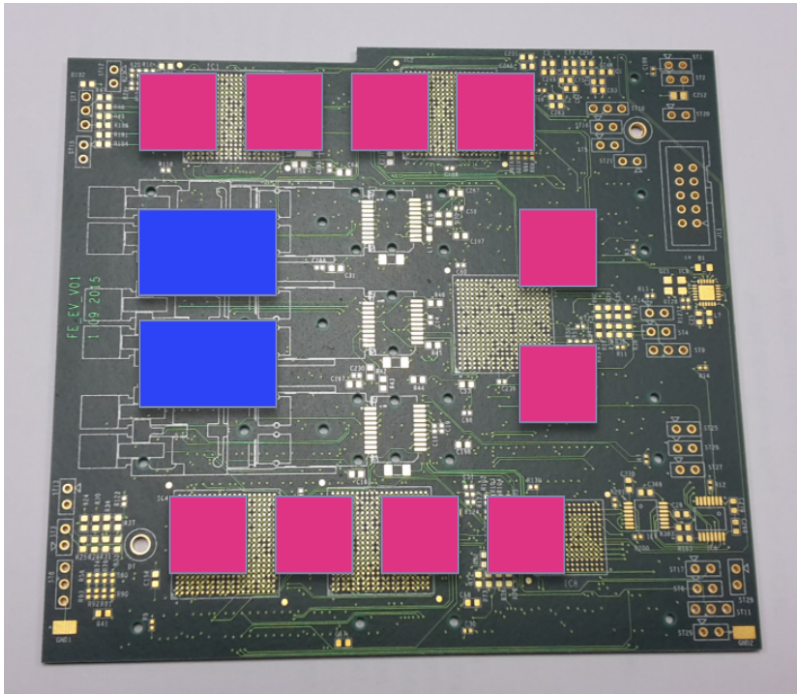
# 5xGBTx option




- We can place on the FE card
  - 5 x GBTx
  - 1 x GBT-SCA
  - 3 x VL modules: 5 x T & 1 x R



# lpGBT options



- GBTx is 20 x 20 BGA, 17mm x17mm
- lpGBT – 17 x 17 BGA, 9mm x 9mm
- No GBT-SCA needed
- VL+ is much more compact than VL
- → we can place more than 10 lpGBT and > 10+1 VL+ transmitters on the FE card

# VL+

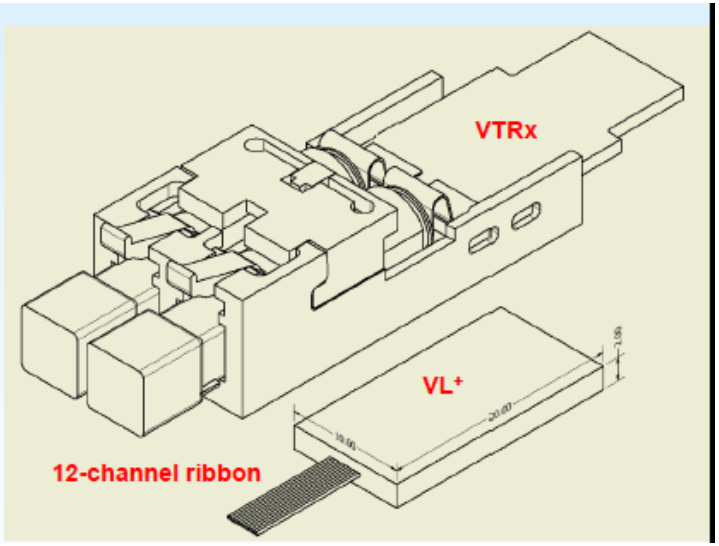
- The Versatile Link PLUS project (VL+) targets the phase II upgrades of the ATLAS and CMS experiments
- VL+ was officially announced at ACES 2014 and started on 1 Apr 2014. It is subdivided in three phases of 18 months each:
  - Phase 1: proof of concept (Apr 2014 – Oct 2015)
  - Phase 2: feasibility demonstration (Oct 2015 – Apr 2017)
  - Phase 3: pre-production readiness (Apr 2017 – Oct 2018)
- Collaboration between CERN, FNAL, Oxford, and SMU

| | Versatile Link | Versatile Link PLUS |
|---|---|---|
| Optical mode | Single- and multi-mode | Multi-mode |
| Flavours | 1Tx+1Rx, 2Tx | Configurable at build time up to nTx(+1Rx) |
| Radiation level | Calorimeter grade | Tracker grade |
| Form factor | SFP+ | Custom miniature |
| Data rate | Tx/Rx: 5 Gb/s | Tx: 5/10 Gb/s, Rx: 2.5 Gb/s |

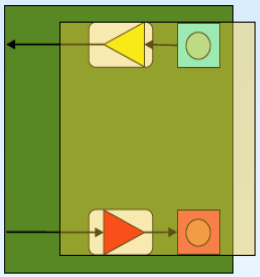
Table : Key differences between VL and VL+

8 March 2016 csaba.soos@cern.ch

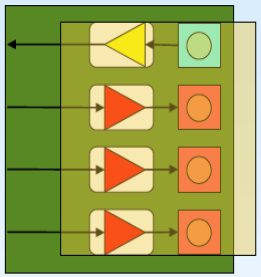
# VL+ Possible opto-hybrid layout



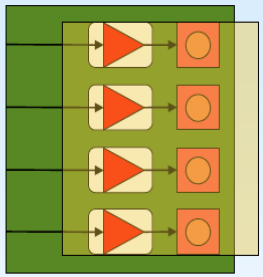

Discrete-based derived from:
- Light peak
- USB-3
- Thunderbolt



1 TX + 1 RX

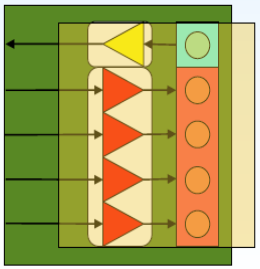


3 TX (single channel LDDs) + 1 RX

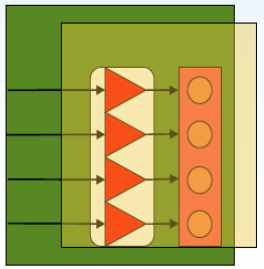


4 TX (single channel LDDs)

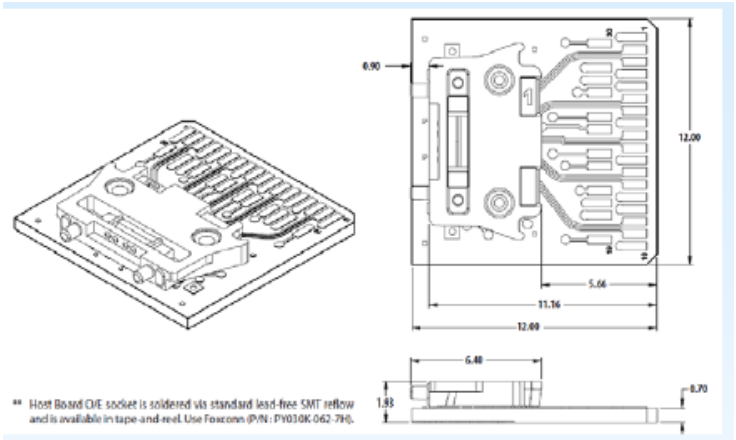
Array-based derived from:
- QSFP+ engine

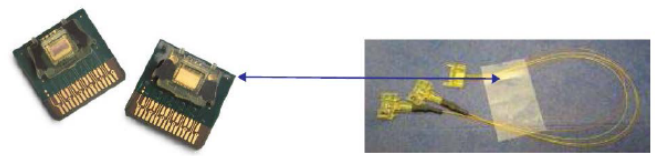


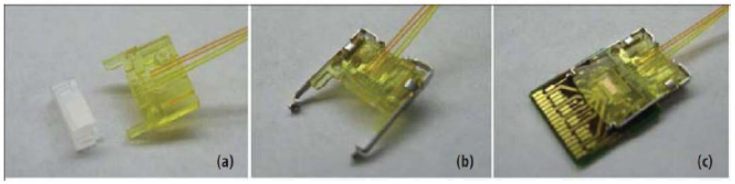
1/3/4 TX (using LDD array) + 1 RX



4/8 TX (using LDD arrays)





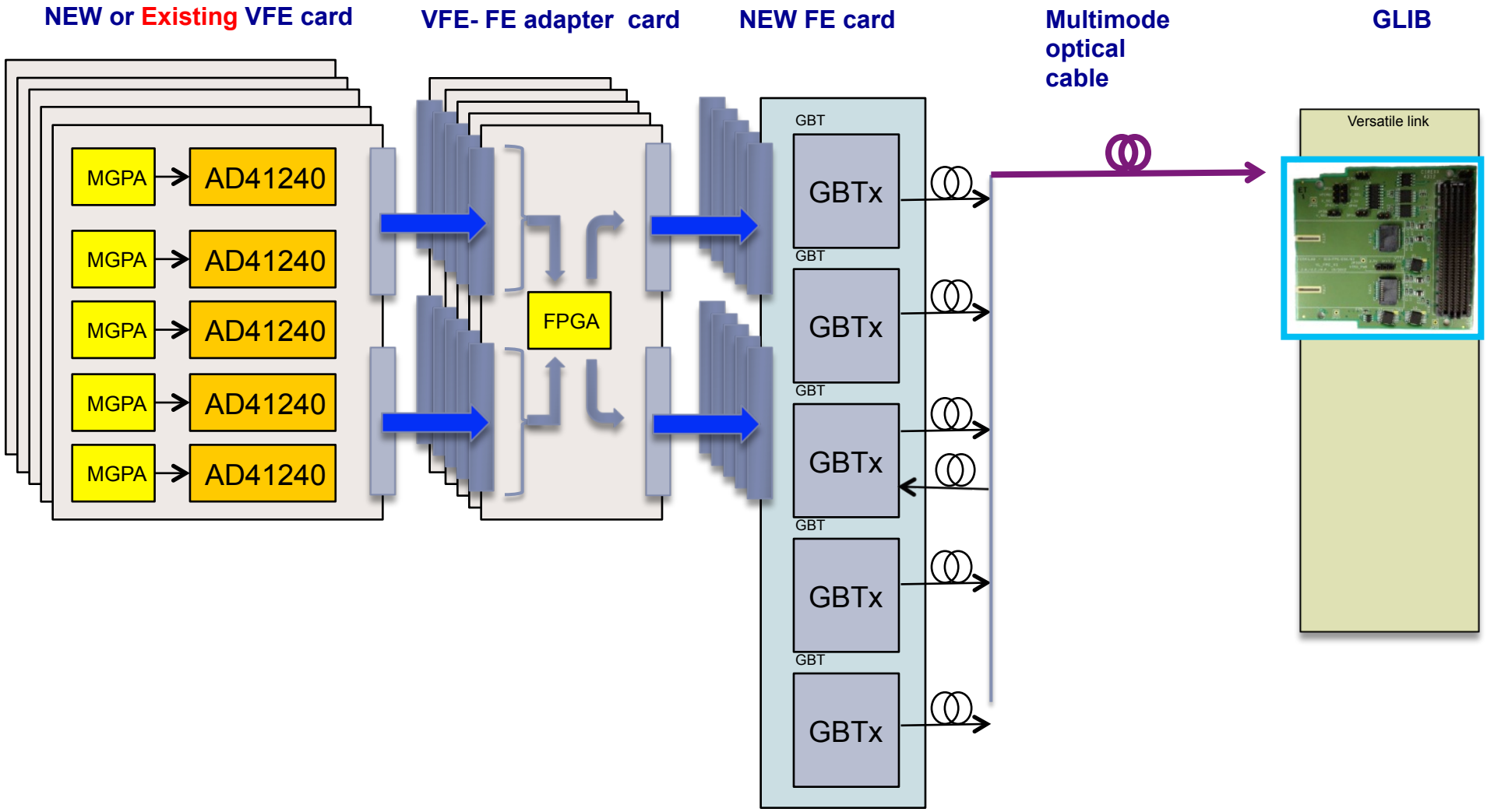

Mechanical samples tested at CERN

# VFE – FE interface

Direct connection, no interface in case of appropriate ADC output configuration.

- GBTx option
  - ADC → GBTx: 8/10 bit eLinks
    - Bandwidth 80 / 160 / 320 Mb/s
    - Max #eLinks 56 / 28 / 14
  - Clock & control: GBT-SCA chip, sufficient capacity for 5xVFE
- lpGBT option
  - ADC → lpGBT: FEC5 eLinks
    - Bandwidth 320 / 640 / 1280 Mb/s
    - Max #eLinks 28 / 14 / 7
  - Clock & control function taken by lpGBT (to be clarified)

# Test in 2016: FE deminstrator



# FE demonstrator: tests foreseen

- VFE-FE eLink interface (via Adapter board)
  - Speed
  - Protocols
- Clock distribution
- VFE slow control
- Data transmission
  - Old VFE
  - VFE simulator (Adapter) @ 40MHz, 80MHz, …
  - New VFE
- Beam test with the real TT

# EE demonstrator