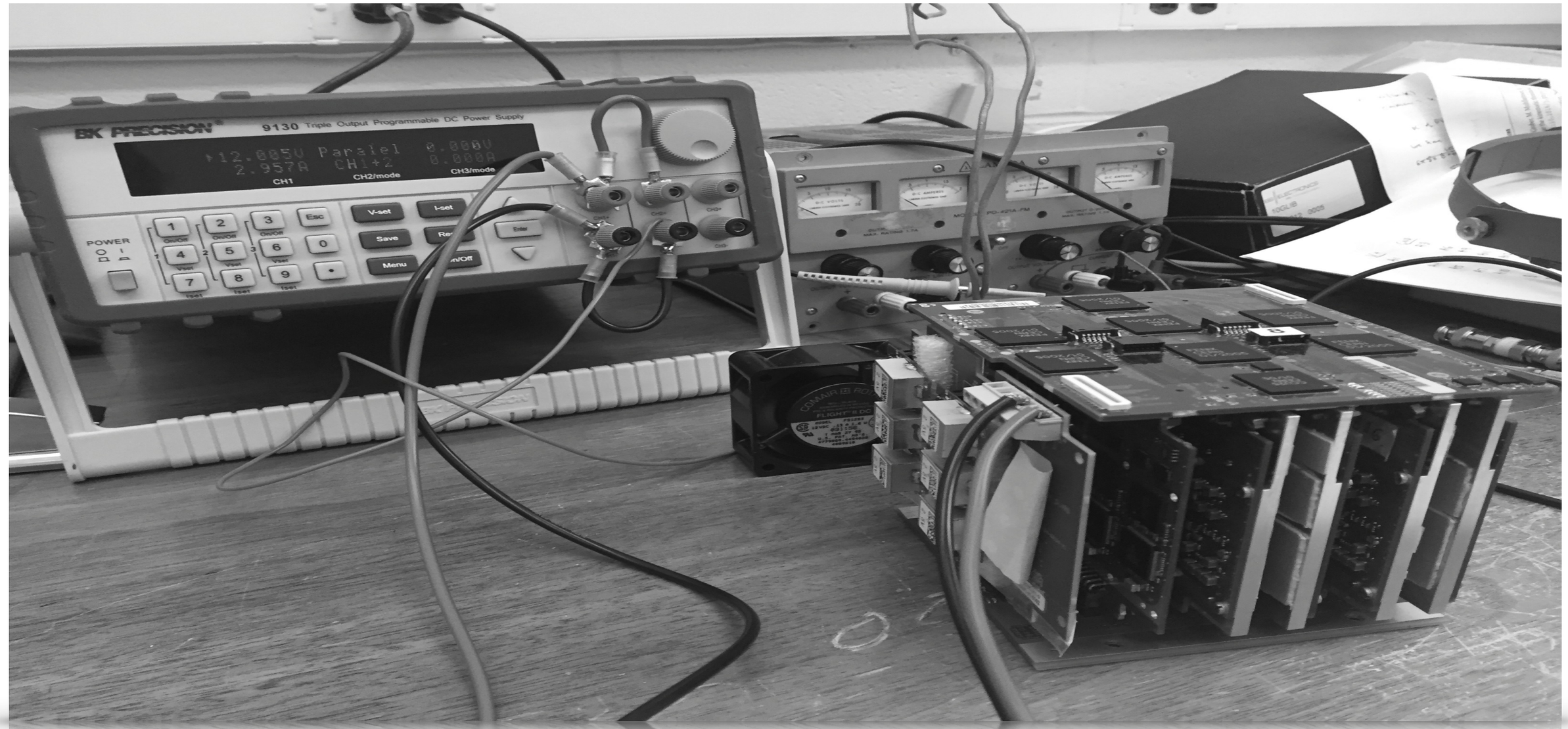


CMS ECAL VFE phase II upgrade workshop

CEA-Saclay INSTN 11-13 May 2016

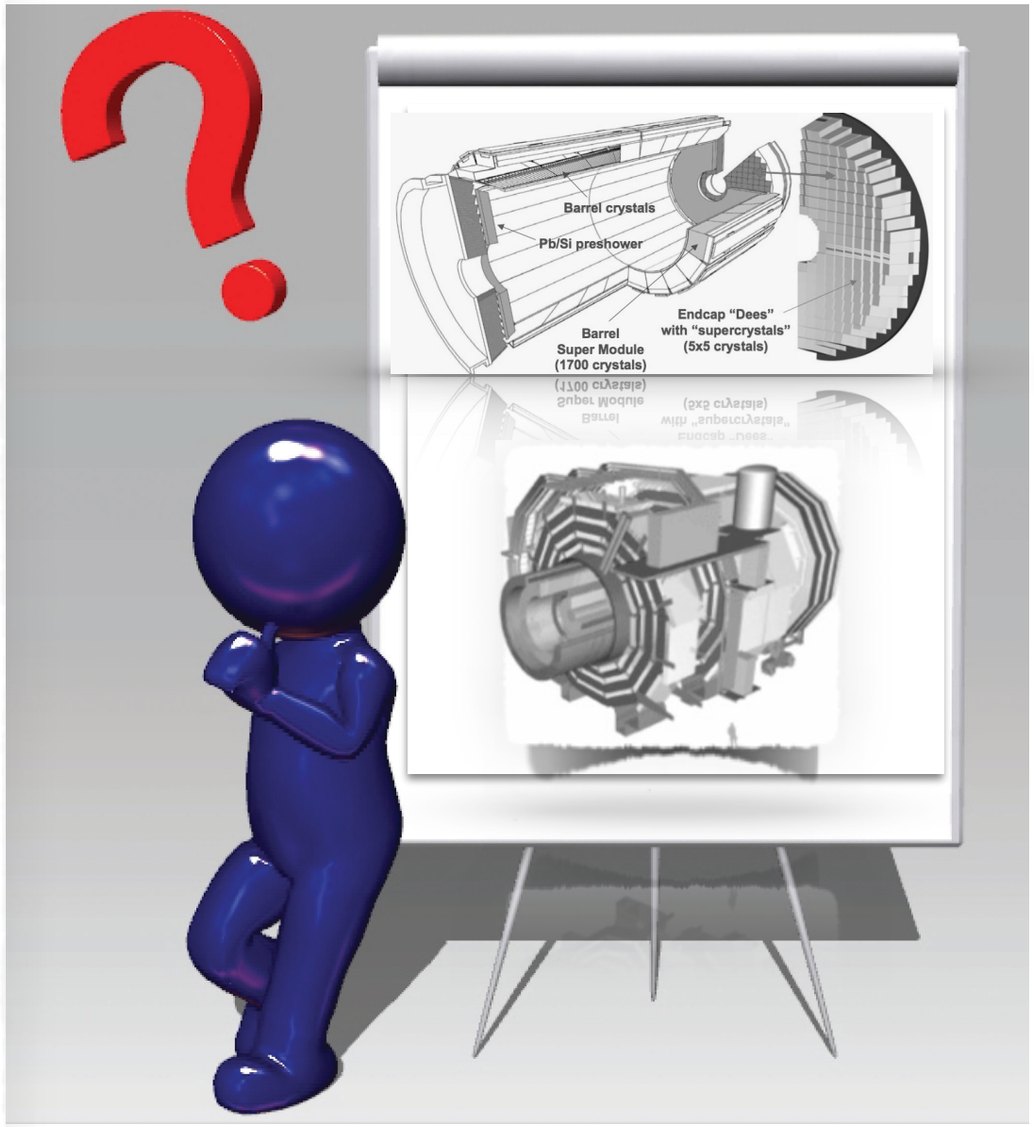
Tests of DC-DC converters

Patrizia Barria

University of Virginia

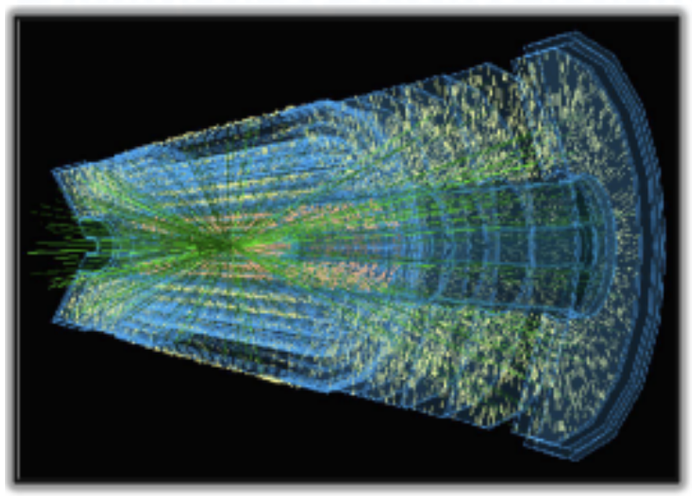
OUTLINE

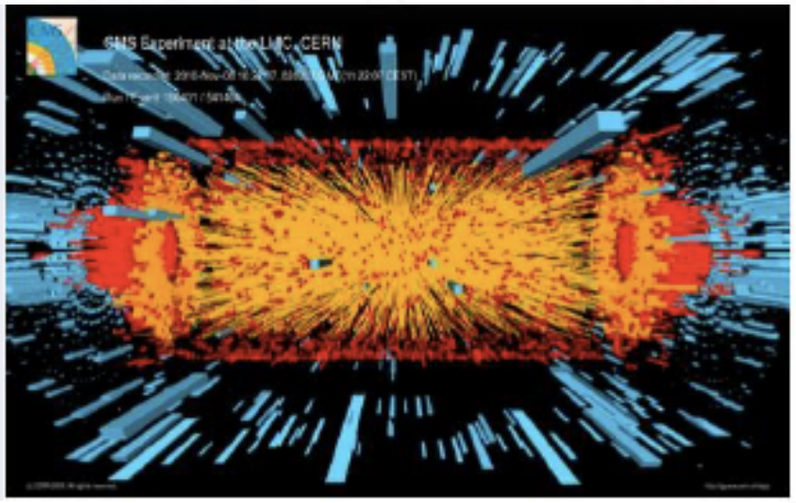
- *Introduction*
  - *LHC and HL-LHC*
    - *CMS and ECAL Phase II barrel upgrades*
- *Preliminary test of DC-DC converters @UVa*
- *UVa's future plans and status of the art*
- *Conclusions*



LHC AND HL-LHC

	LHC	HL-LHC
Instantaneous luminosity [$cm^2\ s^{-1}$]	10^{34}	$7x10^{34}$
Number of events per BC at 25 ns	28	≈ 200
Number of events per BC at 50 ns	56	≈ 400
Integrated luminosity [fb^{-1}]	300	3000



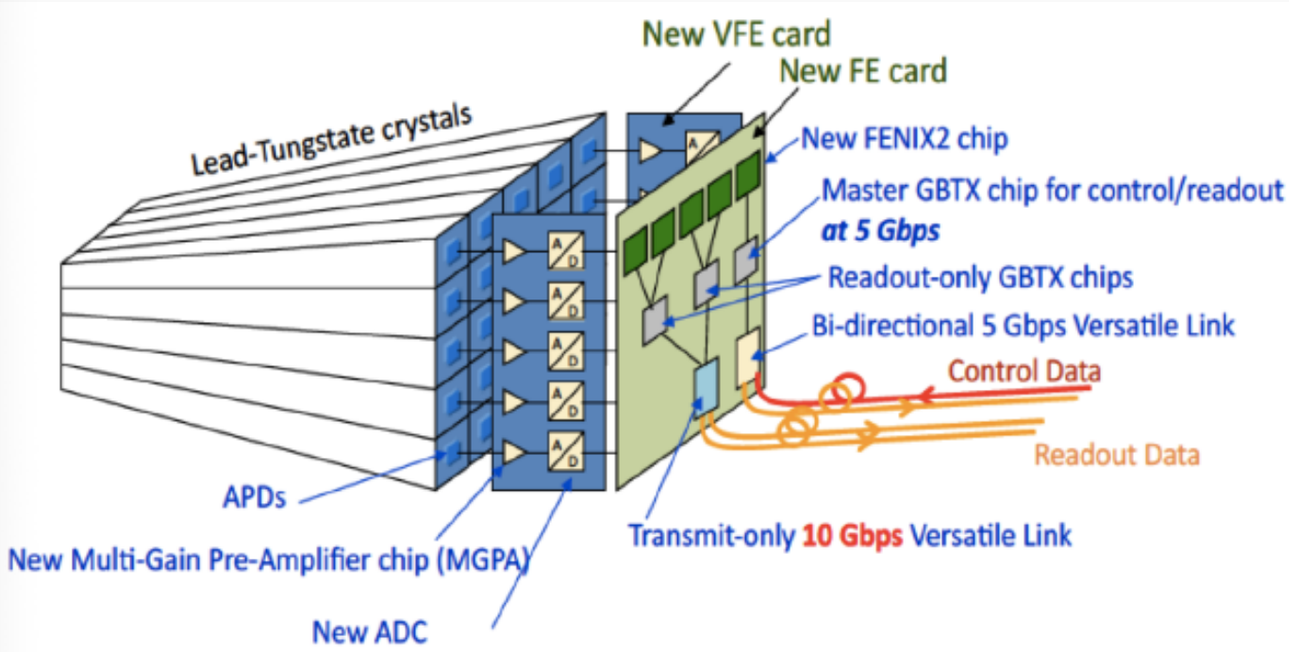


CMS is planning significant upgrades for Phase II

- *Motivations:*
  - *Radiation resistance: replace components with more radiation-tolerance to sustain 3000 fb^{-1}*
  - *Ageing: some components would have ~30 yrs operation, difficult to maintain and repair*
  - *Provide highest granularity information and resolution: efficient and selective triggers at high lumi*

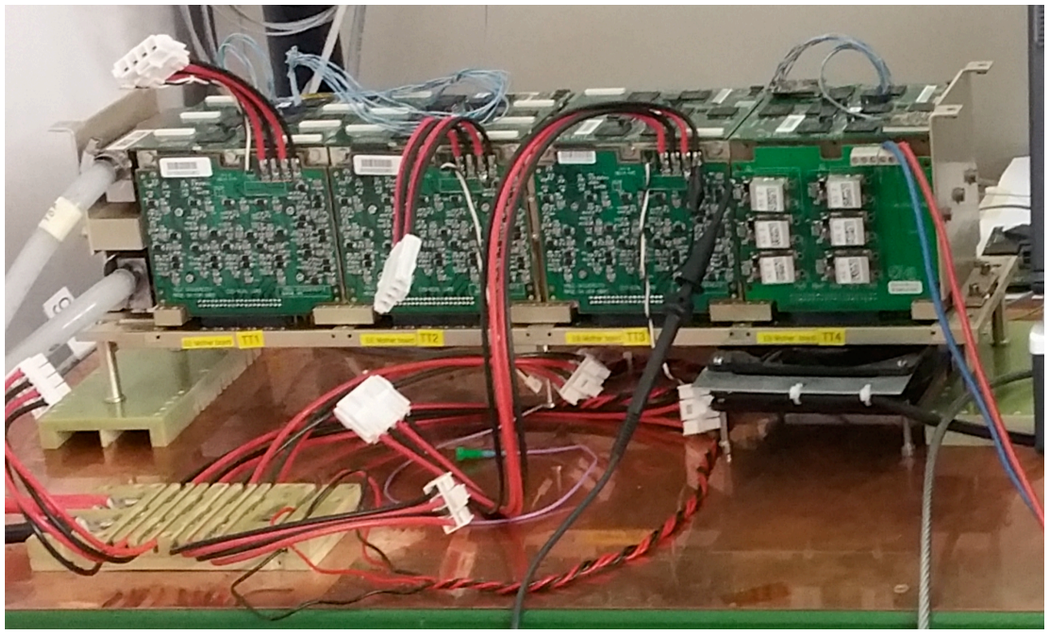
ECAL PHASE II BARREL UPGRADES

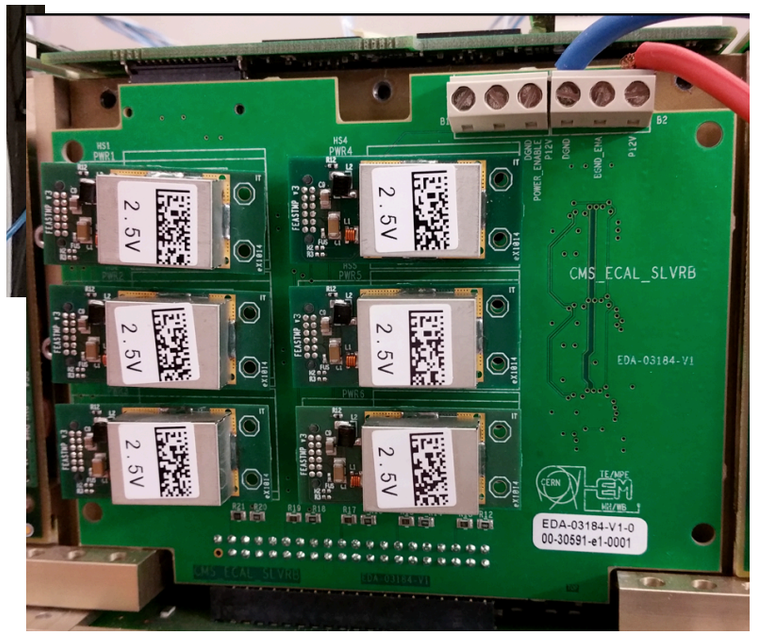
- *Remove all 36 super-modules, replace FE cards + services (power, electrical signals, opto-links, cooling)*
  - *Decrease volume of services on YB0 in order to make the re-cabling easier → E.g. by decreasing the LV current to the EB Front End by using DC-DC converters on the LVRB (switching sLVRB= Low Voltage Regulator Board) thus using less cables*
- *New FE card:*
  - *Remove all L1 crystal sums, remove buffer, send all data out @40 MHz (TRIGGER)*
  - *CERN GBTx/Versatile link for data transfer to back-end and control*
  - *will need 10 Gbps rad-tolerant link*
- *New VFE card:*
  - *Change preamp shaper, ADC*
- *New back-end:*
  - *Evolution of MP7 μTCA board as developed for Phase I Trigger based on FPGA Xilink Virtex 7*



SLVR CARD

- *SLVR card hosts 6 FEASTMP modules. Voltages and currents are monitored via 3 DCU ASICS*
- *Testing the card concerns:*
  - *Testing the proper functioning of the installed FEASTMP modules and of the DCUs in the assembled card*
  - *The performance of the card as part of the detector front-end readout system has to be evaluated/repeated with every version of the front-end electronics*
  - *Reliability and safe operation: card is installed inside the ECAL barrel super modules and maintenance during the life-cycle planned for the detector is excluded*

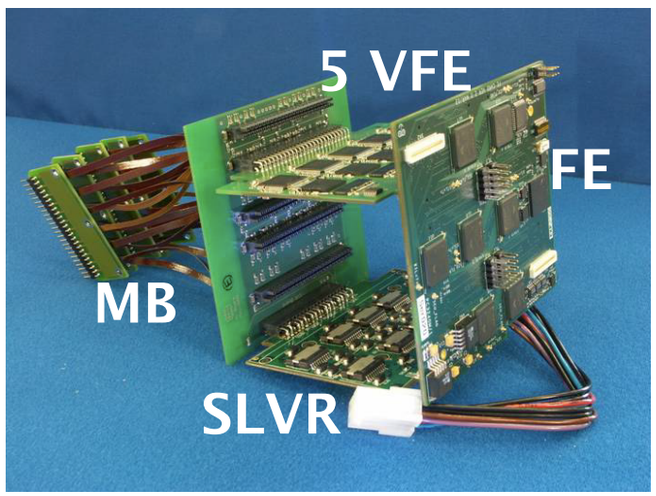




ELECTRICAL CHARACTERIZATION

ELECTRICAL CHARACTERIZATION:

- *Output voltage:*
  - *measure the value*
  - *measure stability as a function of:*
    - *temperature*
    - *radiation*
  - *measure noise*
  - *output voltage as function of load/input voltage*
- *DCUs:*
  - *functionality of all DCU ADC channels*
  - *precision of DCU measurements*
- *monitor temperature*



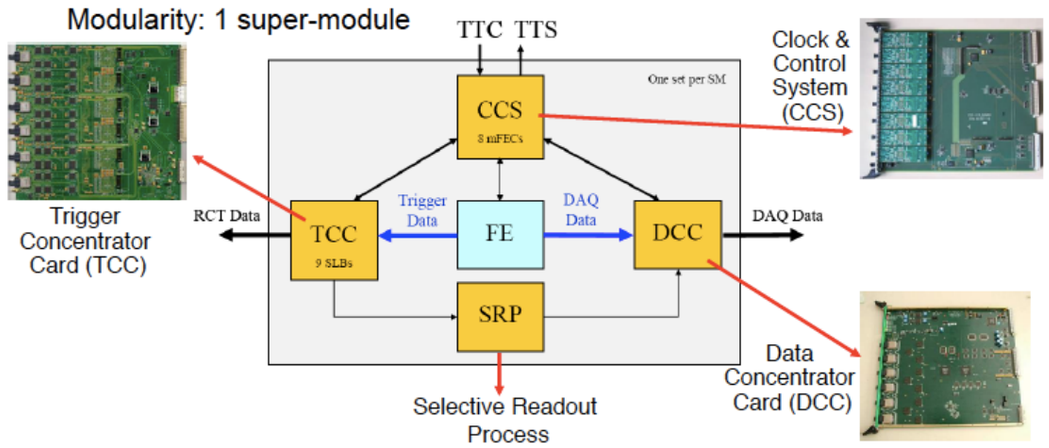
ON DETECTOR ELECTRONICS

Modularity: Trigger Tower – it reads a 5x5 grid of crystals:
- 5 VFEs (Very Front End cards) - each one reads a strip of 5 crystals along φ
- 1 FE (Front End card) – it controls and receives data from the 5 VFEs
- 1 LVR (Low Voltage Regulator card) – it stabilizes and distributes the LV
- 1 MB (Mother Board) – it distributes the HV and provides connections to the VFEs.

On the FE:
- 2 GOHs (Gigabit Optical Hybrids) – to send out data and trigger primitives
- 1 CCU (Clock & Control Unit) – I^2C interface.

The 68 FEs on a super-module are connected by a system of 8 Token Rings.

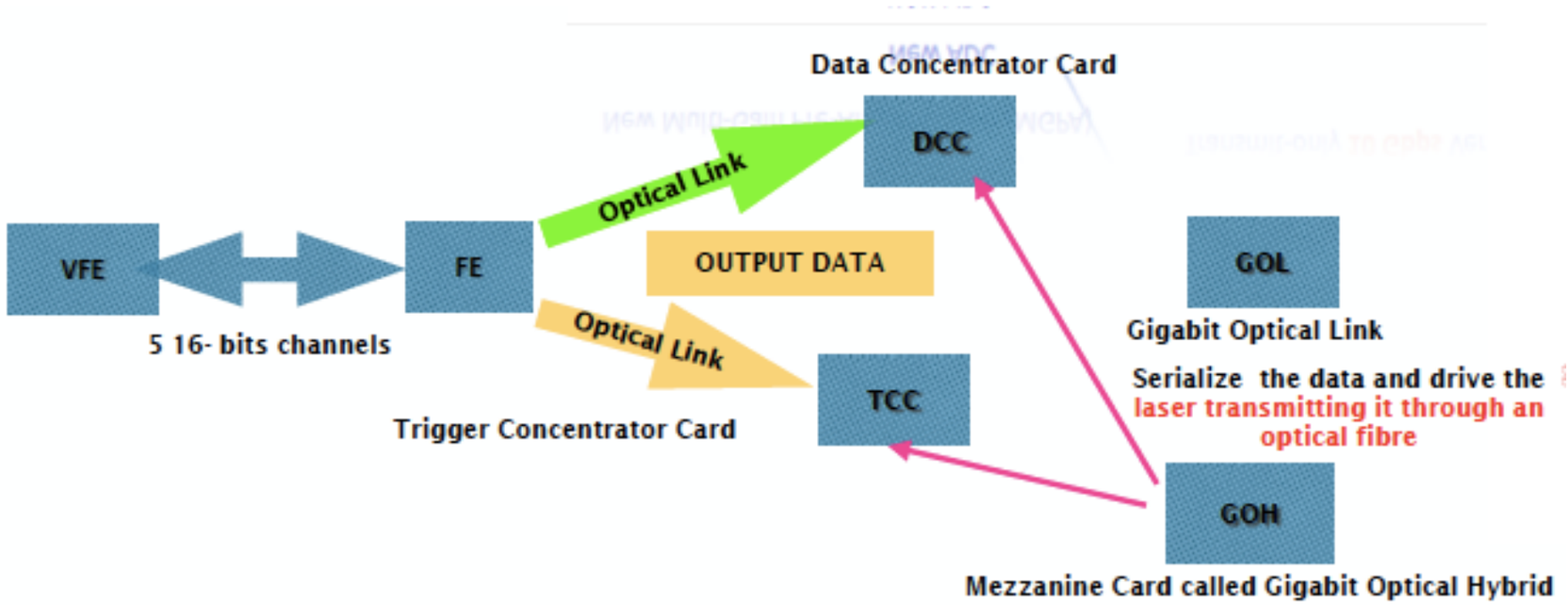
OFF DETECTOR ELECTRONICS



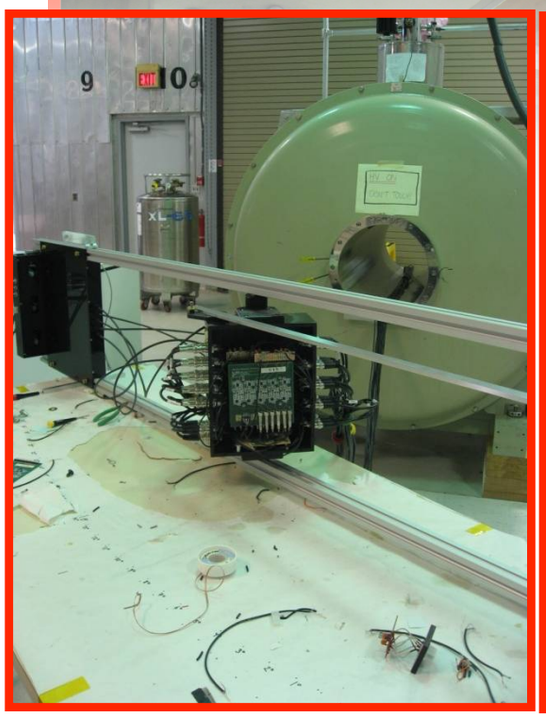
Main functions of the off-detector electronic boards:
- CCS: reception/distribution of LHC clock and control signals + front-end initialization
- TCC: encoding of trigger primitives and transmission to Regional Calorimeter Trigger at 40 MHz + classification of trigger tower importance and transmission to SRP at Level 1 rate
- DCC: integrity check + data reduction + transmission to central DAQ at Level 1 rate

UVa PLANNED STUDIES

- *To characterize the DC-DC converters as well as the front end and the assembly performance under temperature, magnetic field and radiation stresses*
- *To measure the noise generated between the VFE boards*
- *To do the temperature tests in the range between 0 and 18 degrees*
- *The configuration of the Trigger tower and temperature variance environmental box that we need to do 3.8 T test in the UVa superconducting magnet simultaneously with varying the temperature range*
- *We will follow these tests with some radiation testing most likely at UC Davis, Los Alamos or Sandia Lab*
- *If needed, we will do temperature torture testing of the Tower electronics assembly*
- *Finally, we will repeat the desired sequence of test as different versions of the VFE, DC-DC converter and FE card evolve*



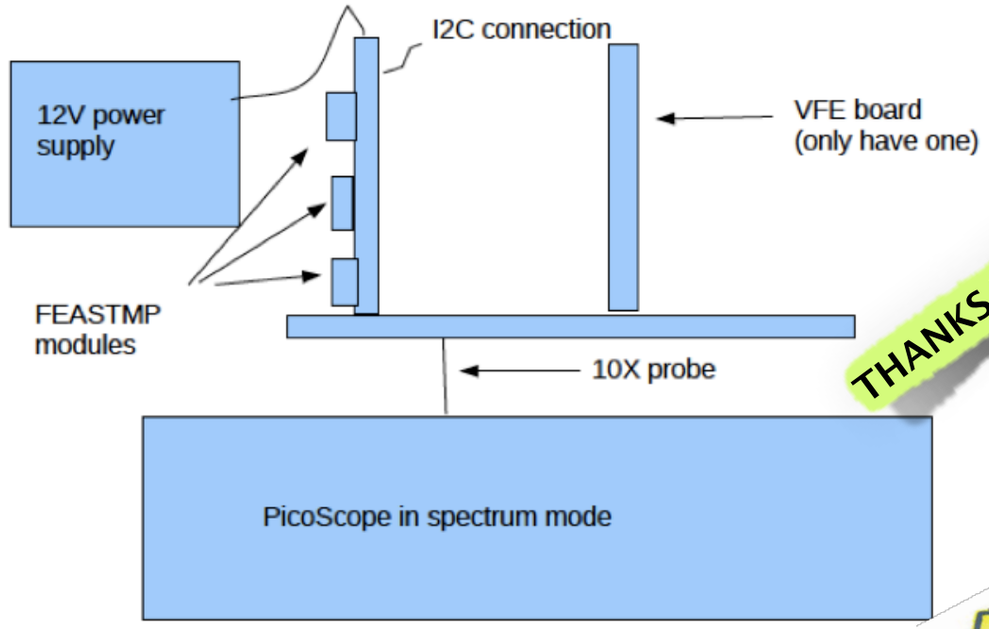
UVa 3.8 T SUPERCONDUCTING MAGNET



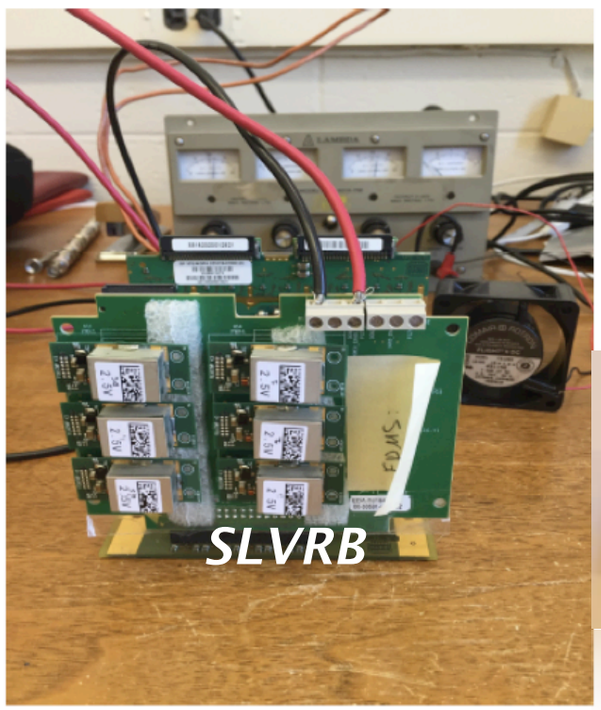
- *The UVa's large-bore superconducting magnet is capable of 4.7 T*
- *Aperture diameter 40 cm*
- *20-year-old beast that began its life in the university hospital's MRI lab.*
  - *for testing vacuum phototriodes (VPTs) (the ECAL endcap photodetector) at <u>various angles</u> in a 3.8 Tesla field*
  - *Increased range of angle scans from +/- 13˚ to +/- 25 ˚*
  - *Using the same amplifiers that comprise the CMS ECAL endcaps for more realistic reproduction of measurement conditions*
- *Upgraded from a CAMAC/NIM measurement and timing system to a National Instruments PXI rig with:*
  - *FGPA based Timing control down to 25 ns*
  - *2 GHz Digital Scope for precise waveform readout*
  - *reduced noise*
- *Other additions/upgrades*
  - *Temperature and Humidity Monitoring*
  - *Amplifier gain monitoring*

UVa PRELIMINARY TESTS: SETUP

- *UVa's "minimal"setup:*
  - *1 DC-DC converter board*
  - *6 DC-DC converter chips (FEASTMP modules)*
  - *1 VFE board:*
    - *board was provided low voltage by the DC-DC converter board with six FEASTMP chips:*
      - *Five FEASTMP chips were used provided 2.5 V to the VFE board*
      - *the other FEASTMP chip powered the DC-DC board itself*
- *GOAL: to measure the noise generated by each of the six DC-DC converter chips on the DC-DC converter board*

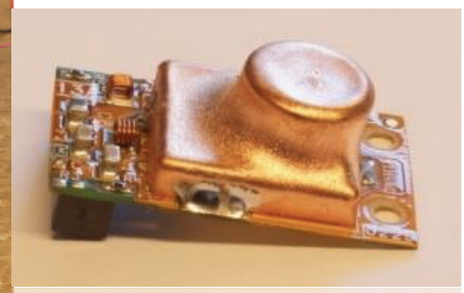


THANKS TO MIKE ARENTON



Input 12 volts

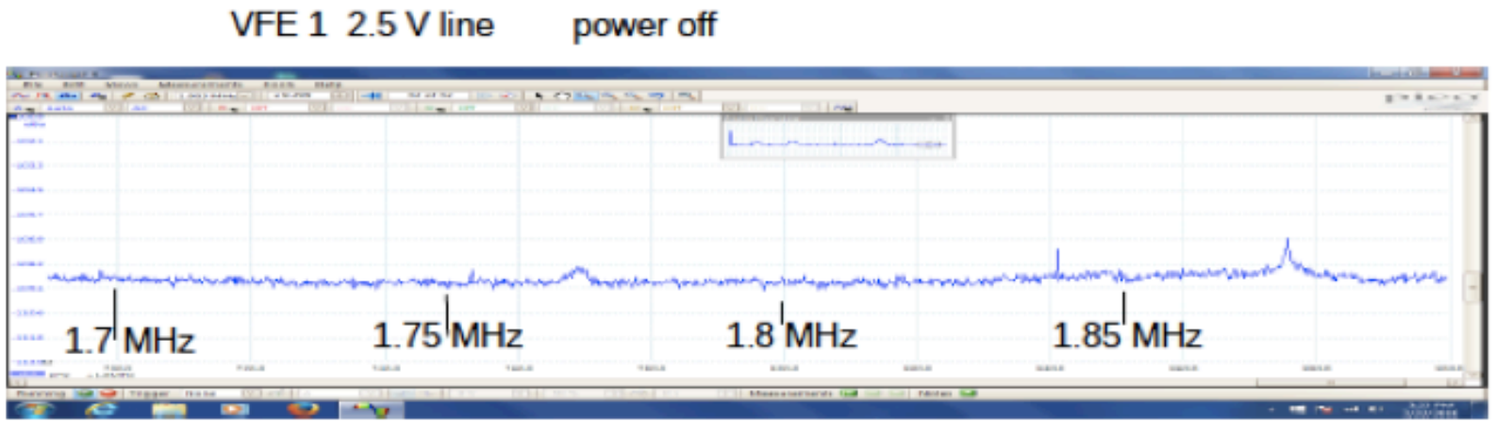
With one VFE board plugged in it draws 0.7 amps from power supply.



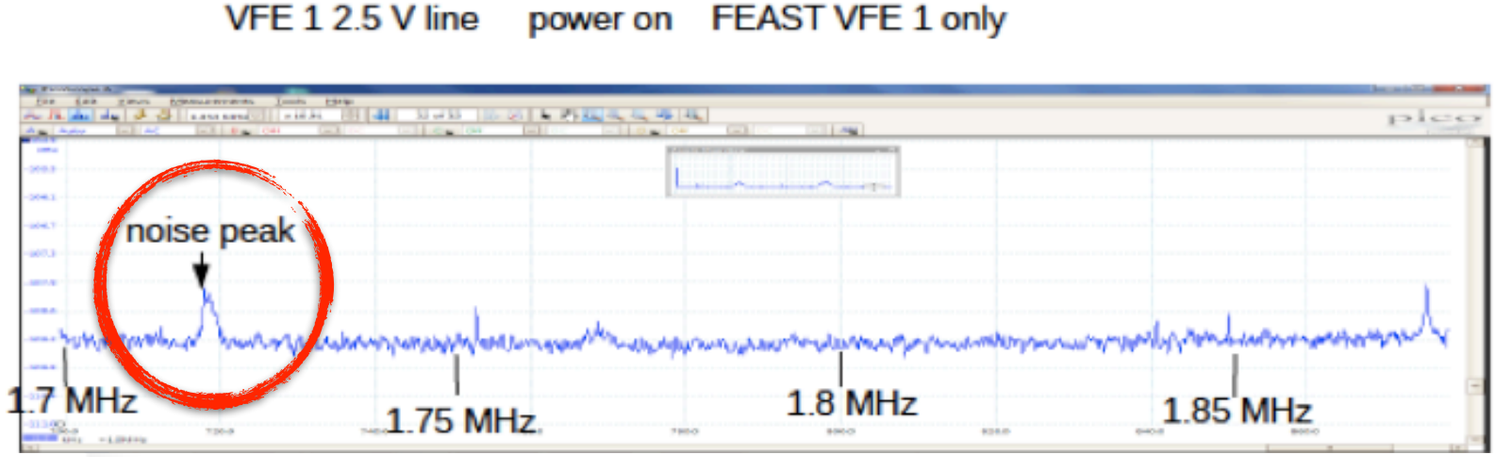
DC-DC CONVERTER

UVa PRELIMINARY TESTS: MEASUREMENTS

- *The noise from the FEASTMP chips is expected to show up at ~1.8 MHz*
- *Some "environmental" noise: so compare the spectrum with power-off to that with only one FEASTMP module at a time plugged in*
- *Noise from each FEASTMP chip measured with only one of the FEASTMP module in place and powered at a time and compared with the power-off noise spectrum*
- *Noise spectra measured on the DC power lines leading to the VFE card*



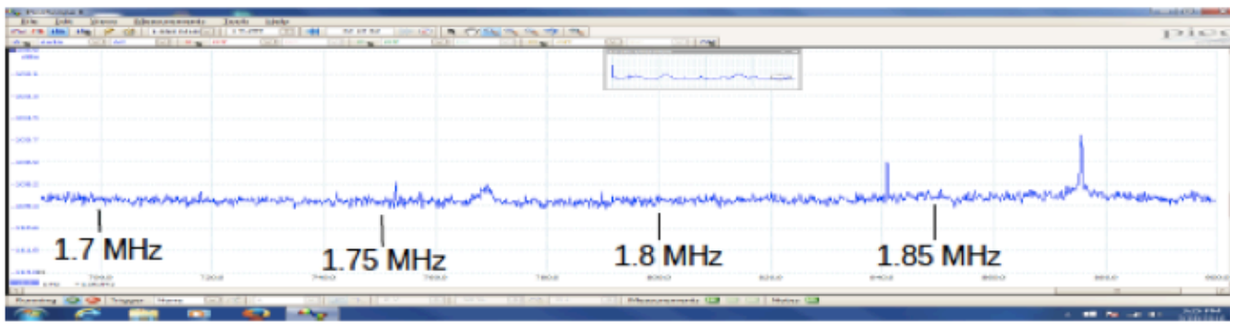
Power-off compared to Power-on noise spectrum FEASTMP chip



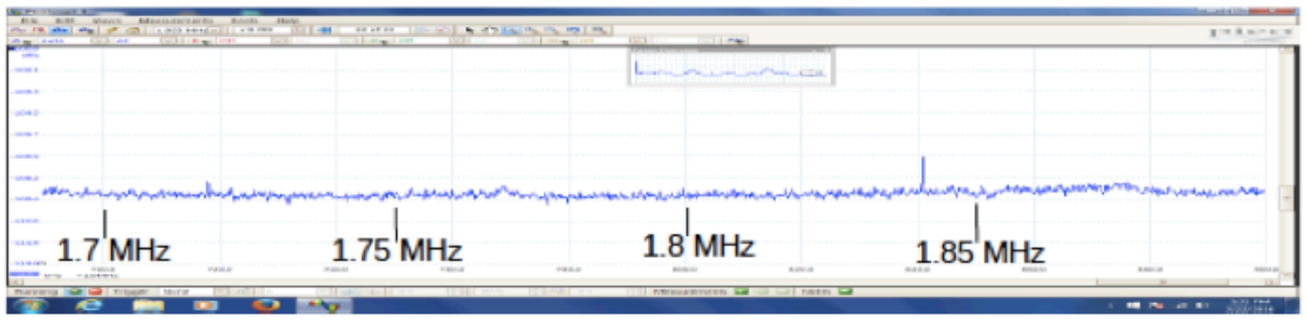
UVa PRELIMINARY TESTS: MEASUREMENTS

Power-off compared to Power-on noise spectrum FEASTMP chip 2

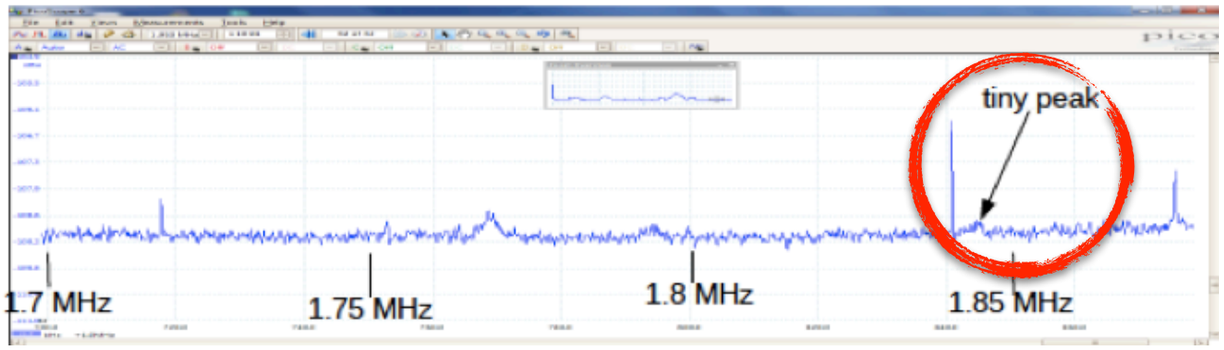
VFE 2 2.5V line power off



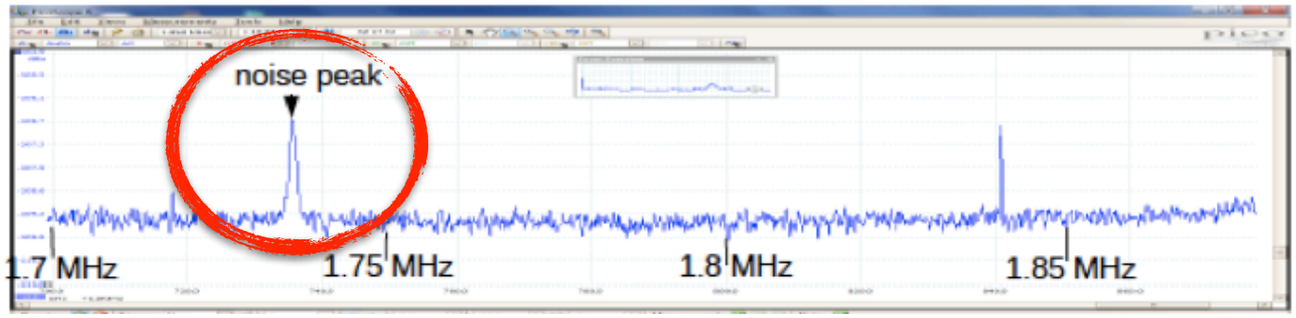
VFE 3 2.5V line power off



VFE 2 2.5 V line power on FEAST in VFE 2 slot



VFE 3 2.5V line power on FEAST in VFE 3 slot



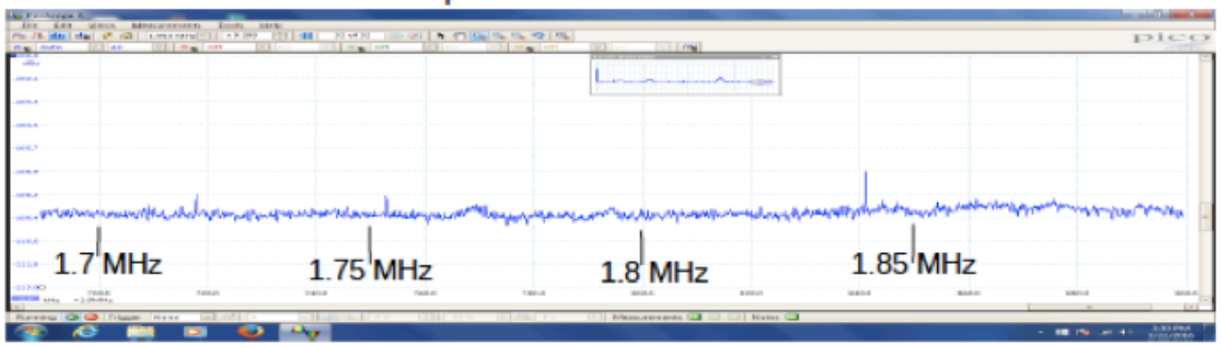
Power-off compared to Power-on noise spectrum FEASTMP chip 3

Note: the horizontal scale not quite the same for the power-off and power-on cases. The frequency range of the measurements is from approximately 1.6 to 1.9 MHz.

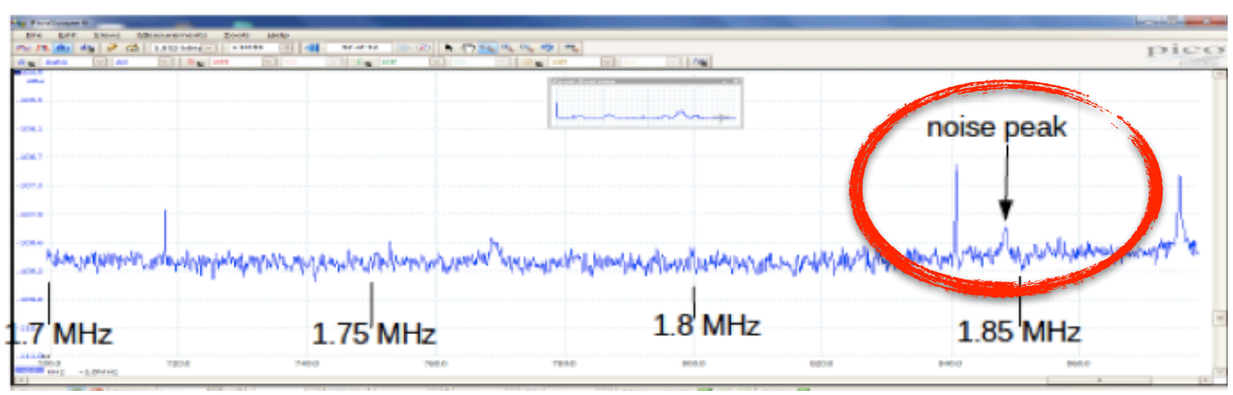
UVa PRELIMINARY TESTS: MEASUREMENTS

Power-off compared to Power-on noise spectrum FEASTMP chip 4

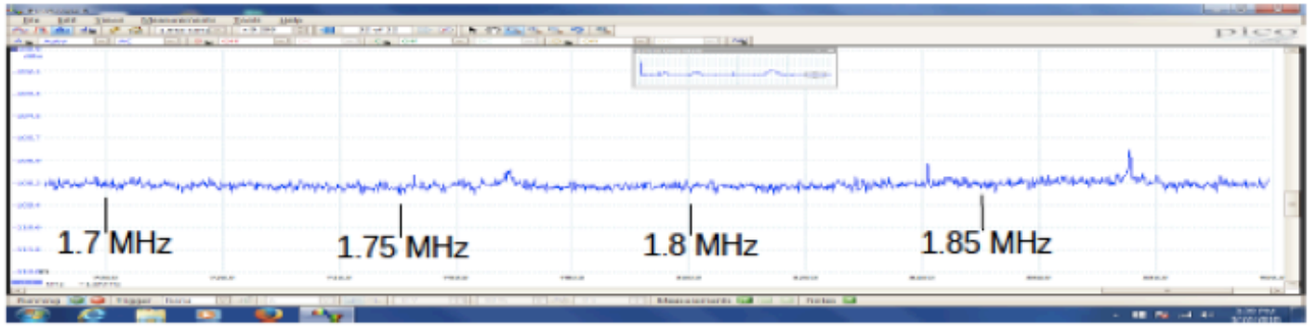
VFE 4 2.5V line power off



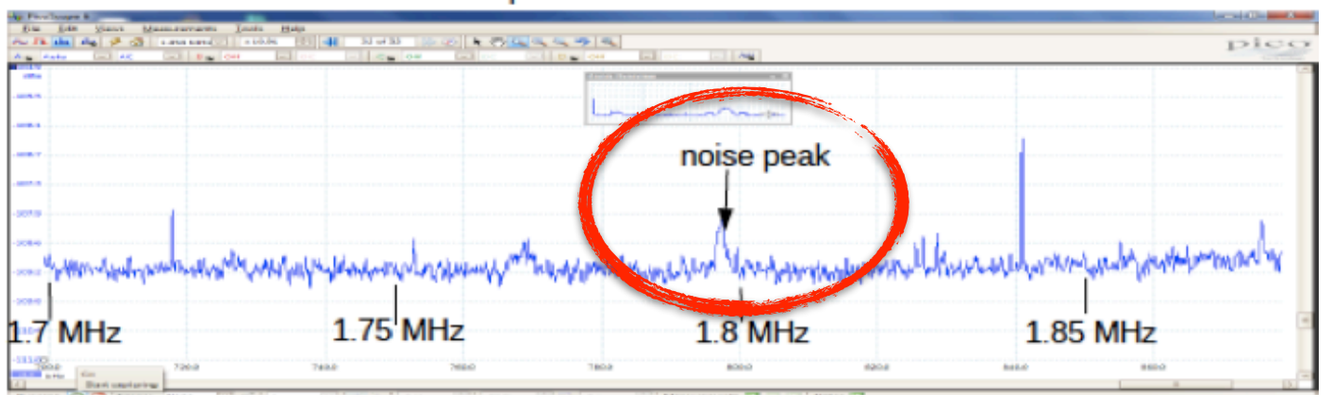
VFE 4 2.5 V line power on FEAST in VFE 4 slot



VFE 5 2.5V line power off



VFE 5 2.5 V line power on FEAST in VFE 5 slot

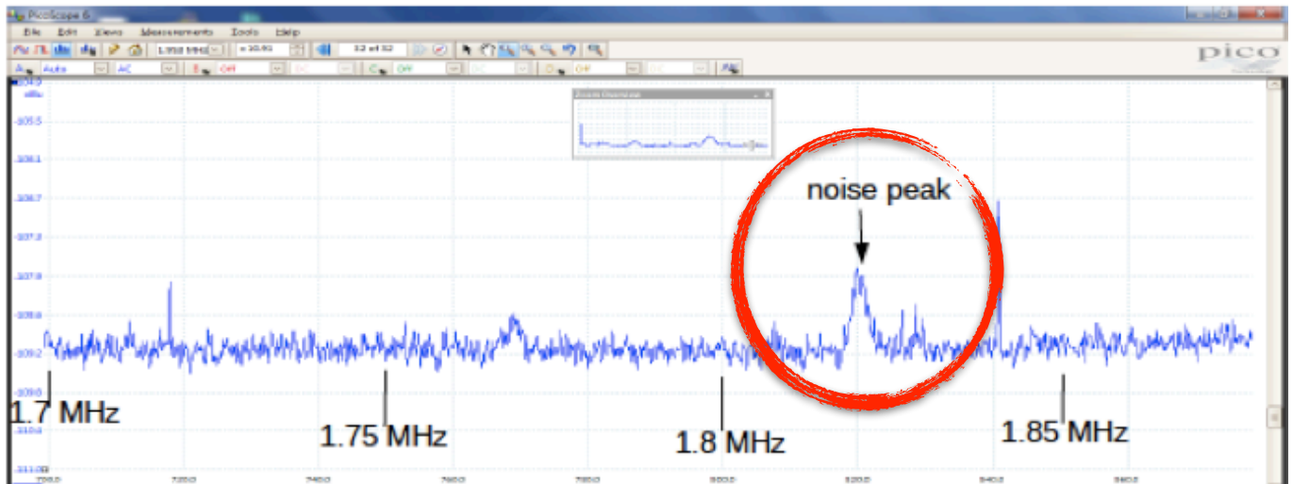


Power-off compared to Power-on noise spectrum FEASTMP chip 5

UVa PRELIMINARY TESTS: MEASUREMENTS

Power-off compared to Power-on noise spectrum FEASTMP chip 6

VFE 5 2.5 V line, power on "DC-DC" FEAST in VFE 5 slot



FREQUENCY OF THE NOISE PEAKS FROM EACH CHIP

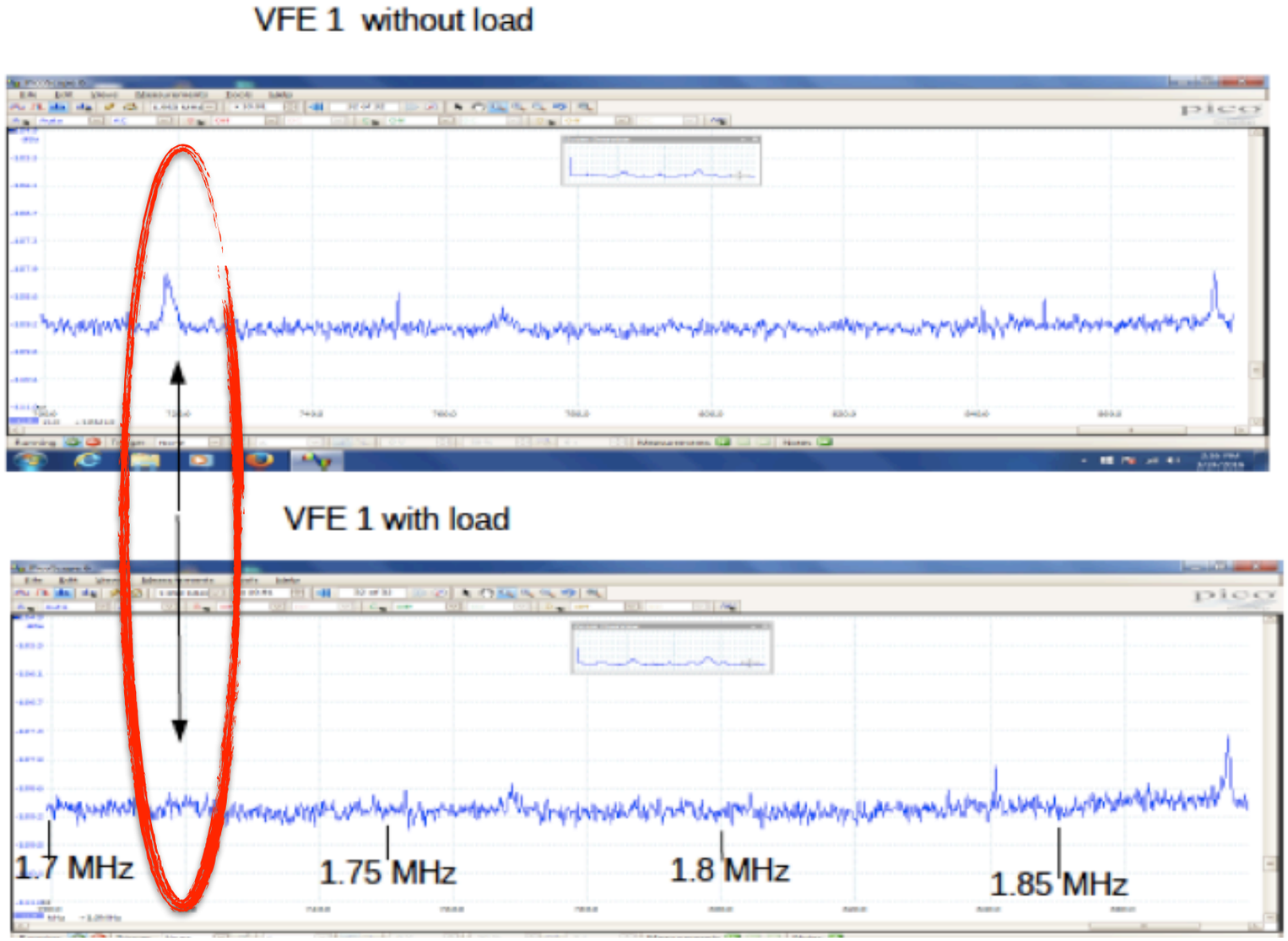
VFE CHANNEL	FREQUENCY (MHz)
VFE 1	1.719
VFE 2	1.845
VFE 3	1.735
VFE 4	1.848
VFE 5	1.795
DC-DC BOARD	1.821

- *All 6 DC-DC converter chips have slightly different frequencies, close to but significantly different from 1.8 MHz.*
  - *One of the chips generated larger noise on the power lines than the other five.*
- *As well as measuring the noise on the DC lines, we have tried to measure the resulting noise on the VFE card at a point between the amplifier chips and the ADC chip ➜ not able to detect any noise signal at the frequency of the FEASTMP noise to date*

NOISE PEAK: DIFFERENCES wrt THE LOAD FROM THE VFE CARD

Is the noise peak different with the load imposed by the VFE card?

- *Power-on vs. power-off measurements were made on the power lines for load and no-load and for each FEASTMP chip.*
- *The arrows show the positions of the noise peaks from the FEASTMP chips*

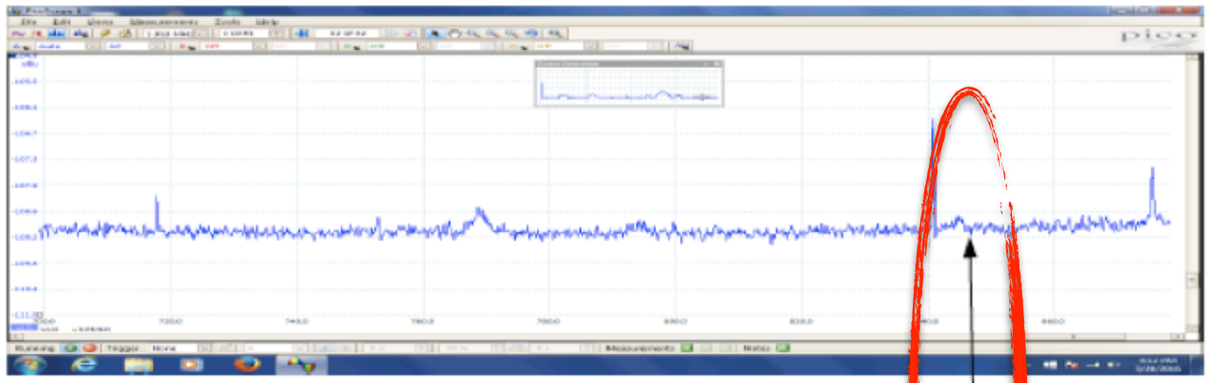


No VFE load is compared to VFE loaded noise spectrum FEASTMP chip 1

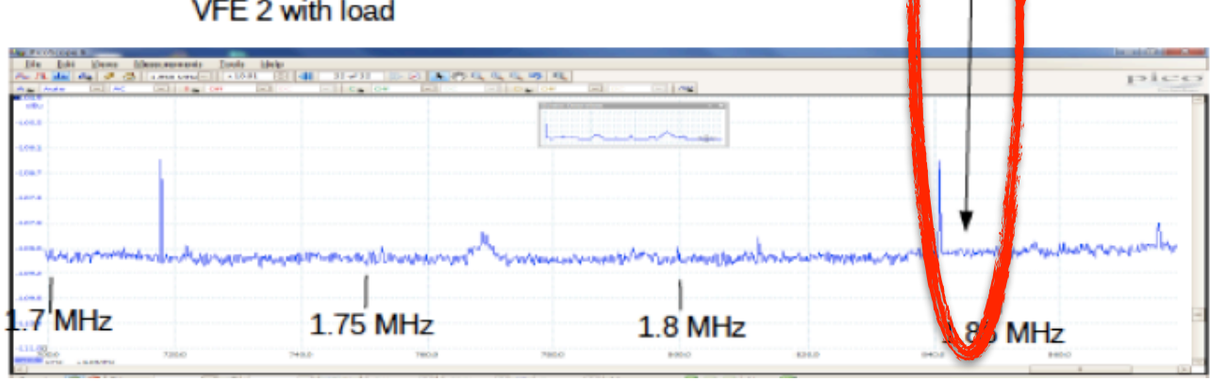
UVa PRELIMINARY TESTS: RESULTS

No VFE load is compared to VFE loaded noise spectrum FEASTMP chip 2

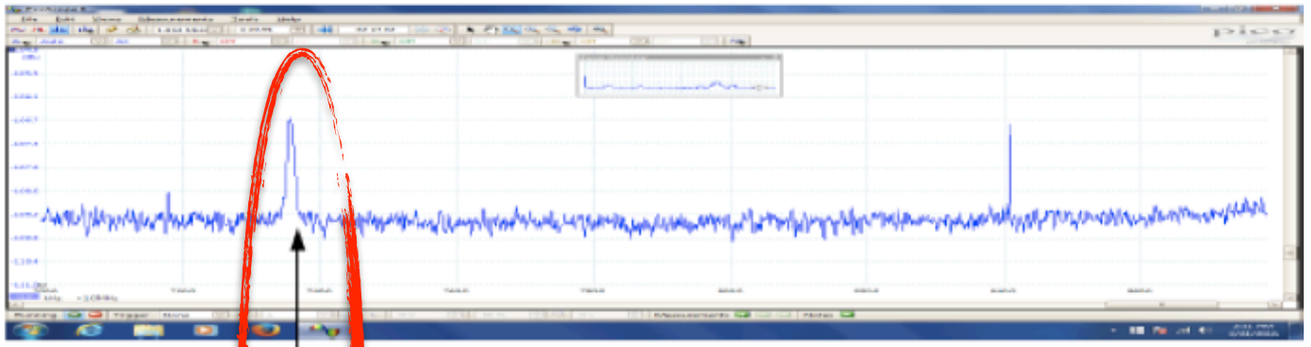
VFE 2 no load



VFE 2 with load



VFE 3 no load



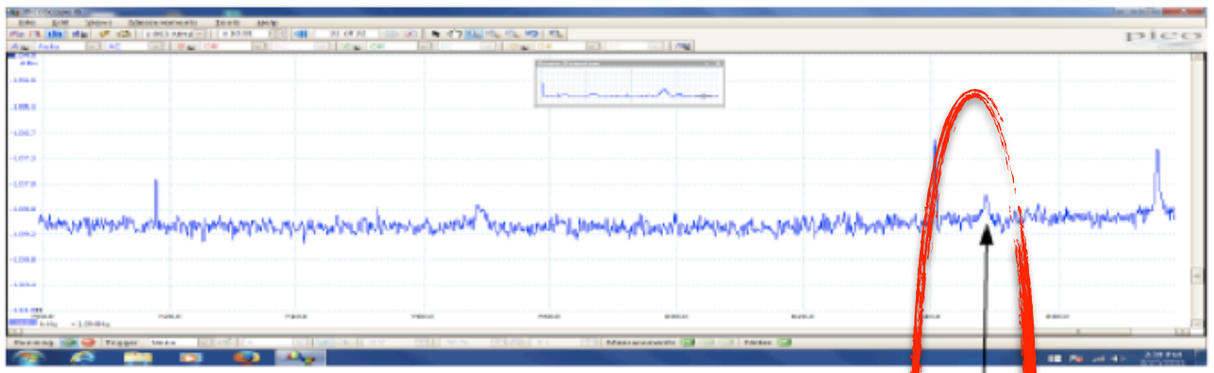
VFE 3 with load

No VFE load is compared to VFE loaded noise sspectrum FEASTMP chip 3

UVa PRELIMINARY TESTS: RESULTS

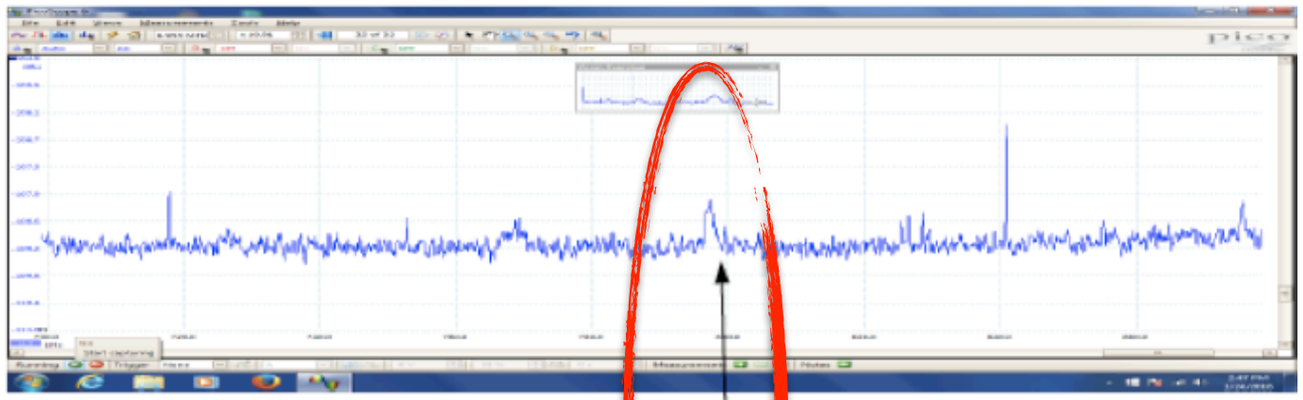
No VFE load is compared to VFE loaded noise spectrum FEASTMP chip 4

VFE 4 no load

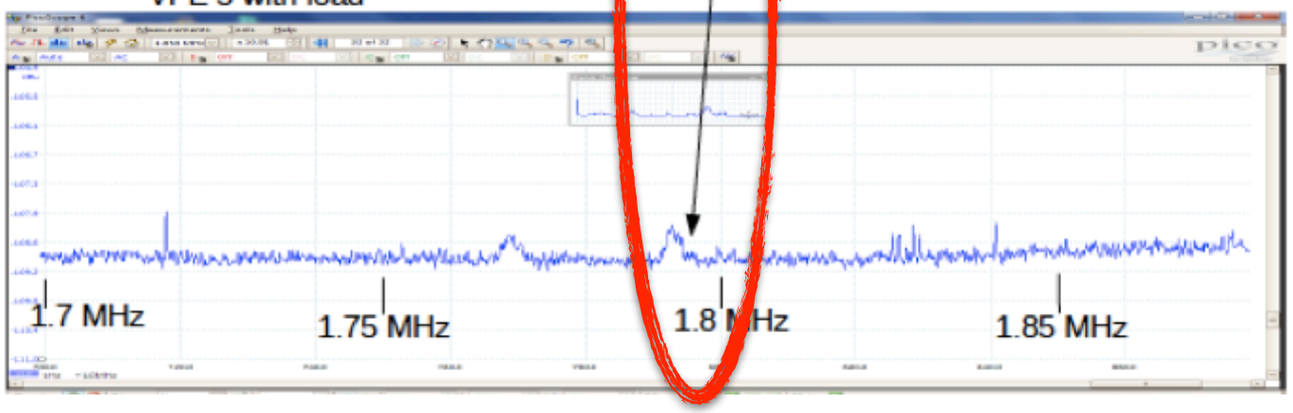


VFE 4 with load

VFE 5 no load



VFE 5 with load

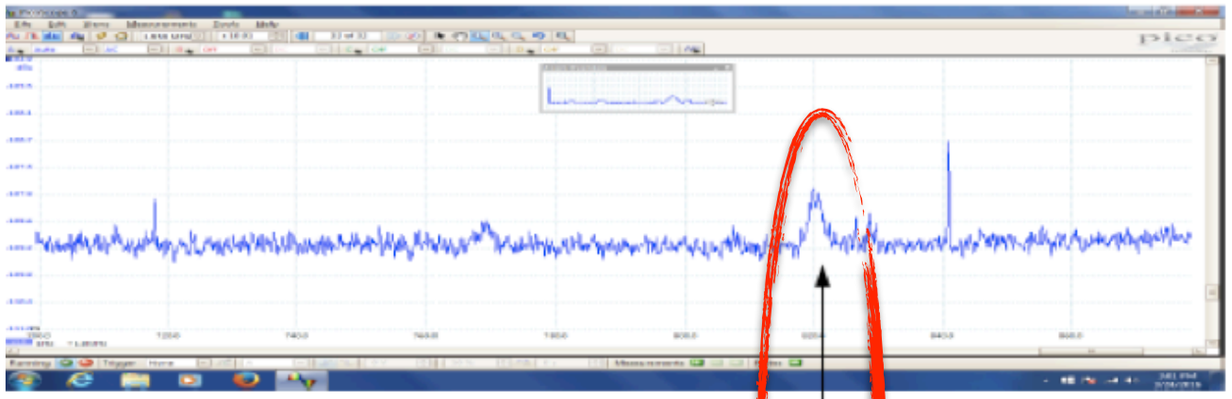


No VFE load is compared to VFE loaded noise spectrum FEASTMP chip 5

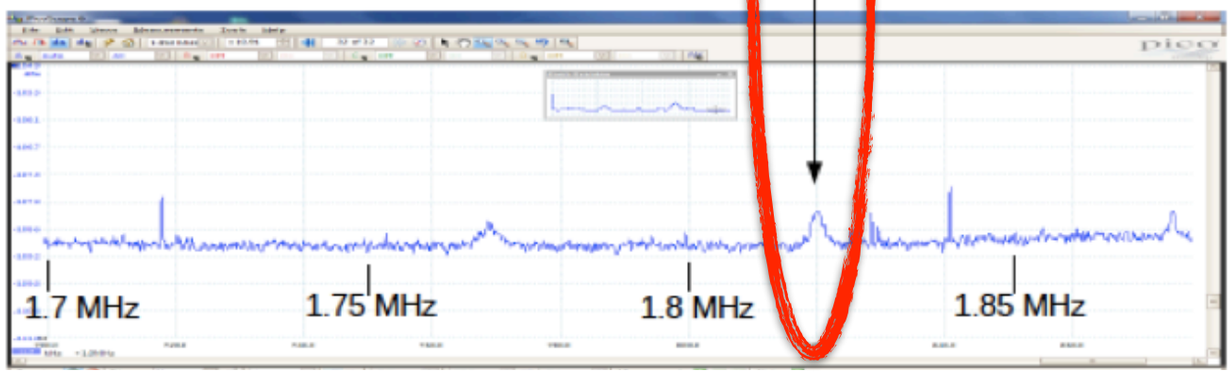
UVa PRELIMINARY TESTS: RESULTS

No DC-DC load is compared to DC-DC loaded noise spectrum

"DC-DC" no load



"DC-DC" with load



NOISE PEAK AMPLITUDE VFE NO- LOAD vs VFE LOAD

VFE CHANNEL	VFE NO-LOAD AMPLITUDE (dBu)	VFE LOADED AMPLITUDE (dBu)
VFE 1	-108.2	NOT VISIBLE
VFE 2	-108.8	NOT VISIBLE
VFE 3	-106.6	-108.8
VFE 4	-108.3	-108.3
VFE 5	-108.1	-108.2
DC-DC	-107.8	-108.2

- *The effect of applying the VFE load seems to decrease significantly the observed noise on two of the power lines but leave the noise unchanged on the remaining four*
- *We will need to fully load the mother board with VFE cards to get a better sense of what is going on ➜ for these tests we only had one VFE card*

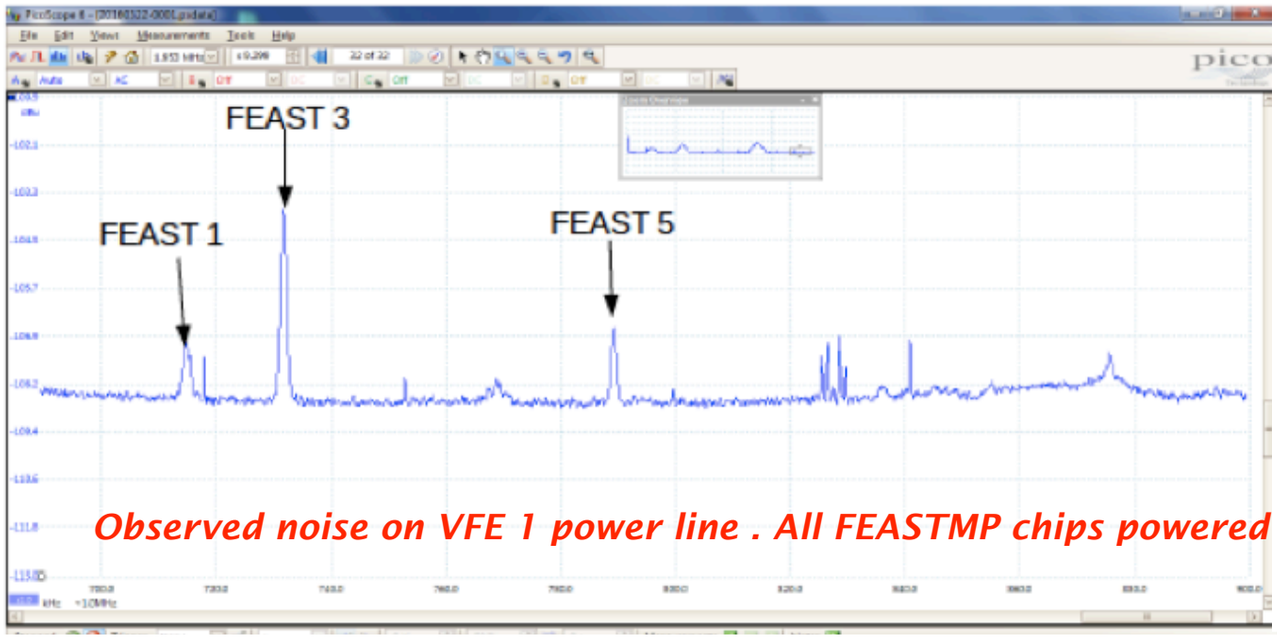
UVa PRELIMINARY TESTS: RESULTS

Possible existence of cross talk: does the noise show up on the other 2.5V lines when all the FEASTMP chips are plugged in?

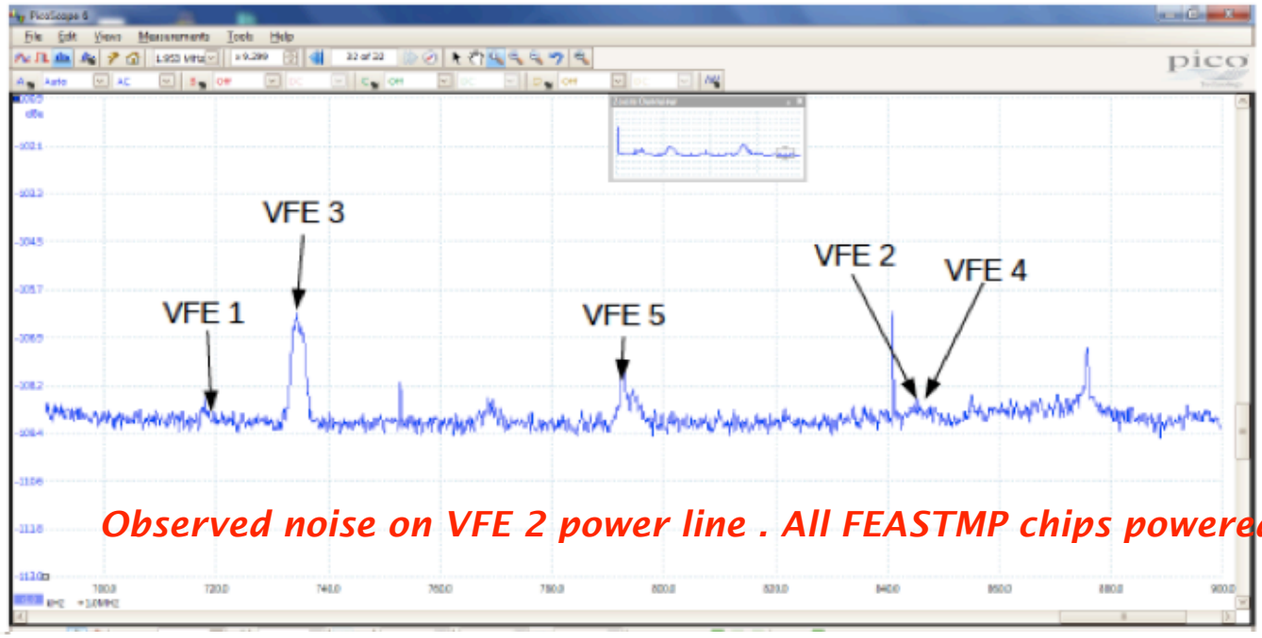
- *This was investigated by measuring the noise on lines other than the ones that are powered by each individual FEASTMP chip.*

VFE 1 2.5V line power on no load (i.e. no VFE card in any slot)

VFE 2 2.5V line power on no load



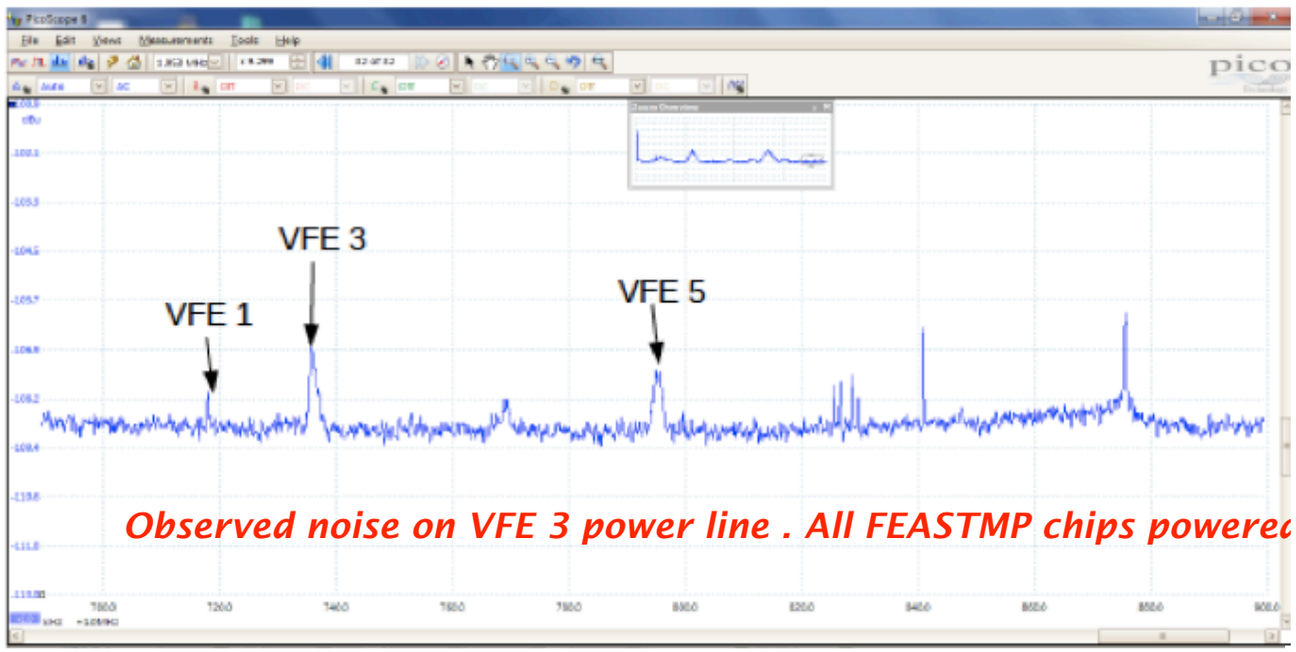
Observed noise on VFE 1 power line . All FEASTMP chips powered



Observed noise on VFE 2 power line . All FEASTMP chips powere

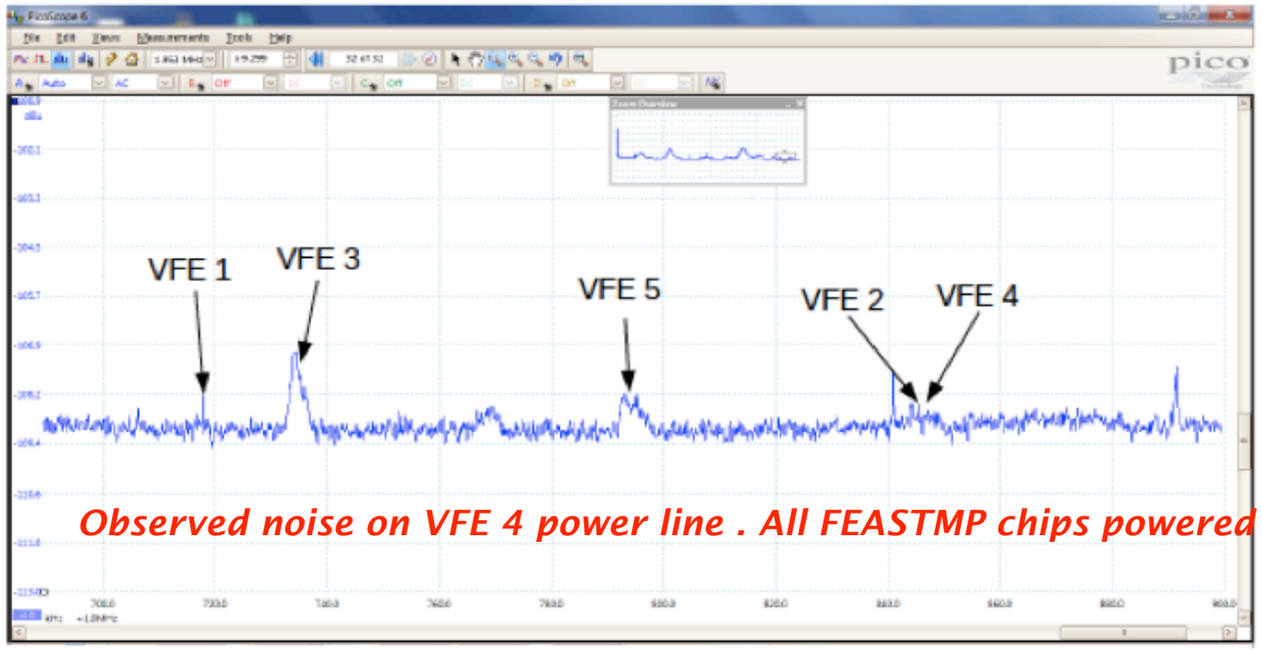
UVa PRELIMINARY TESTS: RESULTS

VFE 3 2.5V line power on no load



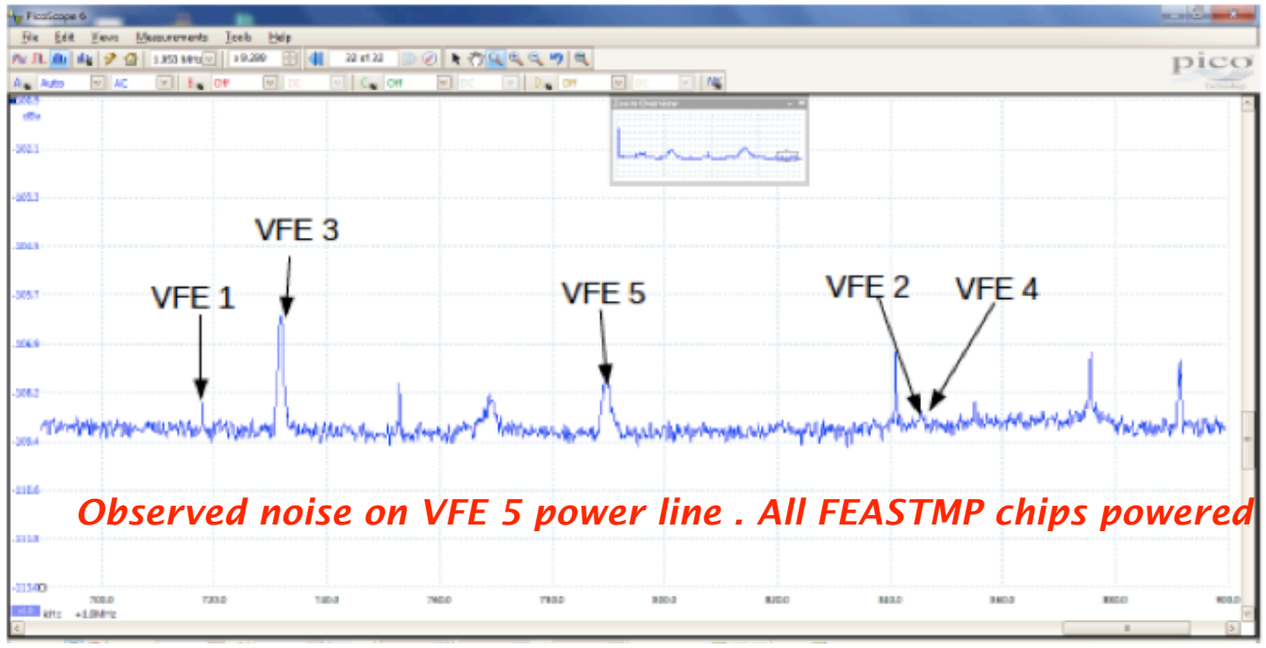
Observed noise on VFE 3 power line . All FEASTMP chips powered

VFE 4 2.5V line power on no load



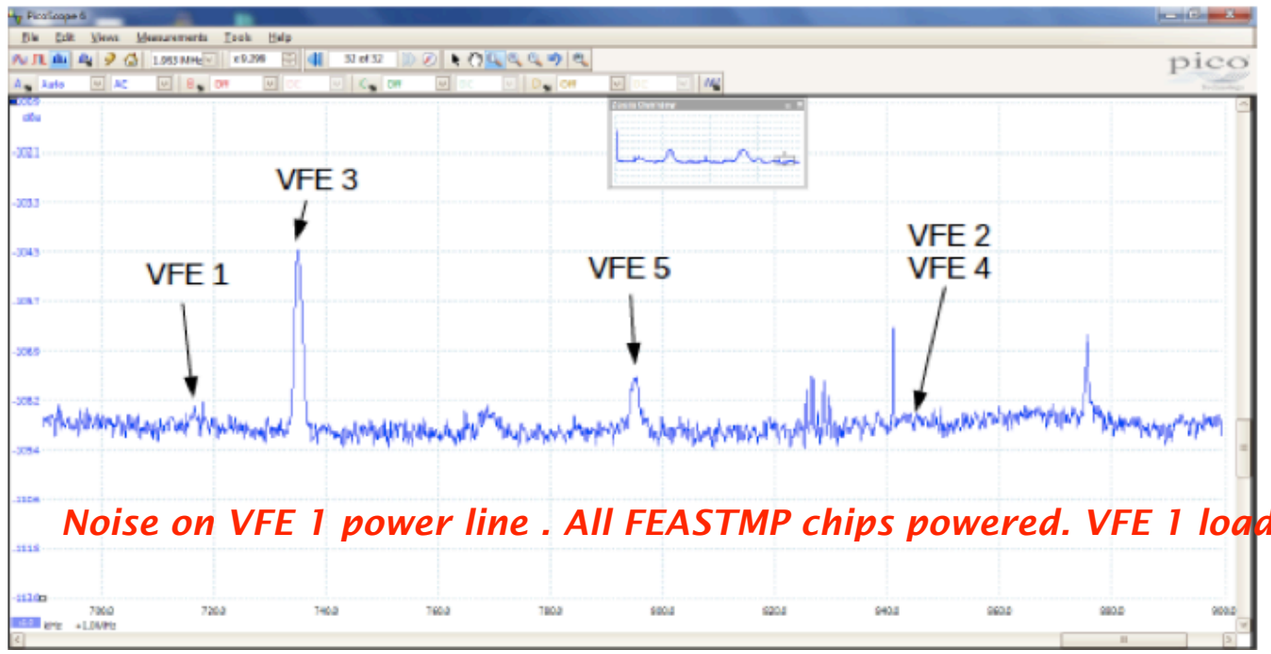
Observed noise on VFE 4 power line . All FEASTMP chips powered

VFE 5 2.5V line power on no load



Observed noise on VFE 5 power line . All FEASTMP chips powered

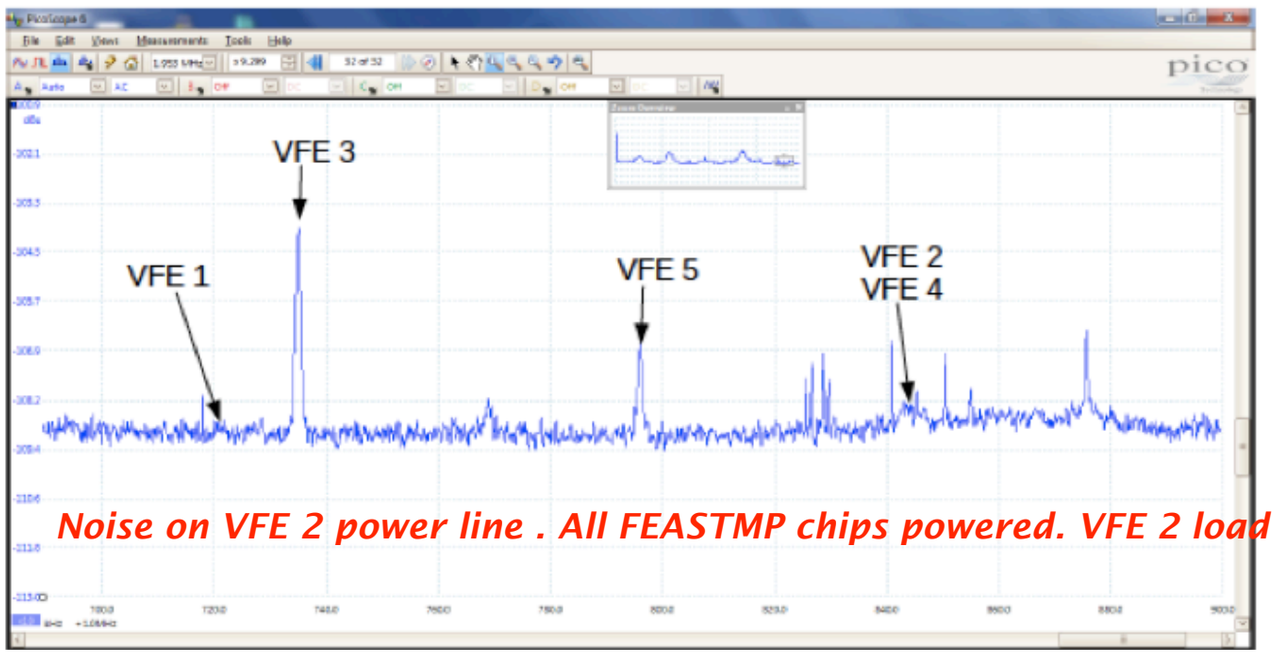
VFE 1 2.5V line power on load in (i.e. VFE card plugged into VFE 1 slot)



Noise on VFE 1 power line . All FEASTMP chips powered. VFE 1 load

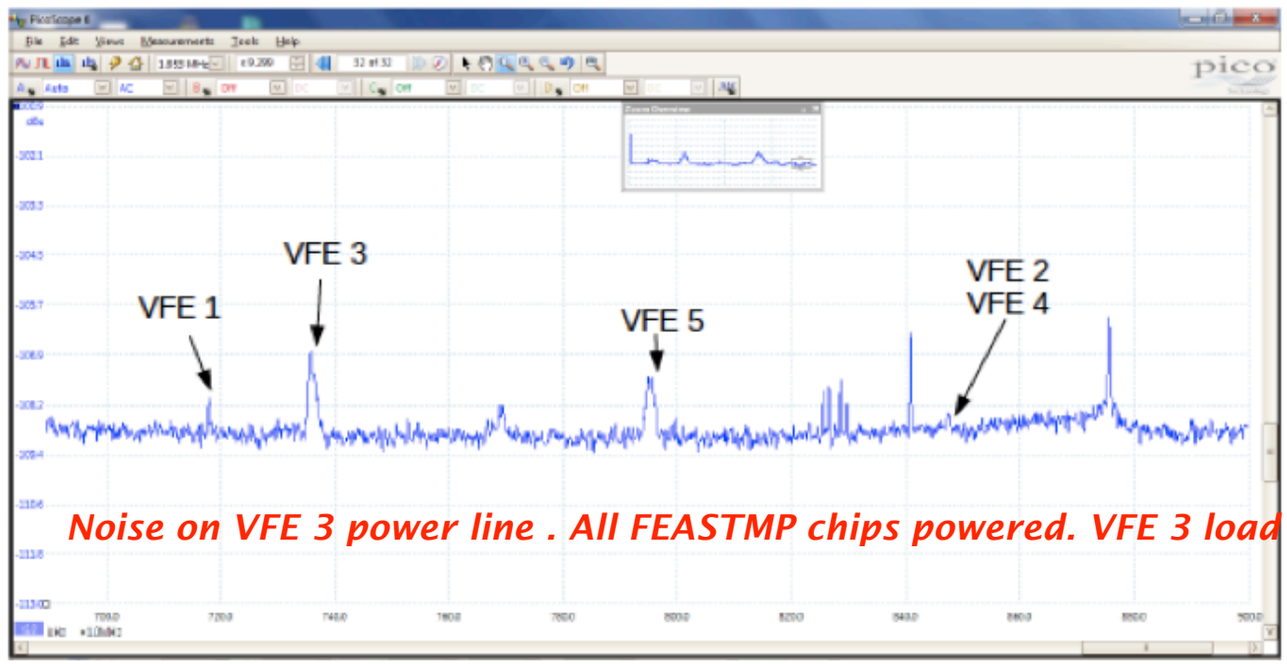
UVa PRELIMINARY TESTS: RESULTS

VFE 2 2.5V line power on VFE card in VFE 2 slot



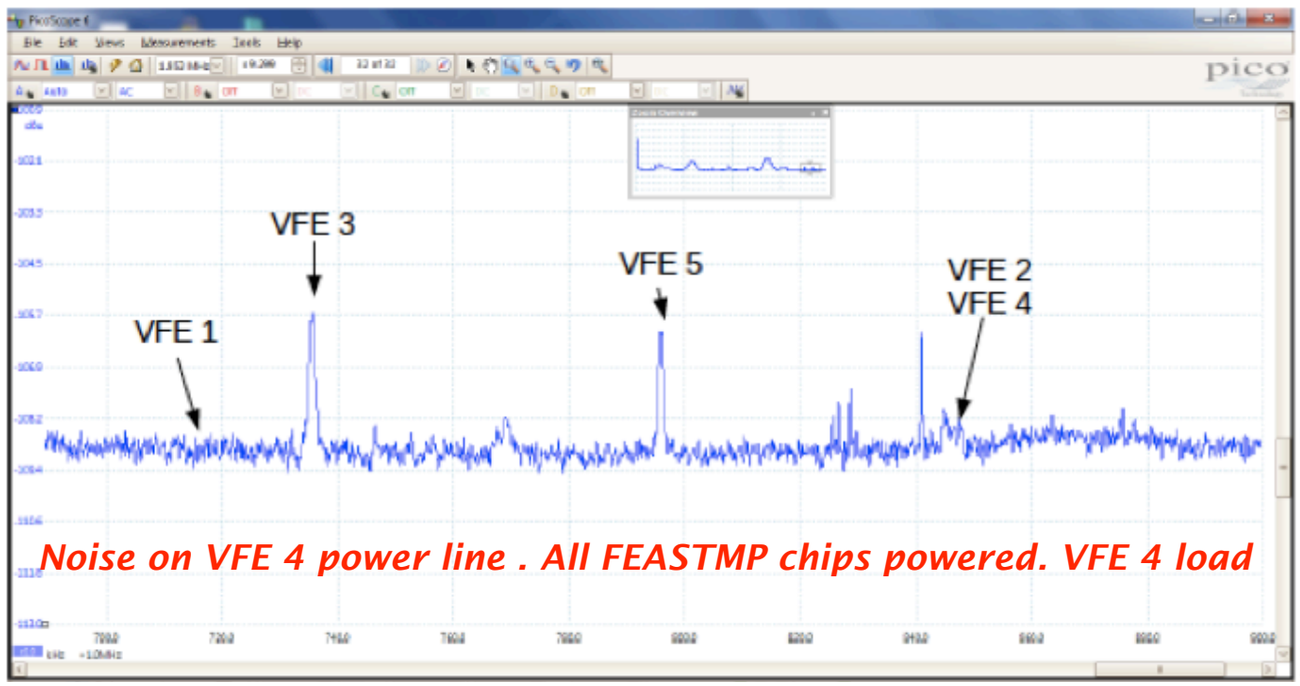
Noise on VFE 2 power line . All FEASTMP chips powered. VFE 2 load

VFE 3 2.5 V line power on VFE card in VFE 3 slot



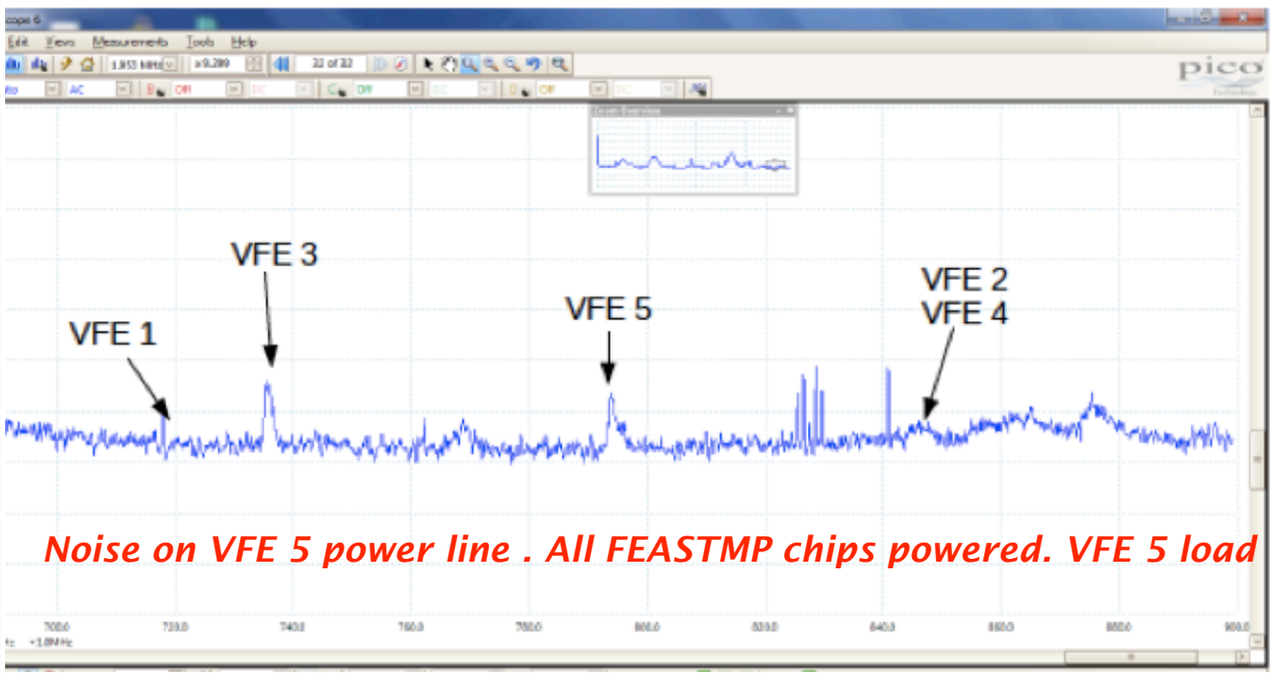
Noise on VFE 3 power line . All FEASTMP chips powered. VFE 3 load

VFE 4 2.5V line power on VFE card in VFE 4 slot



Noise on VFE 4 power line . All FEASTMP chips powered. VFE 4 load

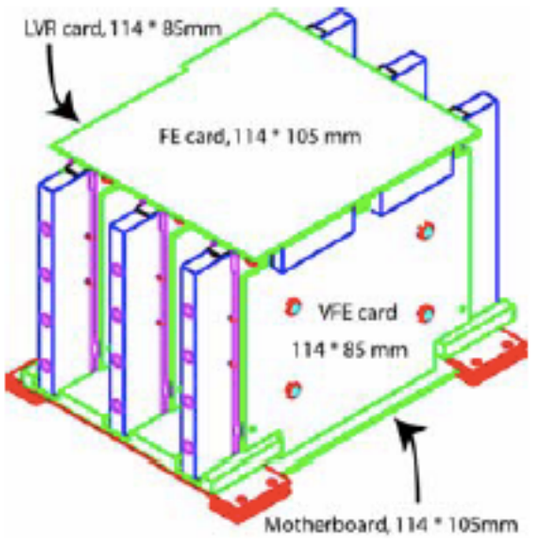
VFE 5 2.5V line power on VFE card in VFE 5 slot

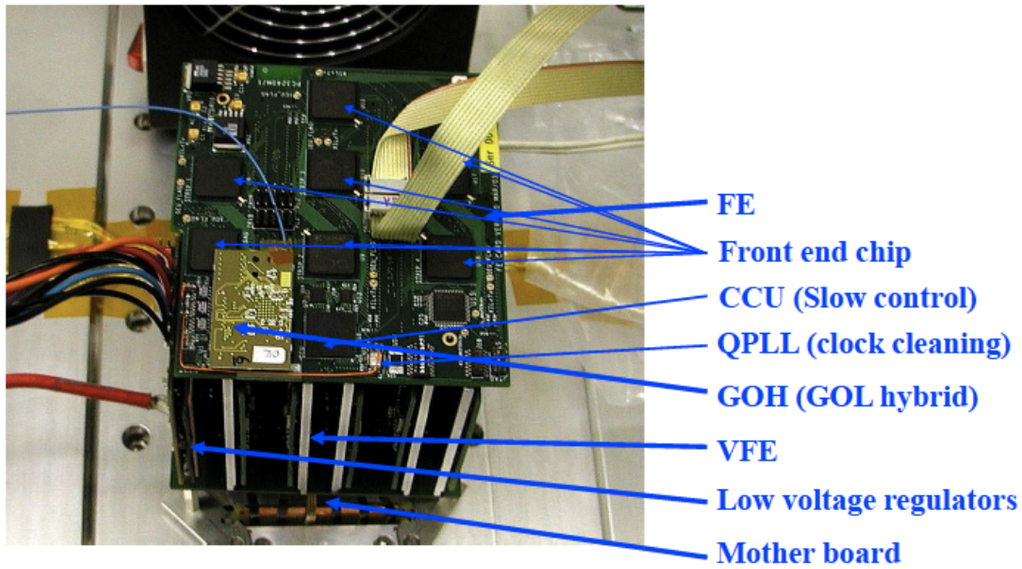


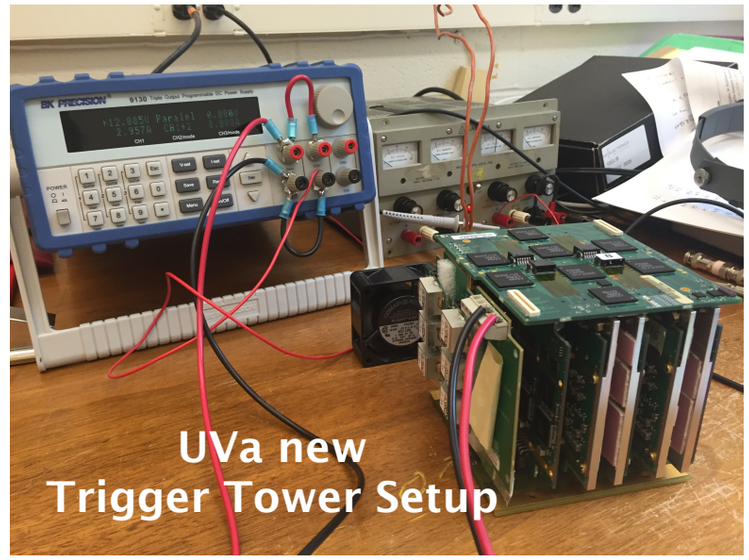
Noise on VFE 5 power line . All FEASTMP chips powered. VFE 5 load

WHAT IS ONGOING

- *Built one complete Trigger Tower Test setup, (the basic element of the front end system)*



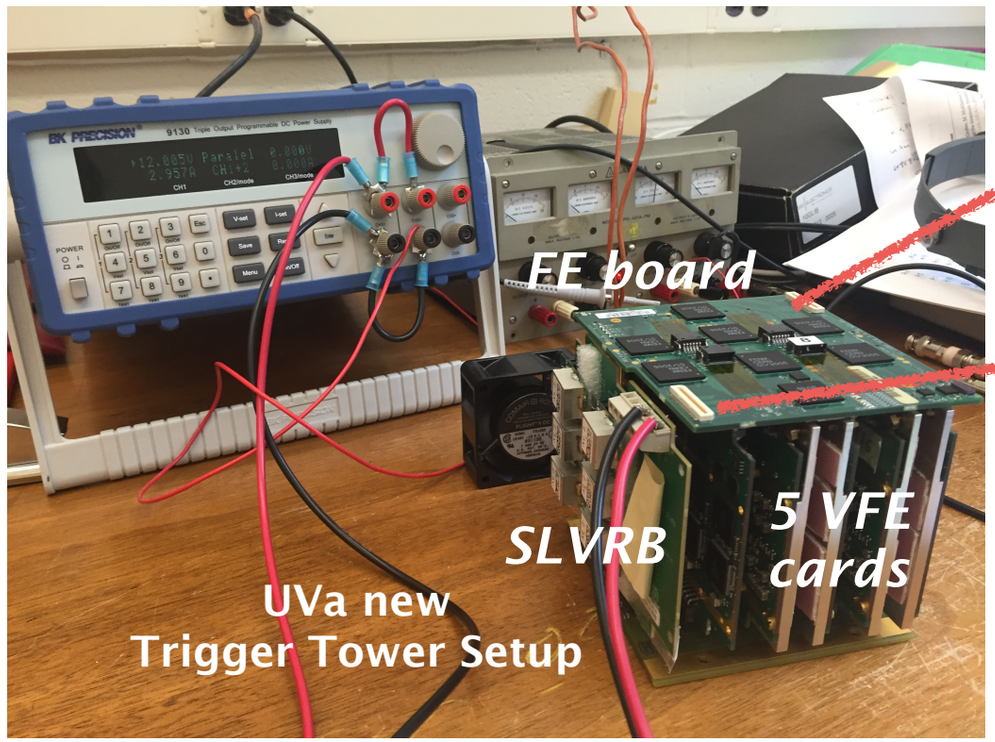


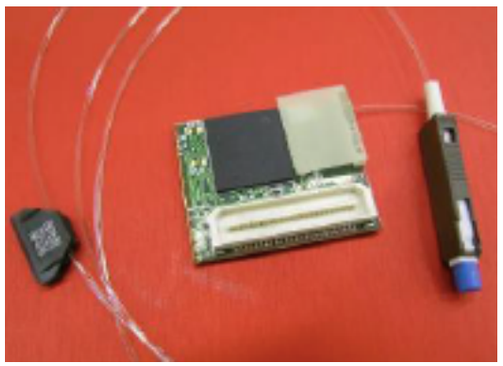


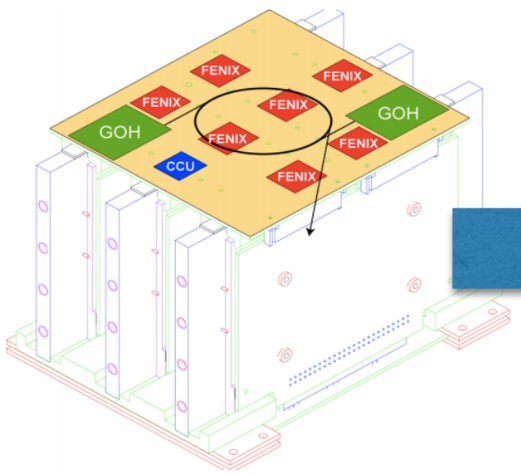
- *We got Trigger Tower powered up*
  - *At 12 Volts input it draws about 3 amps from the power supply*
- *The current card with the FEASTMP modules turns the FEASTMP's on as soon as they are powered*

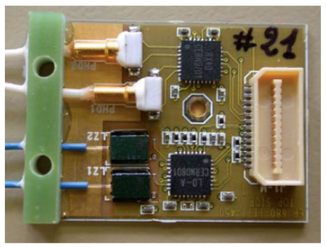
WHAT IS ONGOING

- *Started to think about how to readout it using the GLIB card*



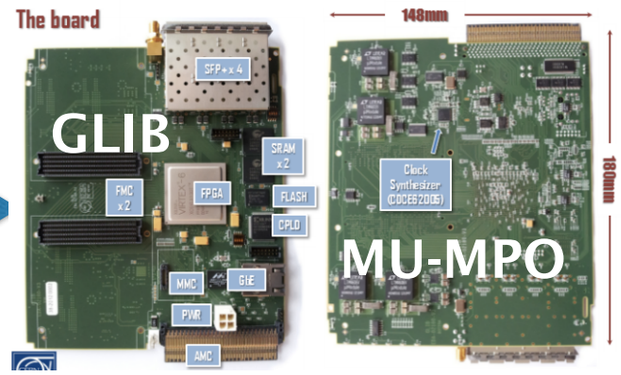




READOUT ? 

DOH
Digital Opto-Hybrid

Optical Fiber



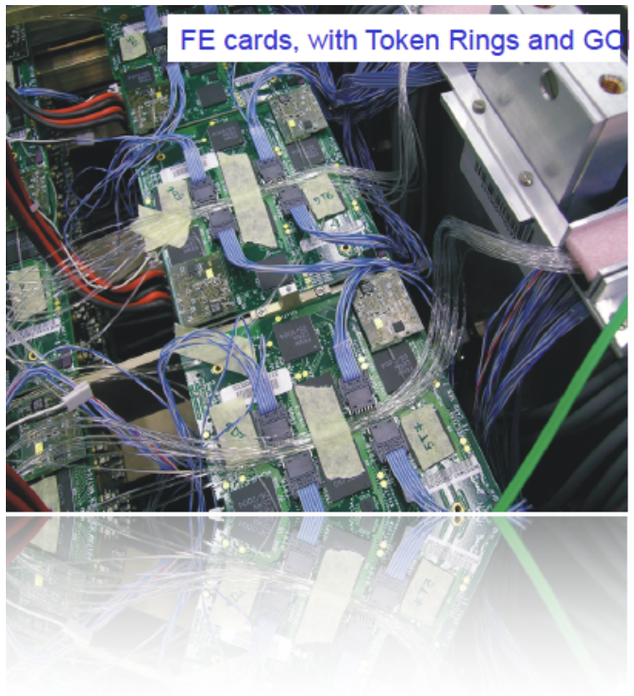
MU-MPO= fiber optic adapters

data are transmitted off of the current FE card with GOH mezzanine modules which are the fiber interfaces

WHAT WE STILL NEED TO READOUT

- *Still some missing pieces that we need to readout the TT using a GLIB card (the optical fiber cable and the mezzanine card to communicate with the GLIB)*

  - *1 aluminum cooling plate for the VFE card that doesn't have one*
    - *better we get another VFE card with the housing already attached otherwise we will also need the gap-filling material*
  - *one or two GOH cards, the optical transmitter that plugs into the FE card*
    - *no problems with GOH and MU-MPO adapters*
    - *No single DOH available*
  - *the rest of the cooling blocks for the 5 by 5 TT setup that maybe we can get from CERN (we need to check if it fits in the UVa's magnet)*
    - *it seems there are 4 pieces of Endocarps cooling blocks but maybe there are not leak tight (maybe we can use Peltier cooler)*
  - *long optical fiber (about 5 meters) or at least the specifics so we can make one by ourselves*



We also need to know what are using at CERN in the test setup for the trigger and slow control and readout through the token ring

CONCLUSIONS

- *Started to arrange a more complete and realistic system as the Trigger Tower Test setup*
- *We still need some suggestions in order to readout using the GLIB card*
- *We aim to be able to conduct tests at the 0.1% level of the effects of noise as a function of temperature variation, 3.8 magnetic fields, and a set of radiation tests at the level expect for 3000 fb^{-1} behind the lead tungstate ($PbWO_4$) crystals*
- *First tests with "minimal setup" shown:*
  - *all 6 DC-DC converter chips have slightly different frequencies, close to but significantly different from 1.8 MHz*
  - *one of the chips generated larger noise on the power lines than the other five*
  - *investigating the noise peak difference with the load imposed by the VFE card we realized that the is effect seems to decrease significantly the observed noise on two of the power lines but leave the noise unchanged on the remaining four*
  - *we also tried to test the possibility of cross-talk by measuring the noise on lines other than the ones that are powered by each individual FEAST chip*


danke
謝謝
ngiyabonga
teşekkür ederim
спасибо
dank je
gracias
thank you
mauruuru
hvala
dziękuje
mochchakkeram
go raibh maith agat
obrigado
sukriya
kop khun krap
arigato
dakujem
terima kasih
grazie
merci
감사합니다

BACKUP