ADC for ECAL Upgrade

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Physics Motivations

- Opportunity opened by ECAL frontend upgrade
- Higher luminosity and radiation levels
  - SEU immunity
- Technology upgrade to CMOS 130 or 65 nm
  - integration of ADC with digital data processing (multi-gain)
- Possibility of precise time measurement
  - using high sampling frequency
- Improved spike and pileup rejection
  - using detailed pulse shape analysis

ADC: tentative specifications

- Resolution 12 bit
- Speed >120 MSPS
- Current < 50 mA
- Supply (V) ≈ 1V
- Architecture: SAR or Pipeline
- Technology TSMC CMOS 130 or 65 nm
- Area < 0.4 mm^2
- Radiation resistance (tbc):
  - gamma dose (TID) ~ 1Mrad
  - neutron flux ~ 2.4×10^{14} n/cm^2
    - integrated dose and neutron flux in ECAL for the HL-LHC integrated luminosity

Institutional Motivations

- LIP contribution to CMS Upgrade should have a significant fraction in-kind provided by Portuguese industry
- The present ECAL ADC (12 bit, 40 MHz) was developed by Chipidea in Lisbon.
- Two poles of high-level expertise in ADC IP in Lisbon with close links to LIP
  - Synopsys (previously Chipidea) Joao Vital, Manuel Mota
  - S3 (previously Acacia Semiconductor S.A.) Joao Goes
- Other options

Synopsys option

- ADC IP for TSMC 65 nm and 28 nm:

Process node	TSMC65LP	TSMC28HPC
Architecture	Pipeline	SAR
Resolution (bit)	12	12
Speed (MSPS)	250	160
Drawn Area (mm2)	0.34	0.08
Current @ 160MSPS (mA)	36	6.5
Supply (V)	1.2	0.9

- It turned out that the implementation of SEU immunity doesn't fit in Synopsys business model
- Synopsys declined the invitation

S3 option

- S3 has ADC IPs with the required specifications
  - (e.g S3AD250M12BIT65LPX, S3ADS320M12BSM40LL)
- S3 has experience in '*radiation-hardened* ADCs'
  - 13-bit 80 MS/s 'self-calibrated Pipeline' ADC in TSMC 90nm for ESA , including IC and radiation tests
  - Expert: Joao Goes
- S3 can adapt these IPs or others to include TMR and possibly other techniques:
  - 12b 160MS/s SAR-based ADC
  - GDS2 and Timing/VERILOG views
  - Radiation resistance customization
  - Development time scale ~ 6-12 months

Radiation resistance customization

	Specification	Effect in the circuit	Hardening by Design Techniques Employed
TID	1000krad Max.	V_T change	• Effect diminished has process geometries are reduced. Should not be very critical in beyond 130nm technology (e.g. 65nm or 90nm standard CMOS). • Use high-Vt NMOS and standard-Vt PMOS devices. • Design transistors with a lower V_{Dsat} voltage to improve robustness to Vt variations. • Calibrate the ADC offset.
TID	1000krad Max.	Parasitic leakage current	• Use P+ guard rings to separate different circuit in the layout. • Use enclosed layout transistors.
SEL	70MeV.mg^{-1}.cm^2	Circuit latch-up	• Use large P+ guard rings to separate NMOS and PMOS transistors. • Use large N+ guard rings inside NWELLS. • Use TMR (triple module redundancy) to deal with SEU.

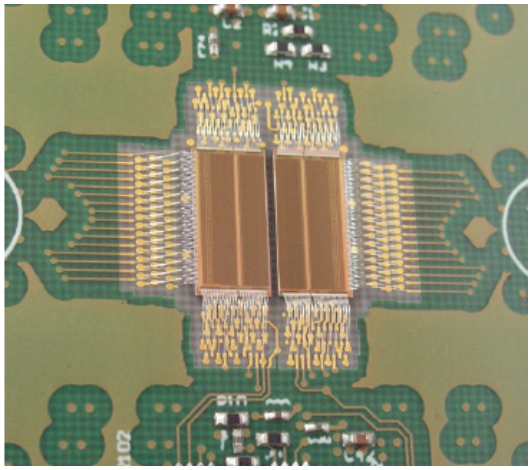
Universidade Nova option

- Direct collaboration of LIP with Joao Goes, Universidade Nova
  - Joao Goes is professor at Univ Nova (microelectronics) and is S3 Advisor
- Possible collaboration with INFN/Torino in chip integration
- Manpower:
  - Univ Nova: team of 4 engineers, licenses Cadence/Calibre, fabrication in TSMC 65 nm
  - LIP: team of 2 engineers in digital design
- Deliverable: ECAL digital chip with ADCs integrated
  - multi-gain selection, data compression
- Development time ~ 18 months, including MPW
- More flexible option towards final chip validated under radiation

TOFPET ASIC

SiPM readout from analog frontend to digital system interface

- 2 x 64 channels in 7 x 7 mm^2
  - CMOS 130nm
- SNR (Qin = 200 fC, C_{in}=350pF): 25 dB
- TDC time binning 50 ps (option 25 ps)
- Optimized for low power
  - 10 mW per channel
- Digital I/O LVDS

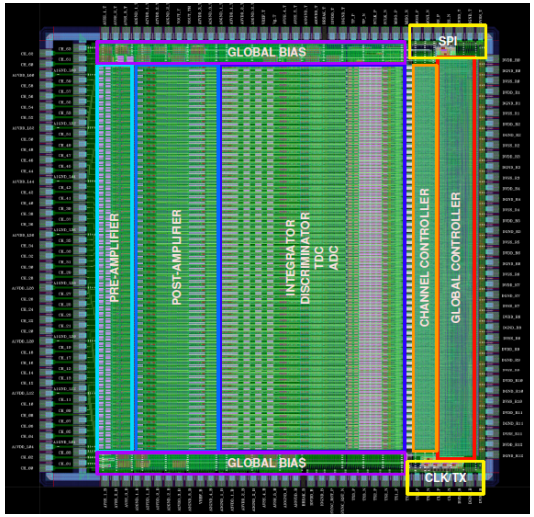


Two 64-channel chips

- New version TOFPET2

- ADC measurement in the range 100fC-1500 pC
- Event rate up to 600 kHz per channel
- Silicon produced. Testing on-going

Developed in collaboration LIP, PETsys, INFN/Torino



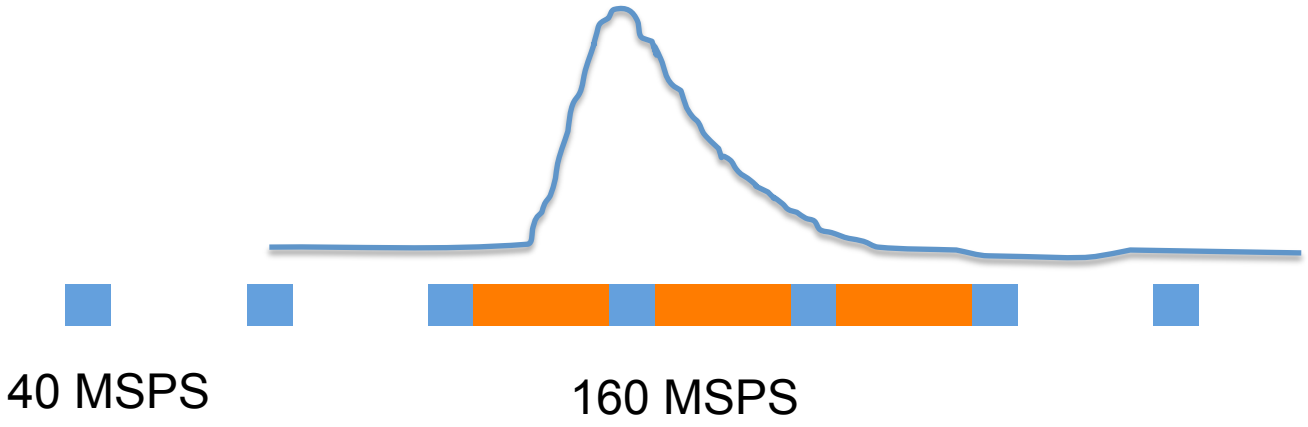
CMOS 110 nm
Die size 5x5 mm^2

Simulation studies

- New Posdoc to participate at 50% in simulation work
- Establish collaboration with the ECAL groups involved
- Study data compression algorithms vs sampling rate
- Example in next slide
- Validate architecture and finalize ADC specifications

Data compression

- 80 MSPS → 3 (4) x 10 Gb/s links per tower (25 crystals)
- Zero suppression algorithm with constant latency:
  - transmit samples at 40 MHz in the baseline
  - transmit samples at 160 MHz in the pulse region
  - one bit identifier per sample
- Assuming pulse contained in 3 BCs, probability of sample above noise is ~ 30% (for 200 pile-up events)
- Equivalent bandwidth required is 76 MSPS



Very tentative ECAL ADC chip

- 1 to 25 channels per chip (tbd)
- Three ADC blocks per channel (multi gain)
- 25 * 3 analog signals = 75 ADCs
  - total silicon area 30 mm^2
  - power 3.5 W
- Digital processing
  - Selection of highest non-saturated sample
  - Data compression
- GBT interfaces
  - eLinks

Tentative schedule

- Simulations and final specs – Dec 2016
- ADC design for radiation & digital design – Sep 2017
- 1st MPW (partial chip) submission – Dec 2017
- 1st MPW tested – Sep 2018
- 2nd MPW (full chip) submission – Dec 2018
- 2nd MPW tested – Sep 2019
- Engineering run submission – Dec 2019
- Wafers available – Jul 2020
- Chips available for VFE production – Dec 2020

BACKUP