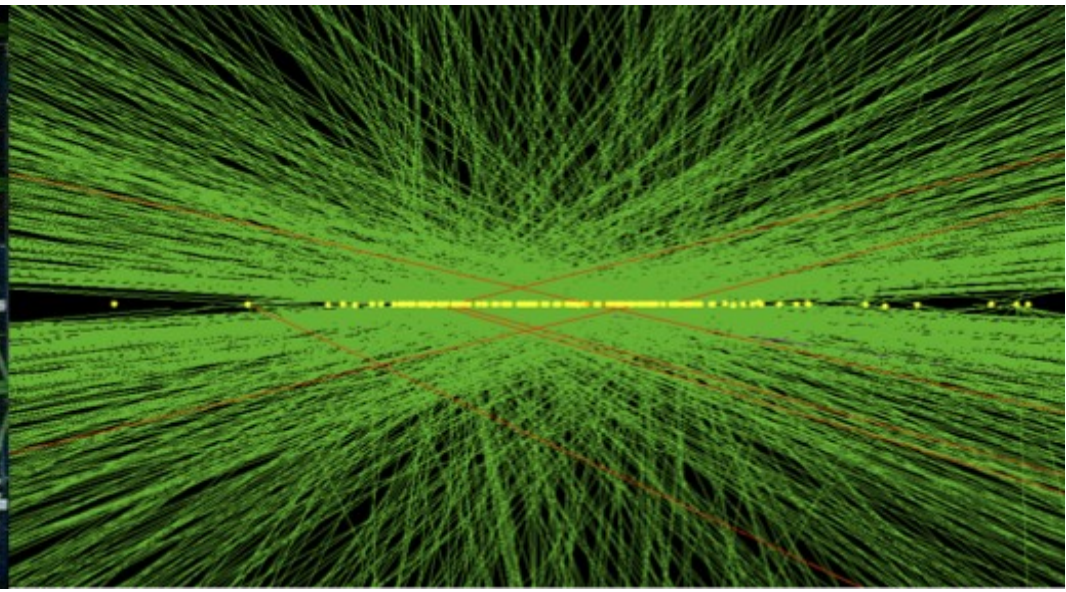
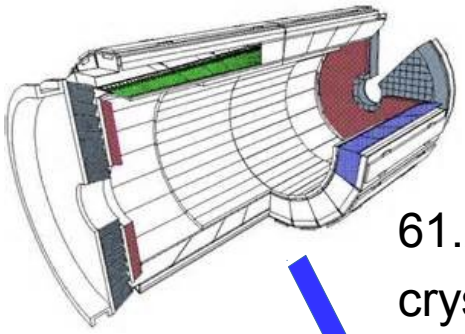
Off detector electronics considerations

Bob Hirosky
VFE Workshop, May 13, 2016



Overview of ECAL Barrel readout



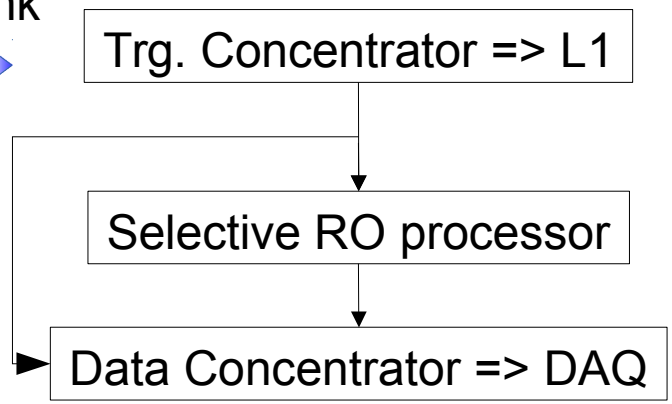
61.2k $PbWO_4$ crystals

5x5 Readout Unit (RU)

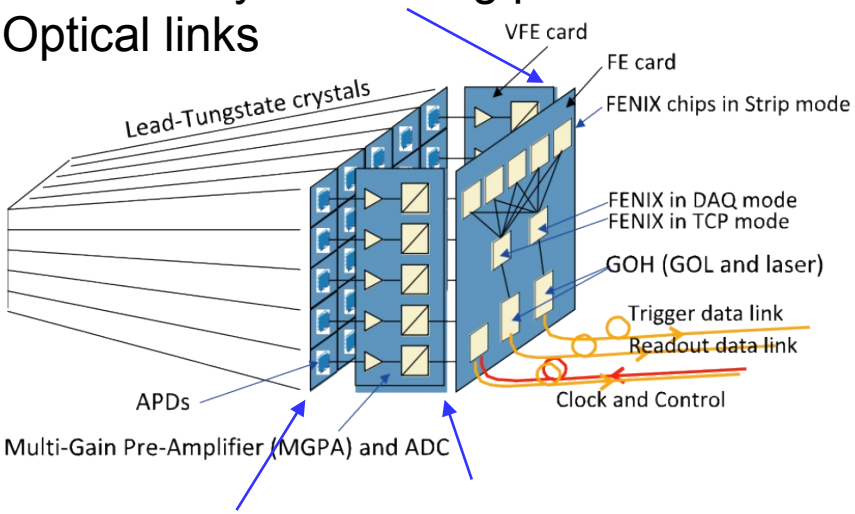
Simplified off detector data flow

FE Trigger Link

FE Readout Link



FE: Latency buffers/Trg primitives
Optical links



APDs/motherboard **VFE**

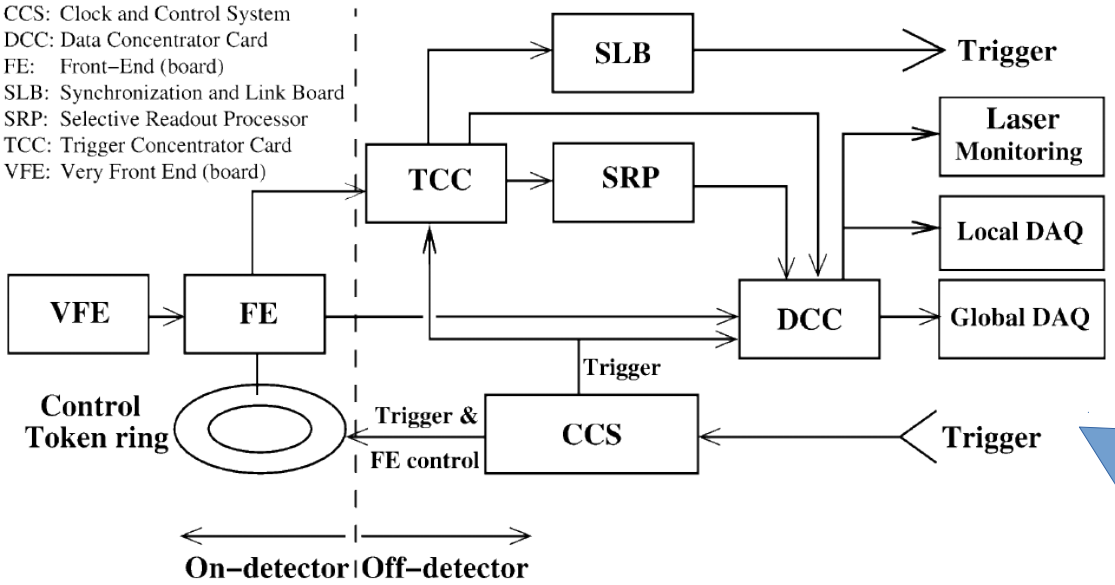
Amplify/digitize
=>16 Gb/s

Present detector

Data buffering on frontend,

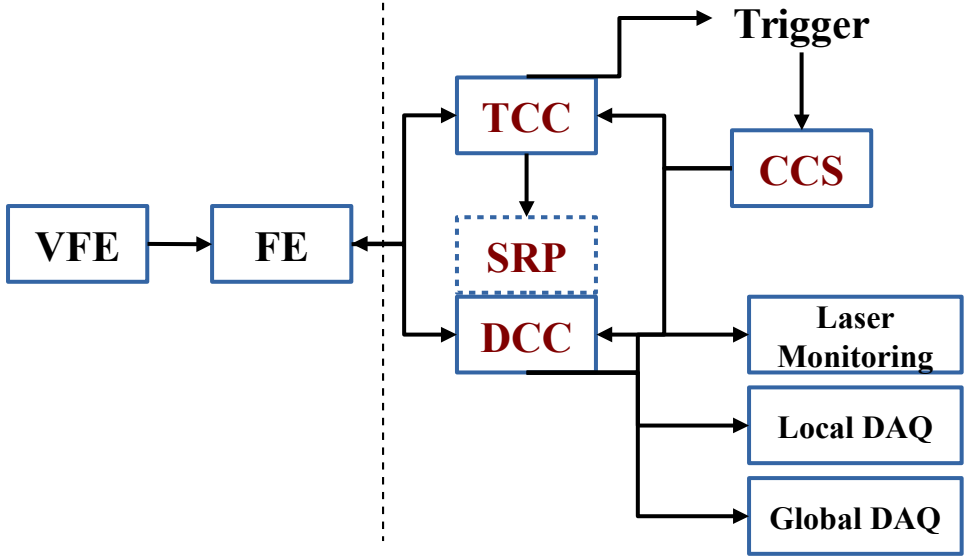
- Selective readout used to stay within bandwidth constraints
- Separate trigger and data paths
- Coarse 5x5 crystal readout at 40 MHz for trigger

Off-detector electronics



TCC: trigger concentrator
DCC: data concentrator
SRP: selective RO processor
CCS: clock & contol card

- Upgrade to handle higher data transfer rates
- Move data buffering and all trigger processing off detector
- Reduce physical complexity of connections, flavors of cards



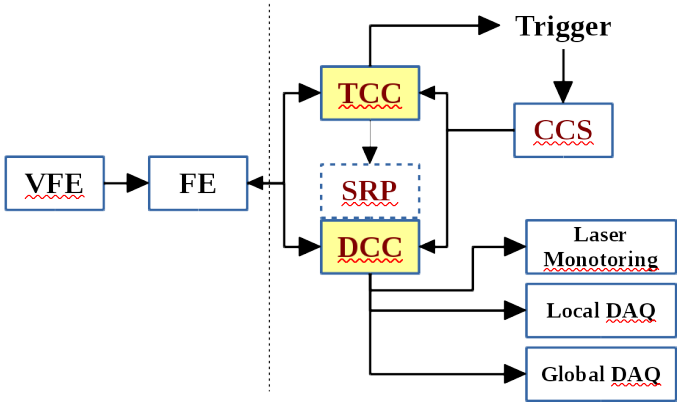
TCC Upgrade

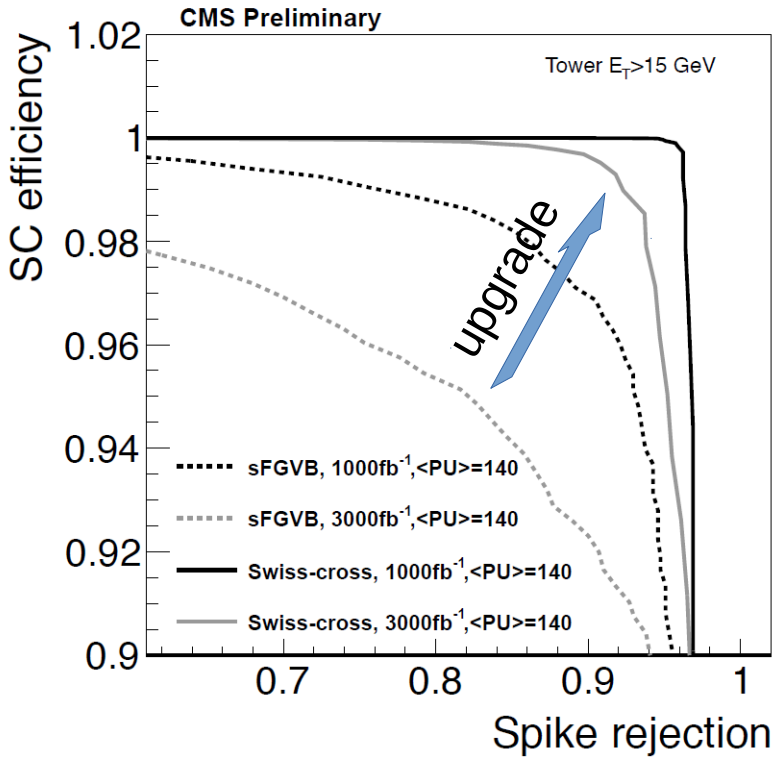
Trigger Concentrator Card (TCC)

- Receive event data from FE
- Alignment, pulse reconstruction
- Calculation of trigger primitives
- Implement offline spike suppression algorithm before L1 (maintain acceptable trigger rates)
- Transmit data to L1 trigger, DCC

Located off detector, no requirements for radiation tolerance

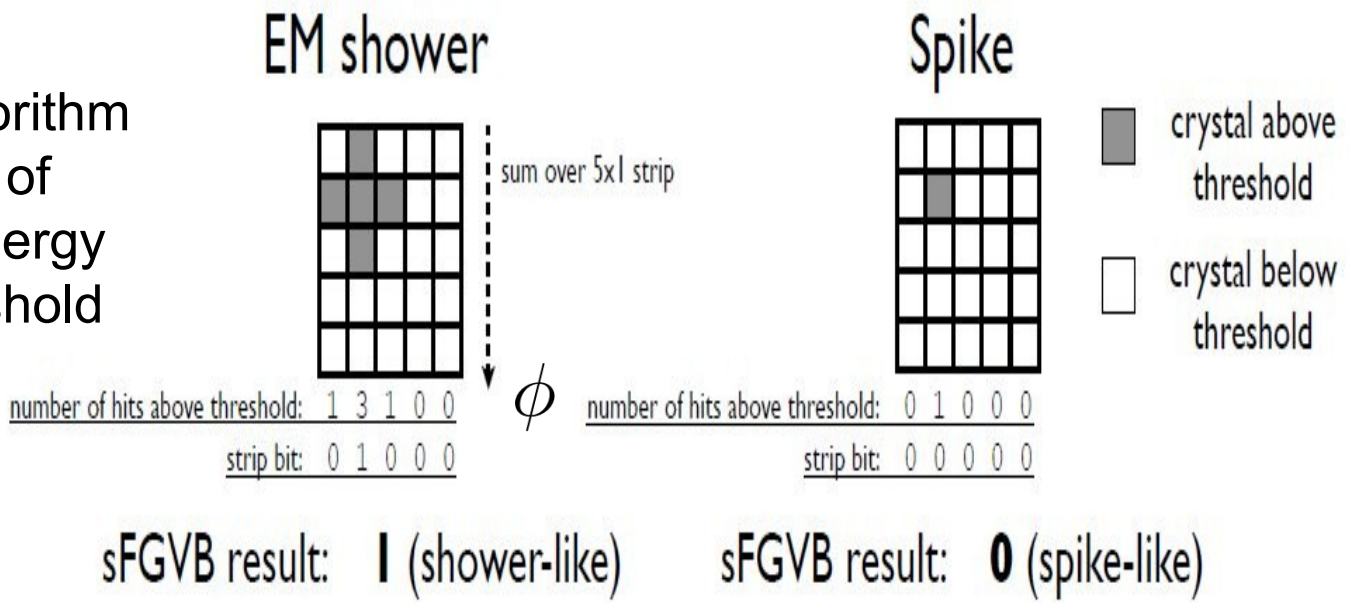
- Implement using commercial FPGA
- Maximize overlap with other technological choices at CMS, with ECAL customization (eg see CTP7)

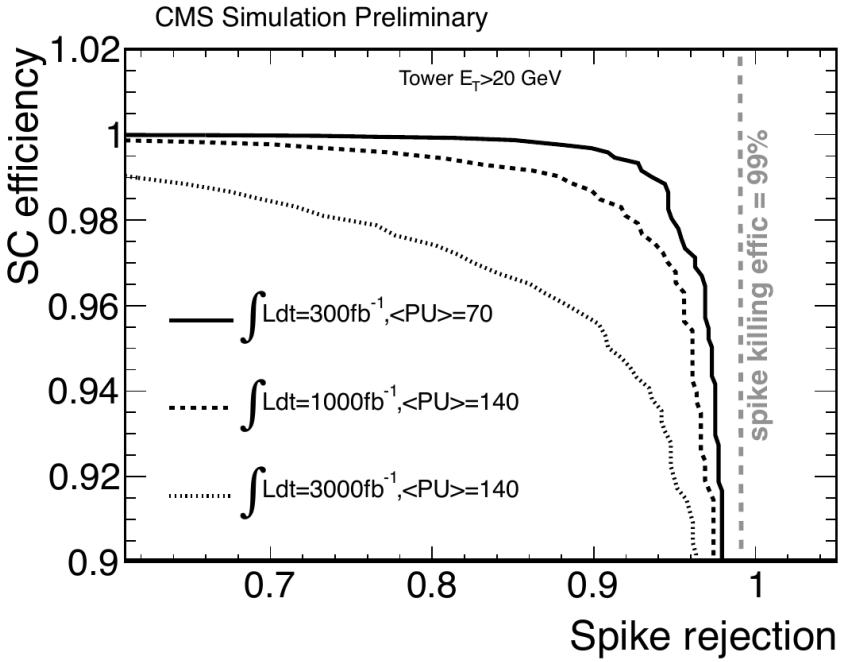




Spike rejection

Present online rejection algorithm relies on coarse summation of crystals in 1x5 strips with energy deposits above a fixed threshold



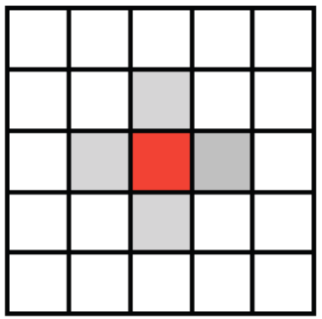


Existing energy L1 algorithm breaks at trigger HL-LHC luminosities:

- Affected by APD noise increase
- Not robust at high pileup levels
- Rate depends on beam intensity
  E_T > 20 GeV: ~1 spike/6k events at 7 TeV

Spike rejection

Offline rejection of spikes rejection algorithm using topological characteristics for L1 trigger

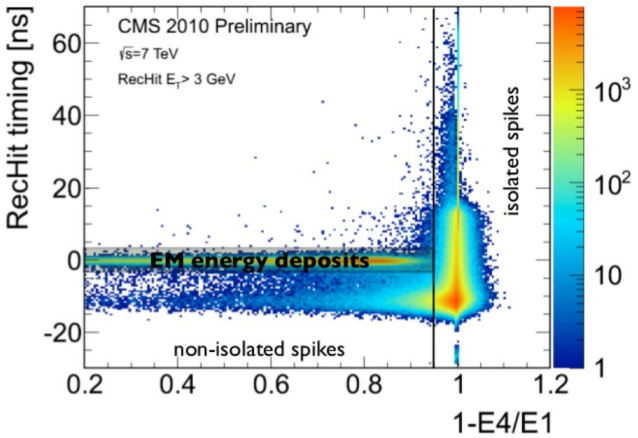


E1

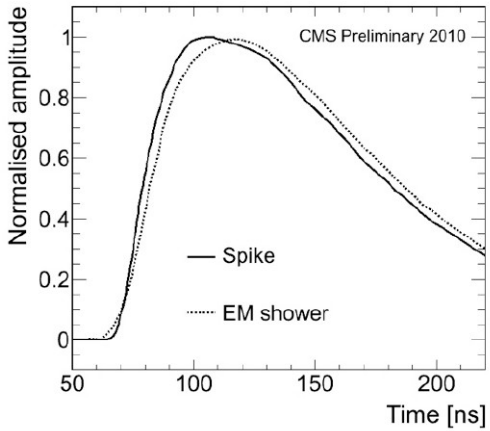
E4

Cut on the "Swiss-cross" variable (1-E4/E1) rejects ~96% of spikes with E_T > 20 GeV, negligible impact on EM efficiency. But retains some pileup and noise sensitivity.

Additionally timing/shape distributions can identify pulses inconsistent with scintillation light.



Run 1 electronics already offer discriminating power based on pulse shape discrimination. Further enhanced with faster VFE shaping.

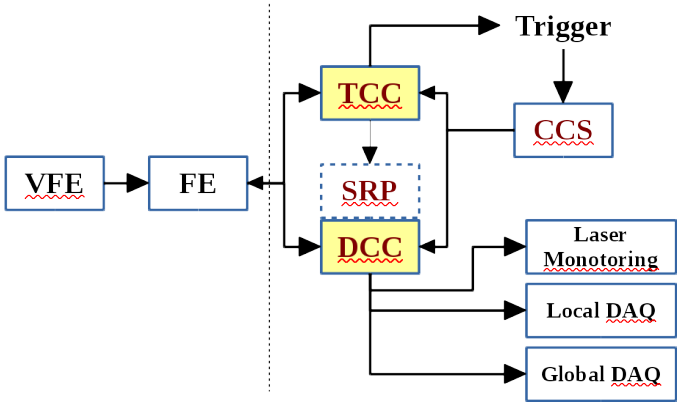


Combining these two methods, topological and timing cuts, a spike rejection factor >>100x can be obtained.

DCC Upgrade

Data Concentrator Card (DCC)

- Receive event data from FE, TCC
- Integrity checks, alignment
- L1 trigger latency buffer, feedback to trigger (throttle)
- Zero suppression, possible SRP functions
- Transmit data to DAQ



In new readout structure a single data stream from the detector feeds trigger and data paths.

=> it's possible to think of these either as functional logic blocks on the same HW or tightly coupled, similar cards

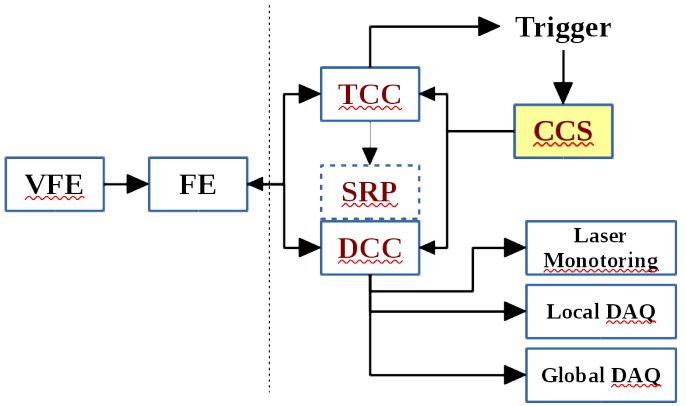
Preferable design may consist of a single DCC/TCC per ½ supermodule

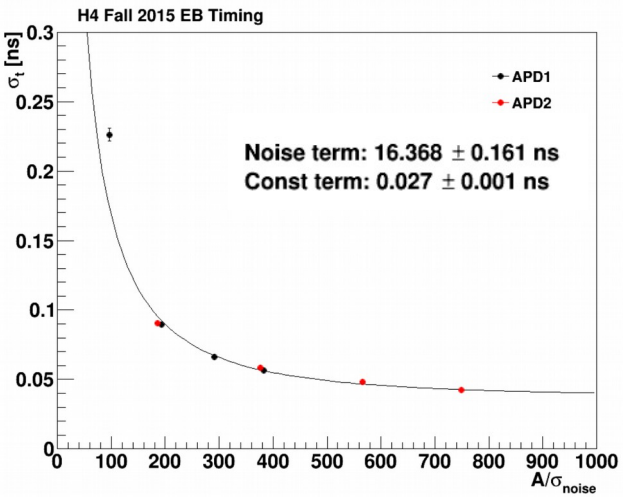
- 72 cards to handle 68 readout units per SM
- Modern FPGAs already close to providing full I/O capability in a single device

CCS Upgrade

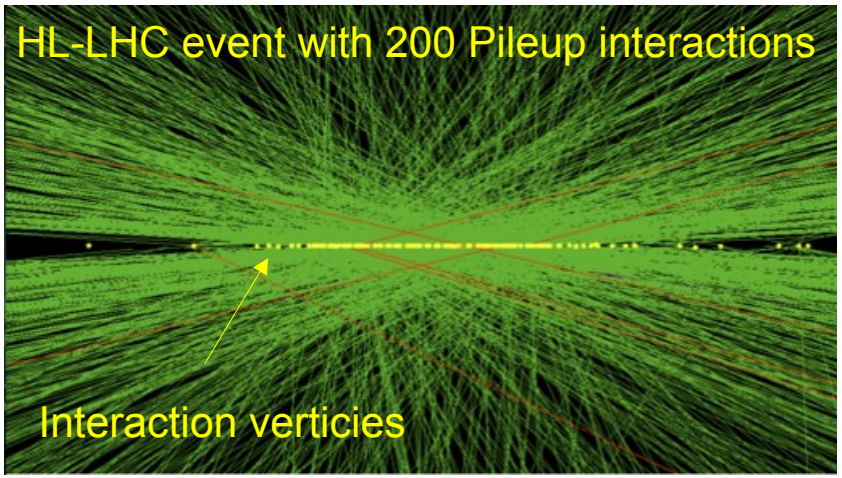
Clock and Control System (CCS)

- slow controls of the front-end electronics: electronics configuration and status report
- distribution of fast timing signals: e.g. clock, trigger.
- routing of the trigger throttle signals





Precision timing capabilities achievable, due to intrinsic performance of ECAL. Improves association of neutral energy deposits with vertex
=> p_T resolution



Photon vertex resolution contributes significantly to Higgs mass resolution

Timing data (Fall 2015) testbeam

- Observe ~30ps constant term (ct <1cm)
- Achieved timing performance insitu ~ 150ps: timing drifts on front end

Include high precision clock distribution CCS/FE upgrade

Counting links

“Baseline – Three up”

- **Three 10 Gbit up-links would allow 24 (26) bits per channel**
  - **Three 320 Mbit Elinks**
  - **11 (12) bits ADC plus gain flag @ 80MHz. Enough?**
  - **Requires e.g. one 3+1 versatile link+ module per FE (foreseen)**

“Four up”

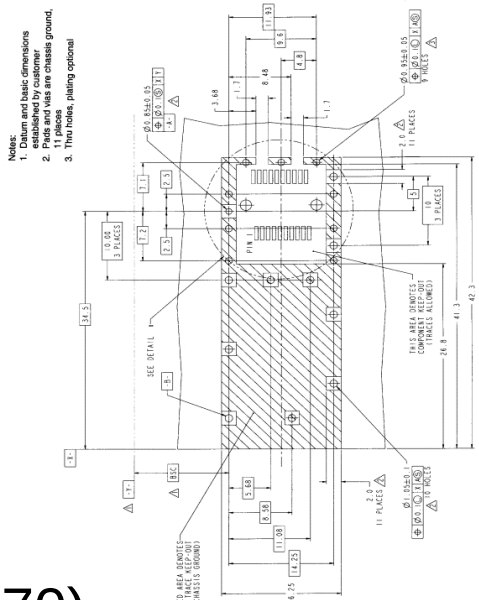
- **Four 10 Gbit up-links would allow 32 (34) bits per channel**
  - **Four 320 Mbit or two 640 Mbit or one 1280 Mbit Elinks**
  - **15 (16) bits ADC plus gain flag @ 80MHz. Better?**
  - **Requires e.g. one 4+1 versatile link+ module per FE (foreseen)**

“Six up”

- **Six 10 Gbit up-links would allow 48 (52) bits per channel**
  - **Six 320 Mbit or three 640 Mbit Elinks**
  - **11 (12) bits ADC plus gain flag @ 160MHz.**
  - **15 (16) bits ADC plus gain flag @ 120MHz.**
  - **Requires e.g. two 3+1 versatile link+ module per FE**
    - **Only one FE control link would be used; the other receiver used for precision sampling clock?**

Counting links

68-readout units/SM
Baseline planning for off detector electronics:
2 xCC cards/SM

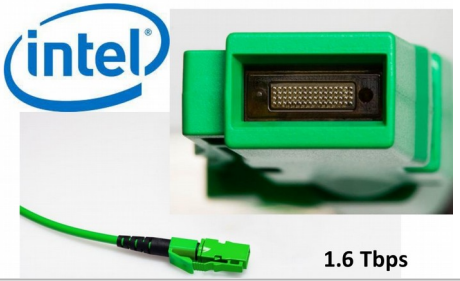


<=~17mm =>

	10Gb Links/xCC	*almost*
3-up	102	Modern FPGAs ^have enough links (~70)
4-up	136	less than 2x what's available today
6-up	204	almost 3x largest today's link counts

Assuming something like 16-fiber matrix connectors:
(eg Molex zCD, almost available)

#connectors		Min linear space	With down links #	space
3-up	7	~12cm	9	~15cm
4-up	9	~15cm	11	~19cm
6-up	13	~22cm	17	~30cm



UTCA / ATCA height ~15cm (double wide), ~32 cm

Summary

- 3-up/4-up scenarios likely compatible w/ 2 off detector boards/SM, each with single large FPGA
- 6-up scenario pushing/(breaking?) limits of front panel real estate, significant increases in FPGA high speed links needed
  - Probably requires going from two to 3–4 boards/SM
- Tradeoffs/Optimizations
  - Online vs offline complexity / flexibility / cost
  - Efficient rejection of spurious signals
  - Precision timing and controls distribution