Science & Technology Facilities Council

Re-engineered MPGA option for VFE

Stephen Thomas
ASIC Design Group
STFC - Rutherford Appleton Lab
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Aims of the MGPA study:

- To understand the potential of the MGPA design to be developed to include spike discrimination;
- Retain circuitry (or implement low-risk changes) where the functionality does not need to change;
- Check compatibility with modern processing options (250nm/130nm design rules);
- Minimise changes required elsewhere in the system (digital interfaces, ADC speed and resolution, power?).

Review of design & simulation techniques:

Schematic conversion

- 250nm design rules
- 130nm design rules

Noise simulation

- AC analysis
- Transient noise

Numerical analysis

- Waveform calculator
- MATLAB

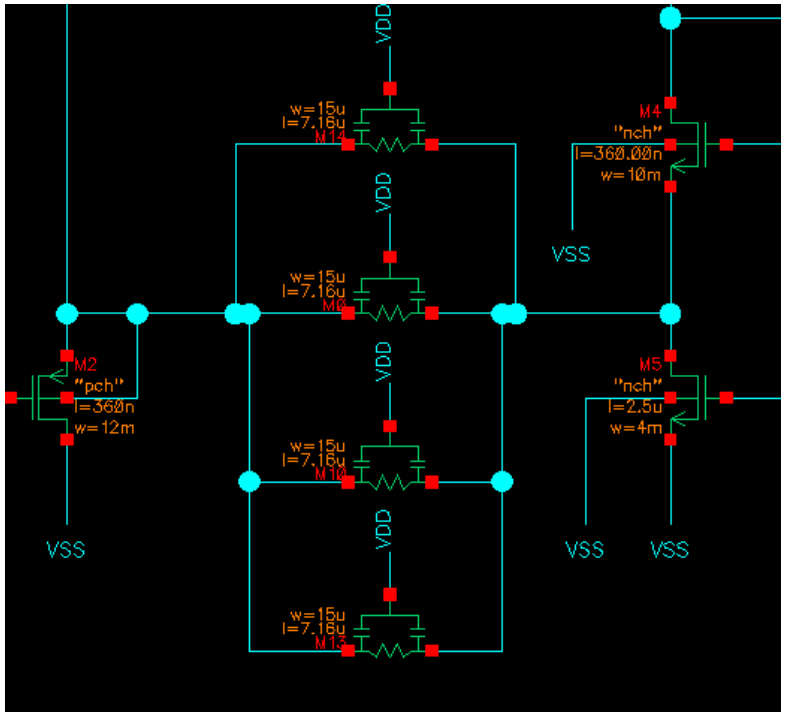
Schematic conversion

Original design: 250nm IBM
New design possibly 250/130nm IBM(GF) or equivalent

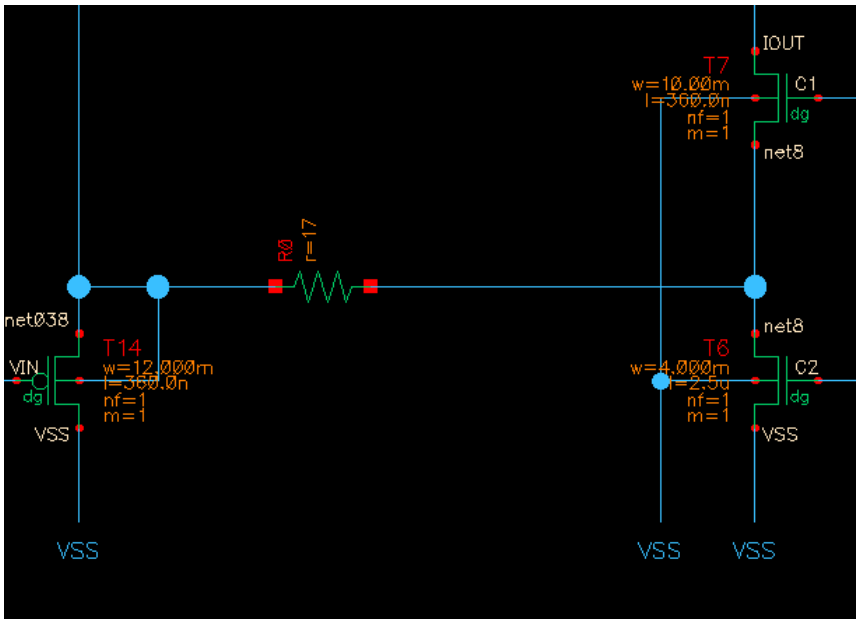
Process Design Kits are not fully compatible
Conversion process:

- Open old database from within new PDK
- Copy schematics and hierarchy
- Replace transistors with new symbols
- Manually enter transistor parameters with the original values
- Check for compatible passive components
- Adjust transistors if necessary, based on simulation results.

250nm IBM



250/130nm process, thick oxide transistors

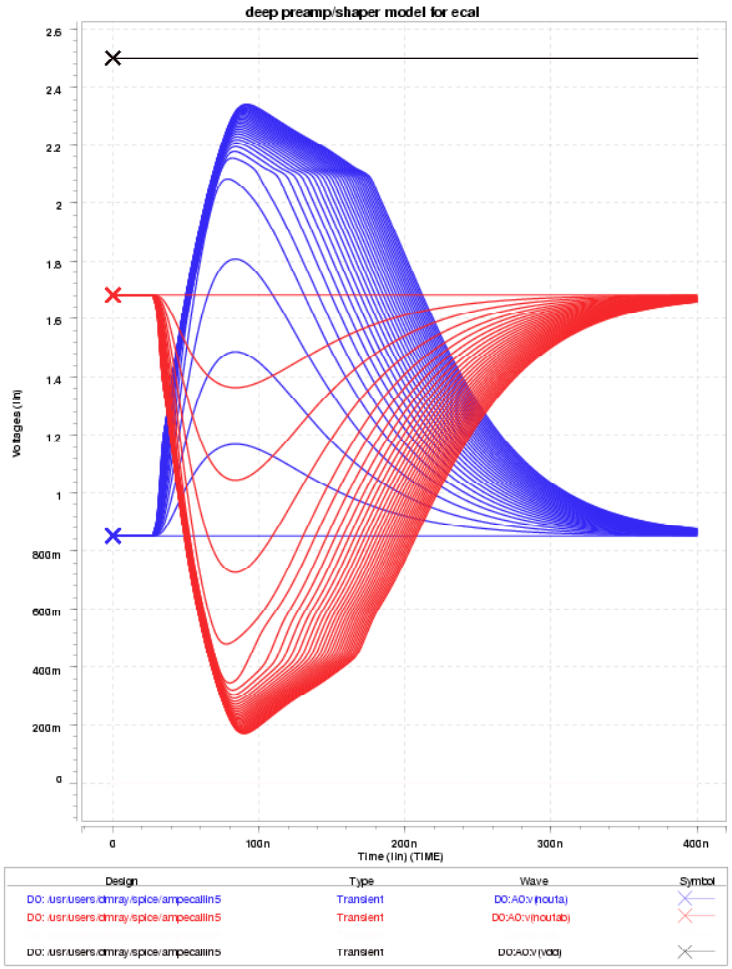


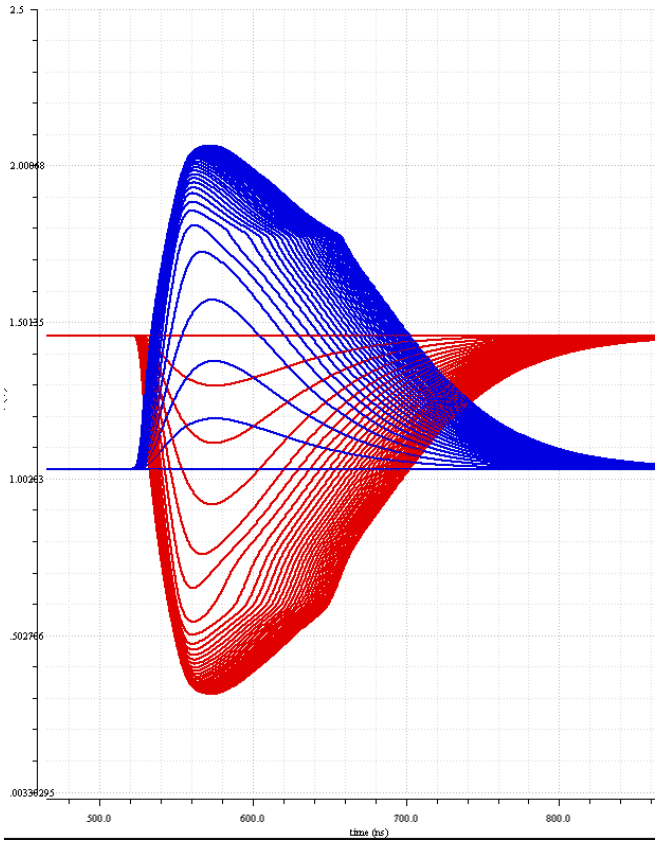
Transistor symbols are exactly the same size, but parameter names and call-backs are not compatible.

Many R/C components cannot be directly replicated. Generic R/C is an option for initial simulations

Design translation: The old IBM 250nm process parameters are similar to the 250nm/130nm process, but not identical ....

0-60pC by 2pC steps - original 250nm design ----- after conversion to 250/130nm process





Large signal response is more limited on new process (with no changes to parameters). Optimisation would help, but this is not a concern for small signal & noise analysis.

Design issues for thin-oxide conversion

Thick-oxide :

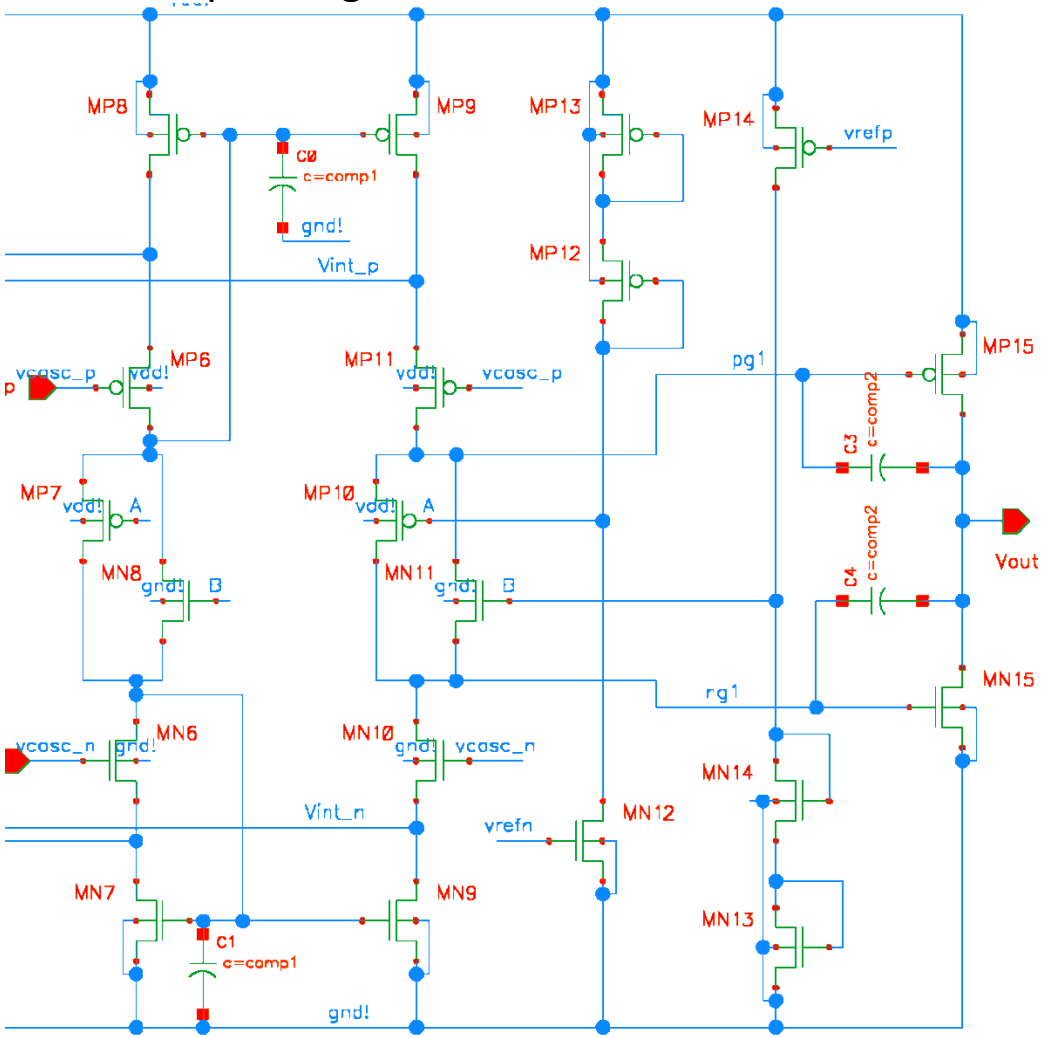
- Transistor threshold Vth0 ~0.5V,
- Typical overdrive Vgs-Vth0 ~0.2-0.5V
- Typical Vds ~0.3-1.0V
- power supply 2.5V, so no problem with series connections of four or five transistors.

Thin-oxide:

- Transistor threshold Vth0 ~0.4V,
- Typical overdrive Vgs-Vth0 ~0.1-0.4V
- Typical Vds ~0.2-0.5V
- power supply 1.2V, so this reduces voltage available per series transistor
- design is more susceptible to process variations with stacked transistors
- low-threshold transistor is an option (Vth0~0.2V)
- scaling down of transistor width/length can maintain circuit performance without change of architecture, but need to watch 1/f noise corner frequency

Example circuit, showing the challenge of low voltage design

Output stage from Class AB buffer



Power supply 1.2V

Typical threshold Vth0 ~ 0.4V

For drive strength, Vgs>>Vth0

For saturation, Vds>>Vgs-Vth0

The stack of five transistors limits Vds per transistor, which also limits Vgs drive. This can result is a reduction in analogue performance (gain, bandwidth, stability).

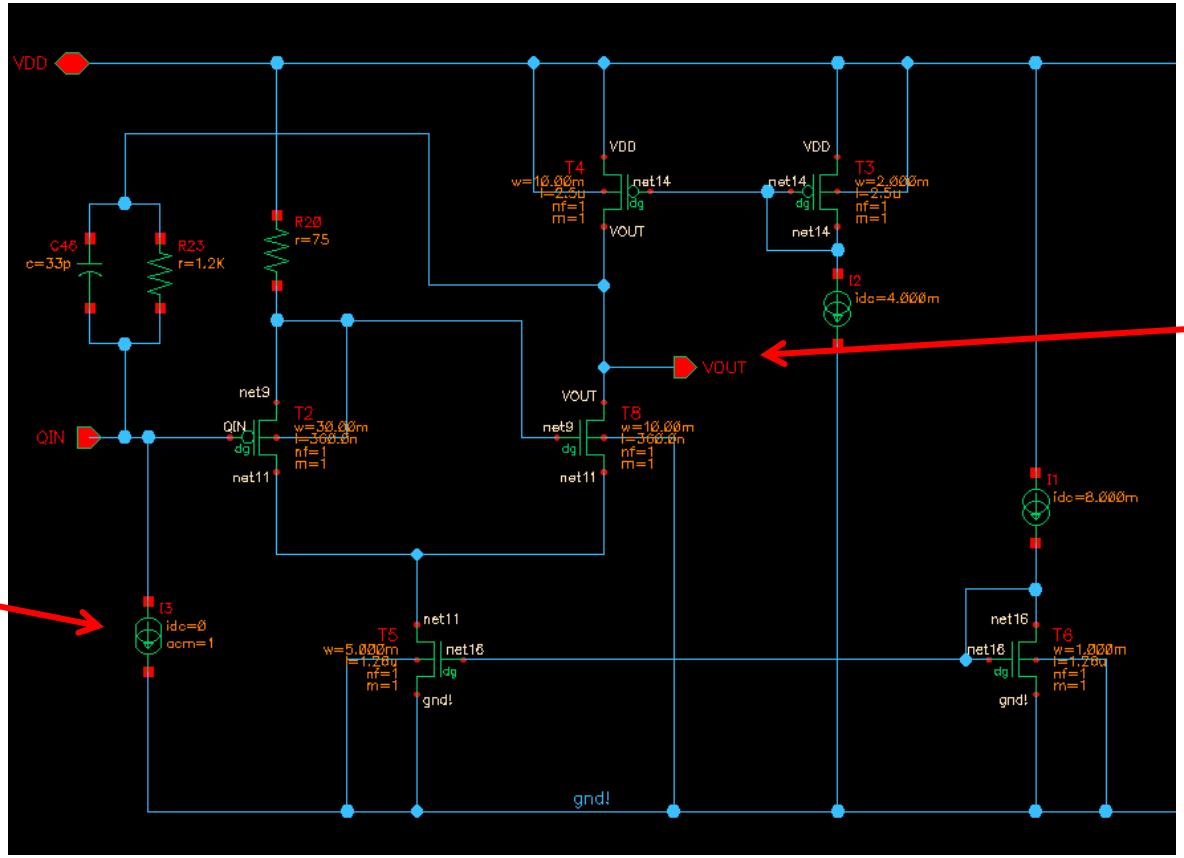
Low Vgs drive makes the circuit more sensitive to threshold variations and radiation.

The split of Vds between transistors needs to be carefully controlled.

AC noise analysis:

Noise contributions of all components calculated at the output

Simulation time is short



Output node

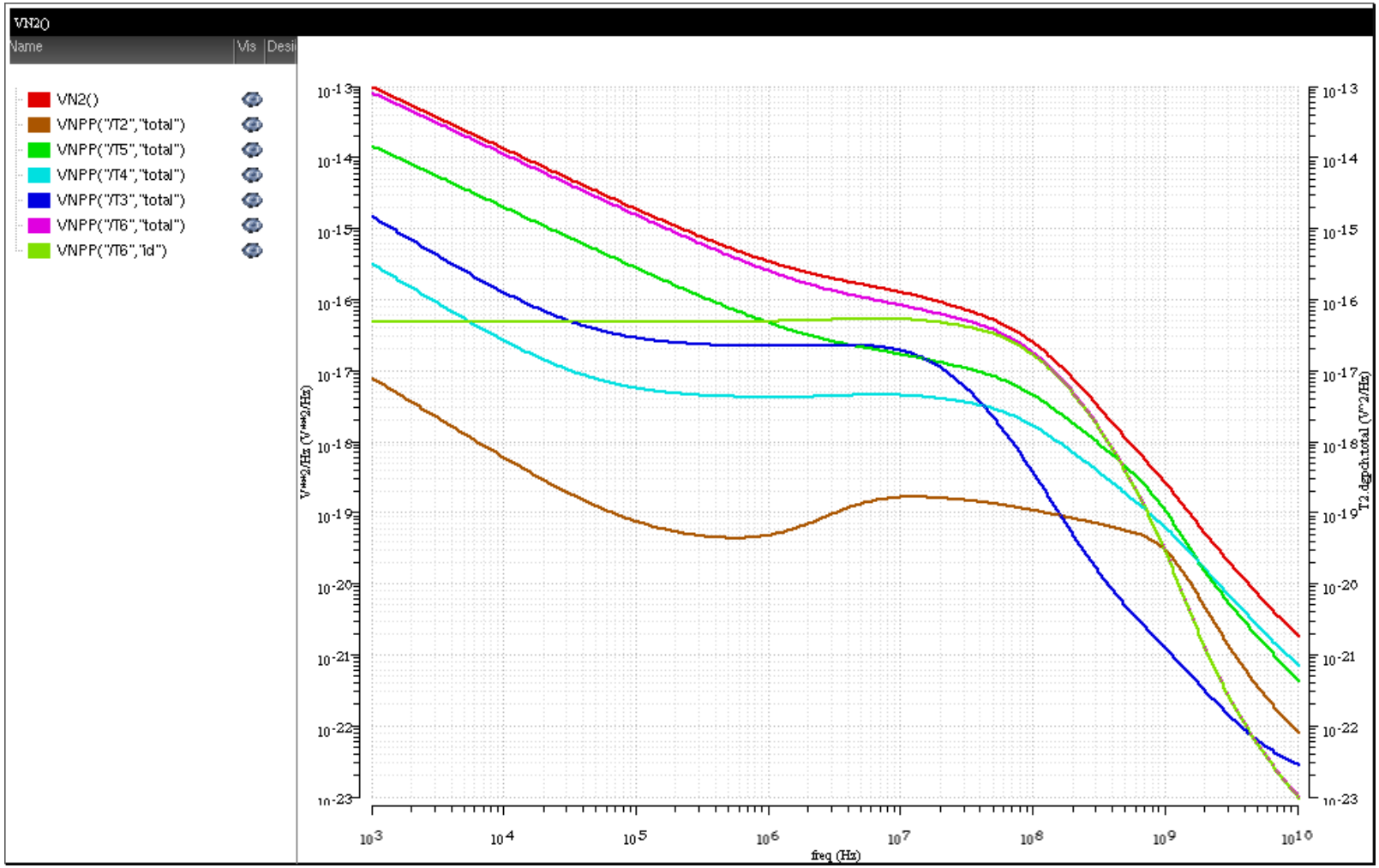
Input reference

AC noise analysis:

Plot of pre-amplifier noise density against frequency (total in red)

Different noise sources can be identified (total, flicker, id, rs, rd)

Easy to pick out the major noise source at each frequency

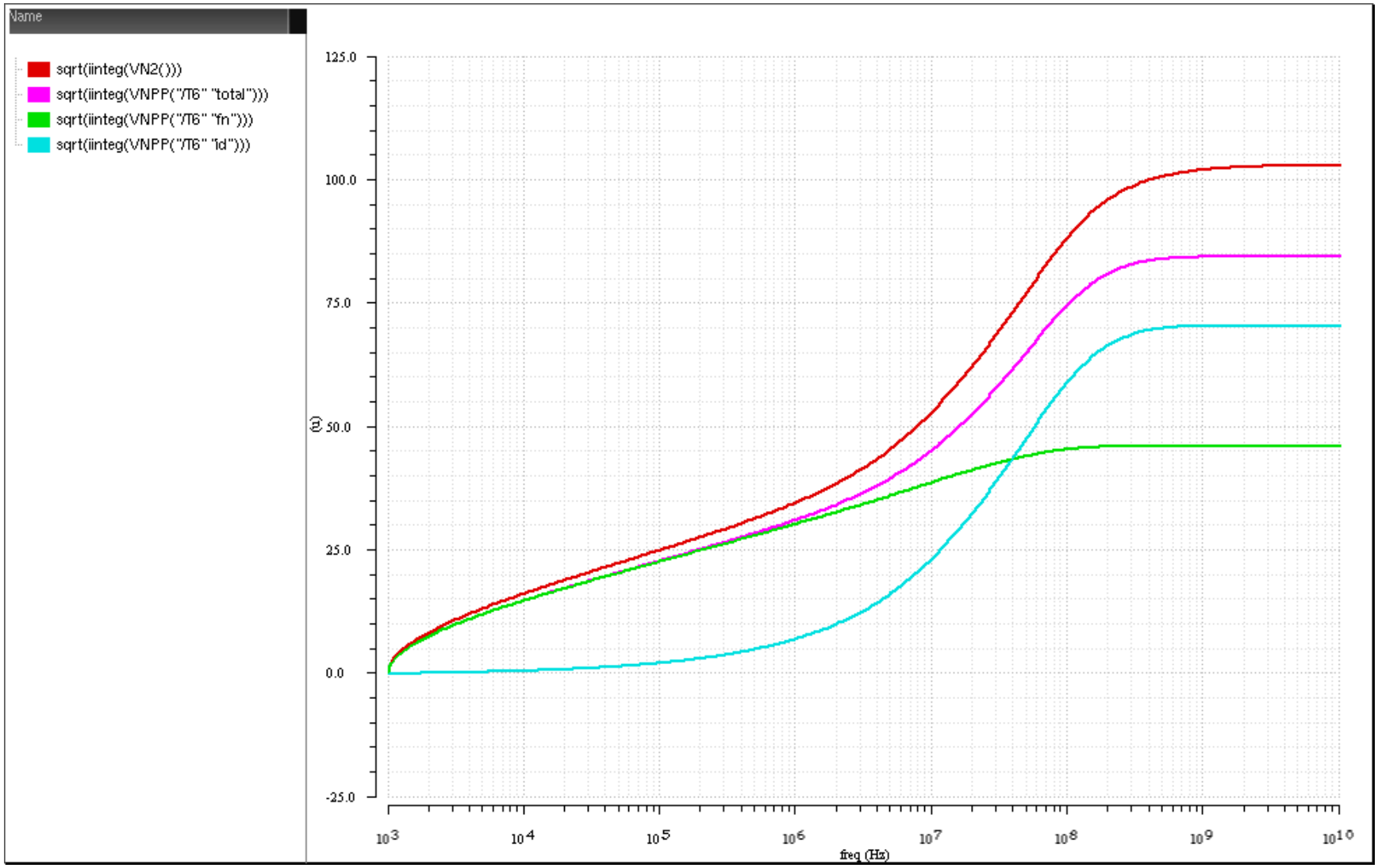


AC noise analysis:

Plot of integrated noise density against frequency for T6 (total, fn, id noise)

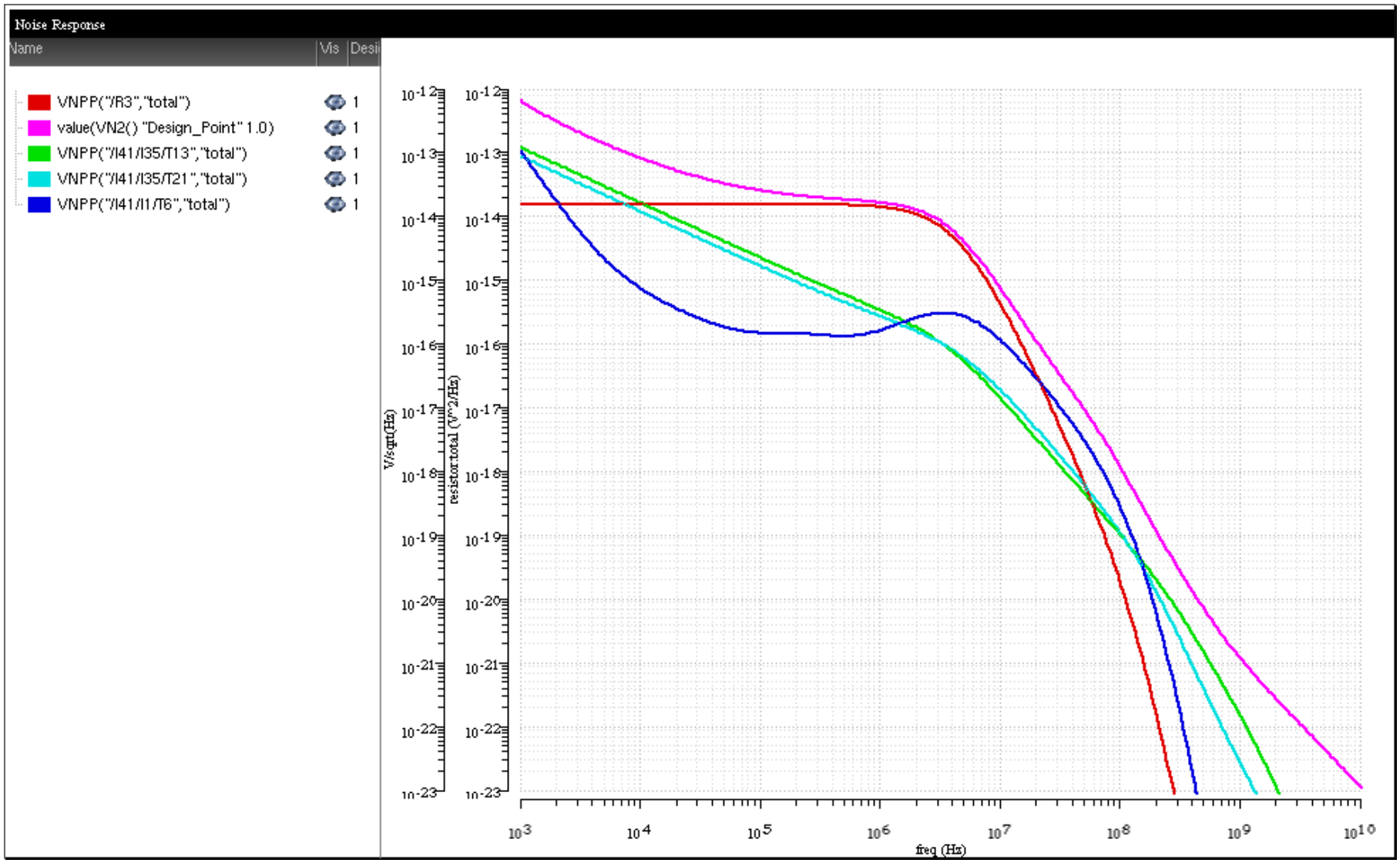
Amplifier total noise in red

Plots clarify the frequency range over which noise accumulates.



AC noise analysis for full MGPA channel with detector

Red trace is detector leakage noise (10uA)



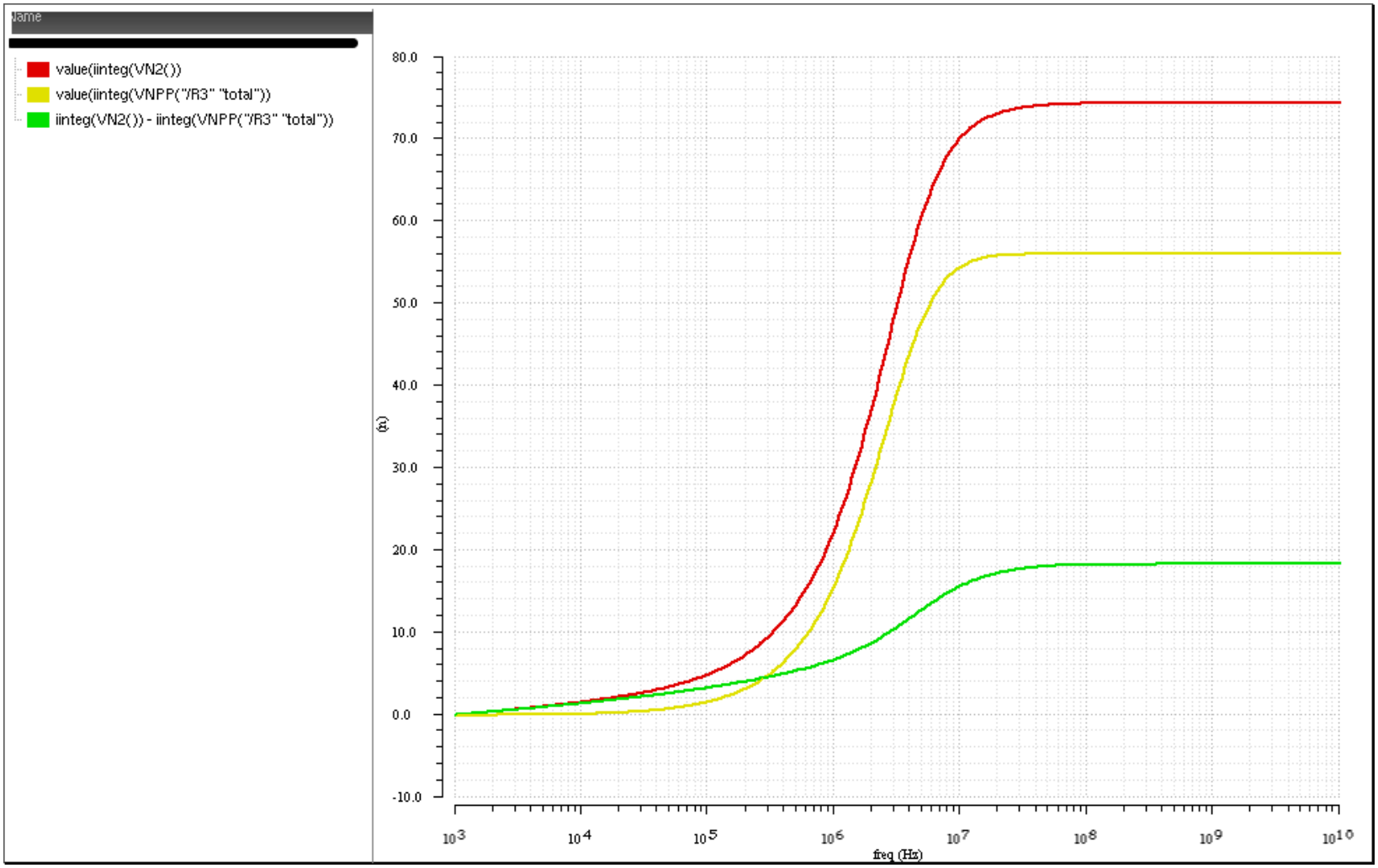
Noise contributions by device and type of noise

Integrated Noise Summary (in V^2) Sorted By Device Composite Noise
Total Summarized Noise = 7.44614e-08
Total Input Referred Noise = 42.1206

Device	Param	Noise Contribution	% Of Total	
/R3	rn	5.60988e-08	75.34	[detector leakage]
/R23	rn	2.6837e-09	3.60	[feedback resistor]
/I41/I35/T13	fn	1.84469e-09	2.48	
/I41/I1/T6	id	1.71803e-09	2.31	
/I41/I1/T6	fn	1.52038e-09	2.04	
/I41/I35/T21	fn	1.41232e-09	1.90	
/I41/I35/T15	fn	9.35404e-10	1.26	
/I41/I1/T3	id	6.02088e-10	0.81	
/I41/I35/T23	fn	5.92281e-10	0.80	
/R24	rn	5.42903e-10	0.73	

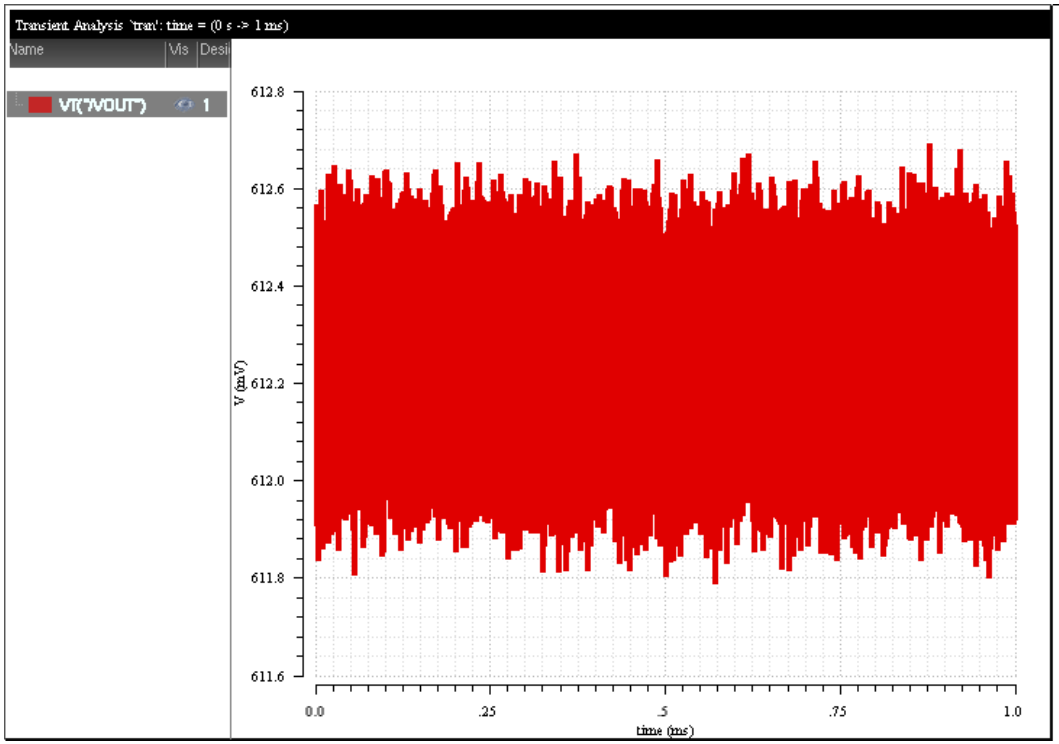
Integrated Noise Summary (in V^2) Sorted By Noise Contributors
Total Summarized Noise = 7.44614e-08
Total Input Referred Noise = 42.1206

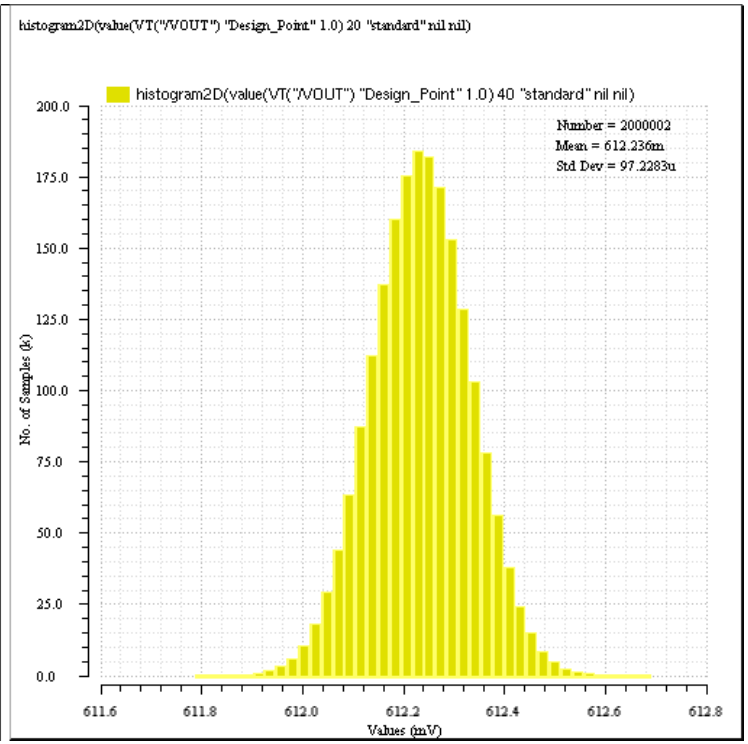
Noise contributions (indefinite integrals). Detector leakage 10uA is the dominant noise source (yellow trace), but other noise sources (green) add up to ~25% of total



Transient noise analysis:

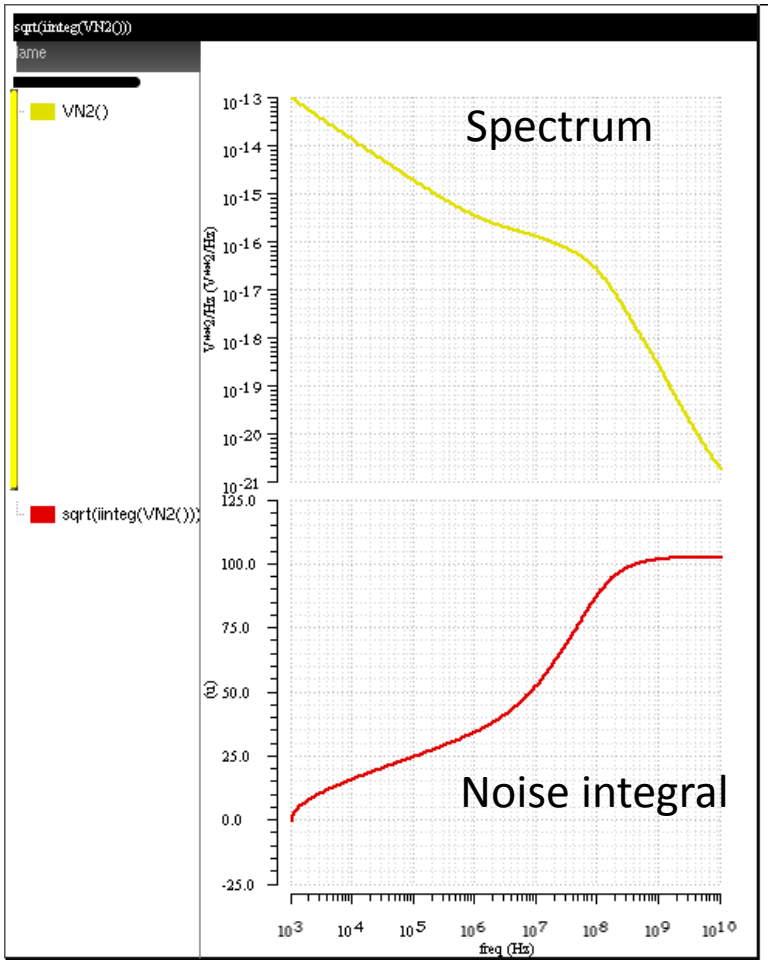
- Plot of time domain noise from all components (by default)
- Includes model of flicker noise gradient
- Noise can be stored for all nets and terminals
- Individual noise sources cannot be separated after analysis, but components can be individually enabled/disabled during simulation set up
- Analysis can be very slow (~1000 times slower than AC)
- Care needed in selection of noise bandwidth (Fmax) and run time

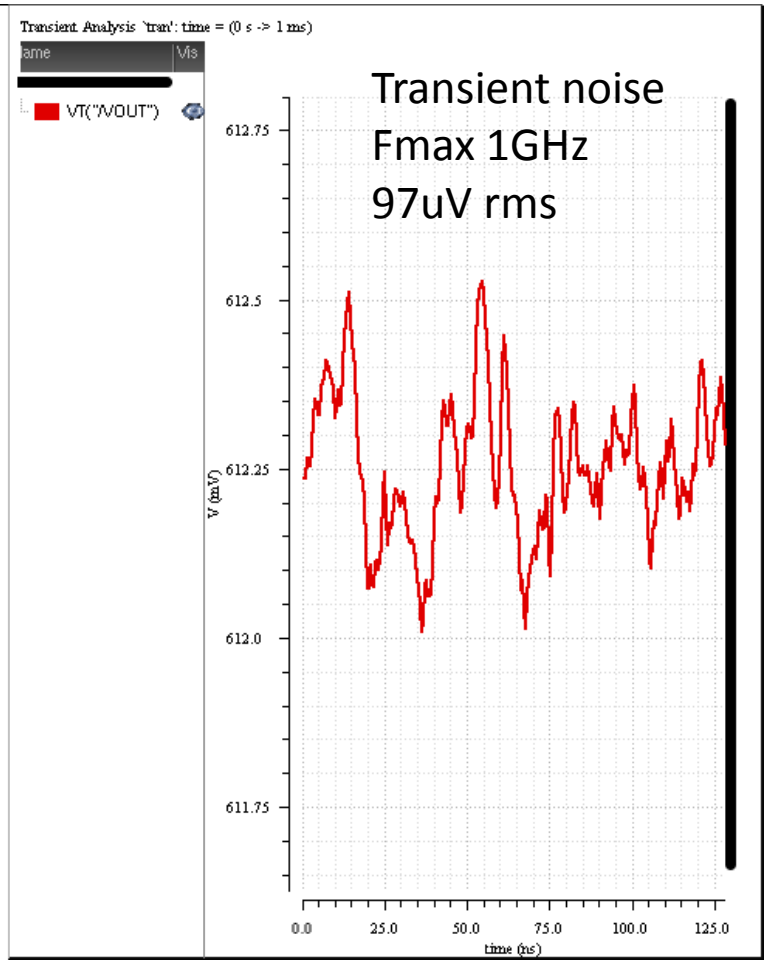




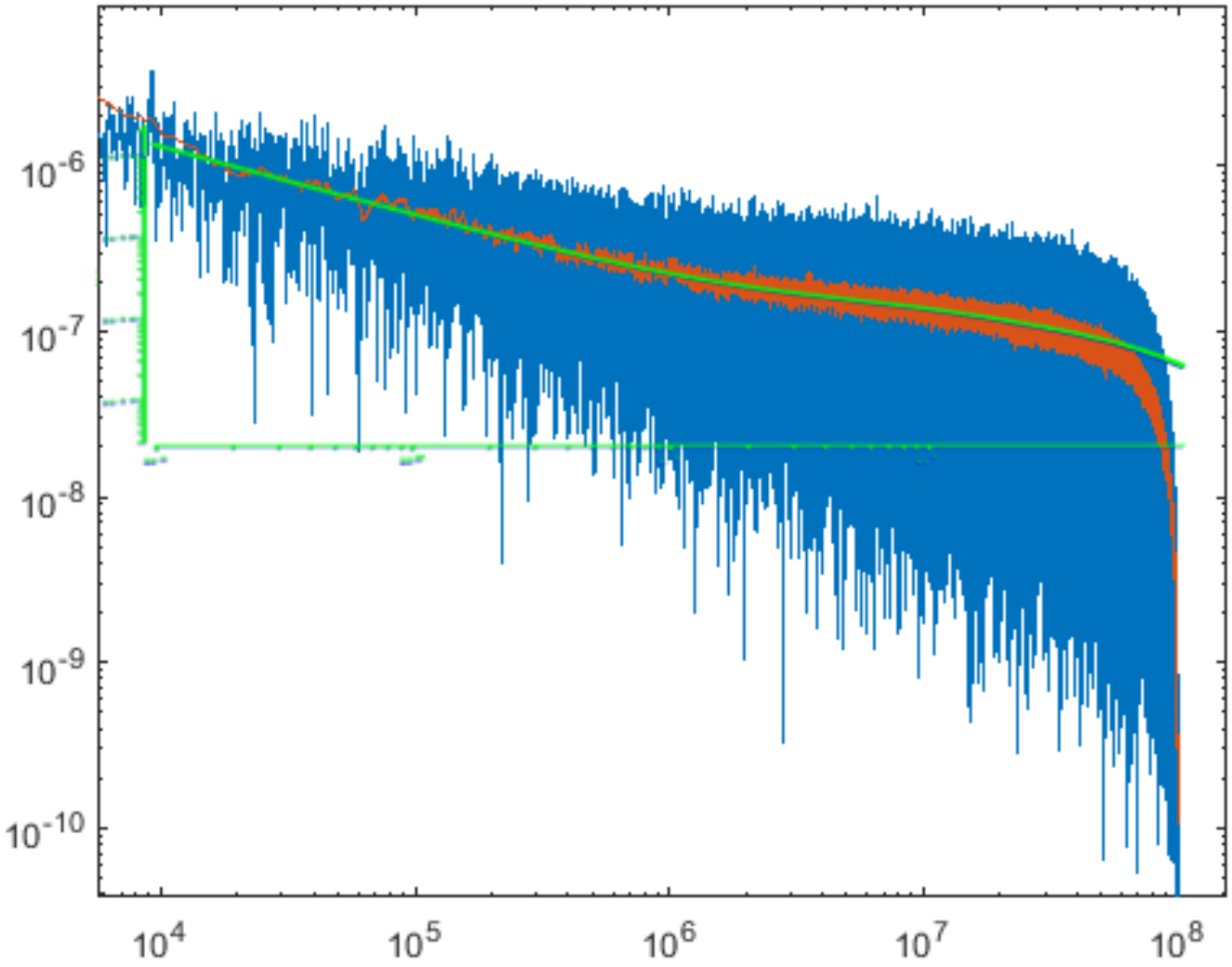
AC noise compared to transient noise

Integrated noise: 103uV rms AC, 97uV rms transient
AC from 1kHz, transient for 1ms
Effective noise shaping is not exactly the same for the two simulations





Comparison between transient noise FFT and AC noise.



FFT
Smoothed FFT
AC noise

Transient noise with Fmax 1e8, showing inaccuracies towards the edge of the range
Best to set Fmax >10 times higher than frequency range of interest.
Match for flicker noise corner and gradient is perfect

Waveform analysis and processing:

The Cadence design framework allows mathematical functions
of waveforms to be created and displayed eg

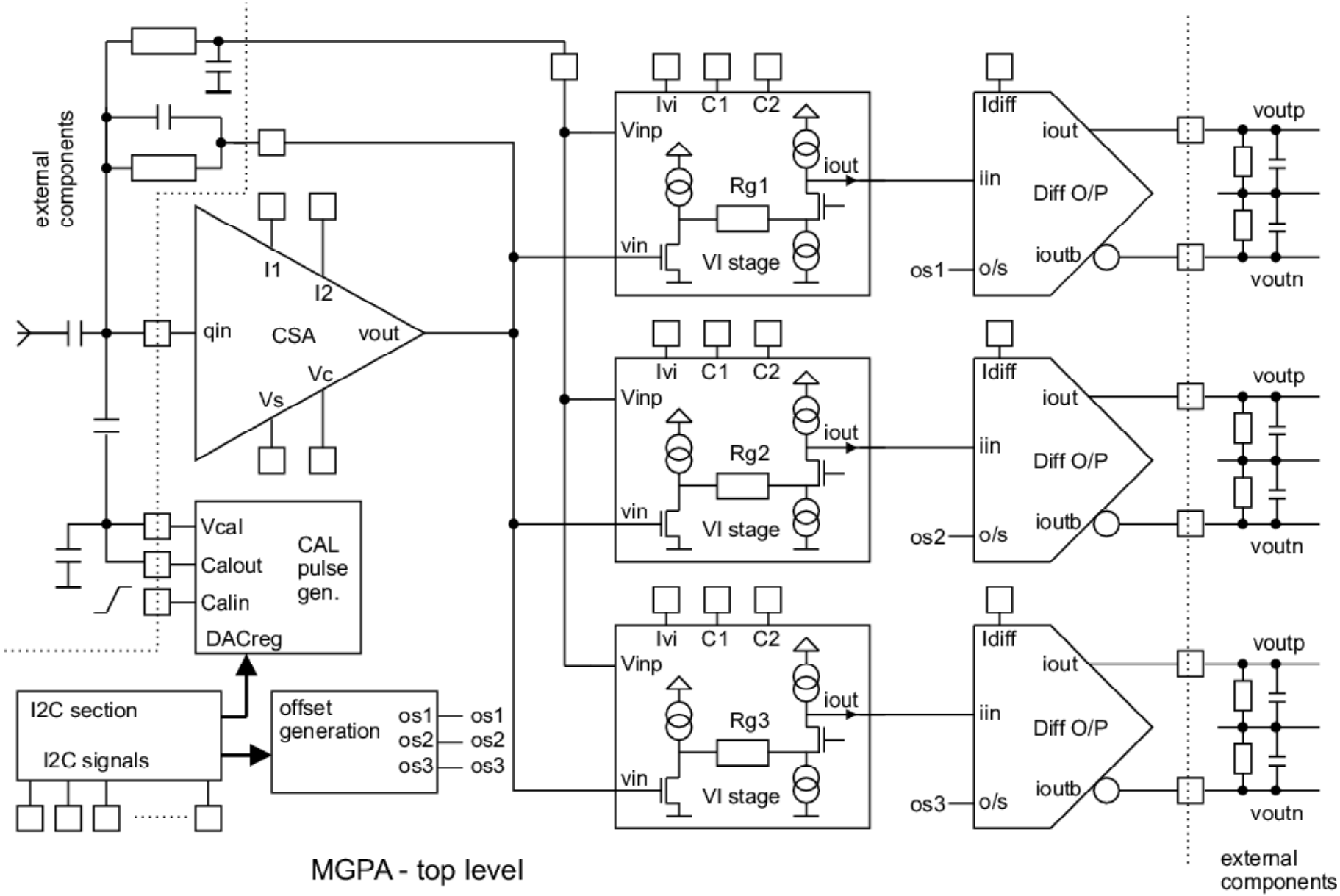
Peak-hold: ymax(sample(VT("/CSA_FILT_DIFF") 0.0 1e-07 "linear" 1e-10))
Sample and hold: value(VT("/CSA_FILT_DIFF") 535n)

These functions are used extensively in the spike discrimination evaluation, as there are not any equivalent functional circuit blocks in the MGPA design (IP blocks from other projects would not be fast enough).

The updated MGPA will require new circuits to provide fast PH/sampling to give the same performance as the mathematical functions.

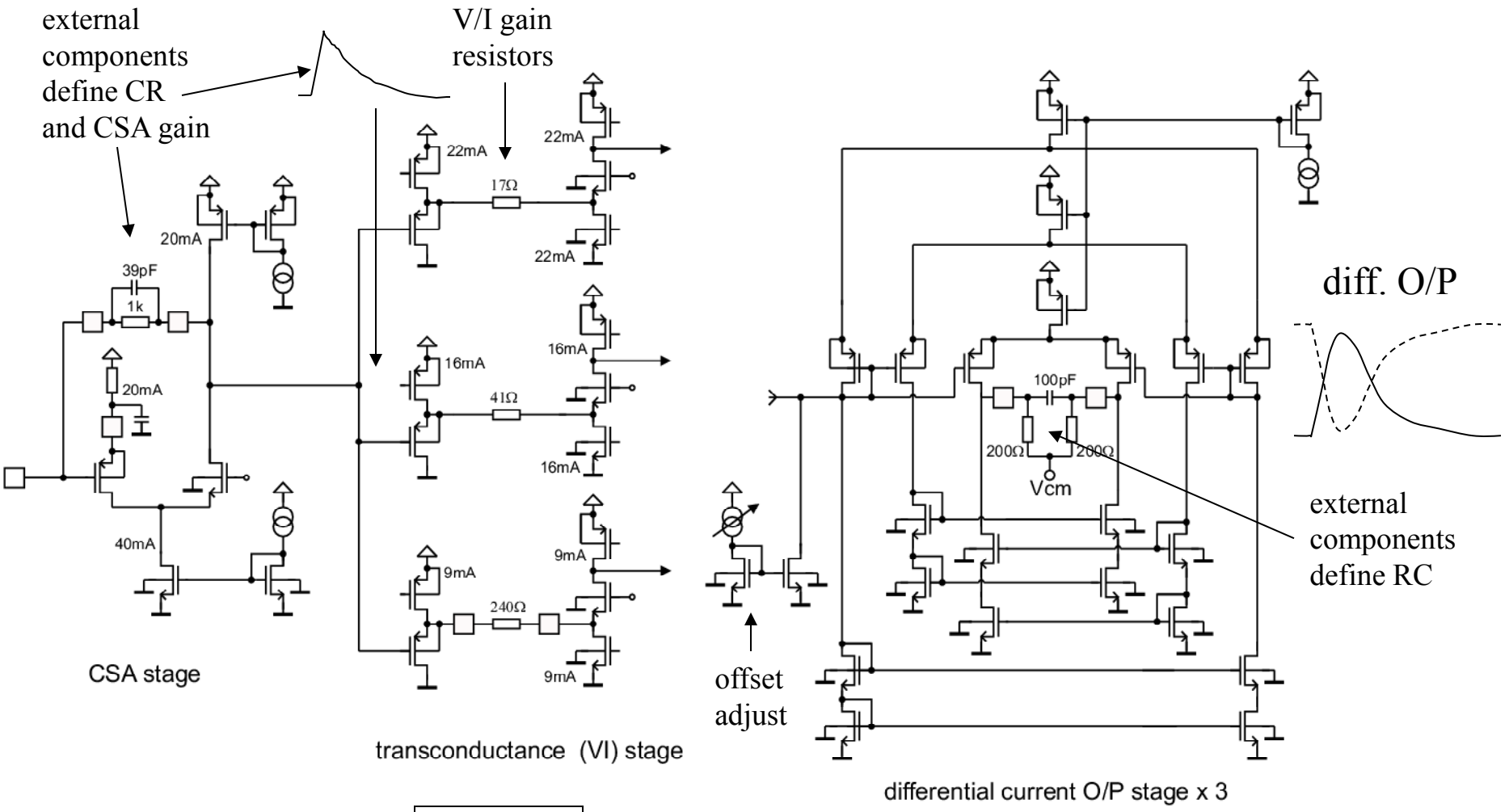
For more complex waveform processing, the waveforms can be exported as text files for MATLAB analysis (eg spike/scintillator efficiencies).

The existing design: CSA ---------- three gain stages (x1,x6,x12) with buffering

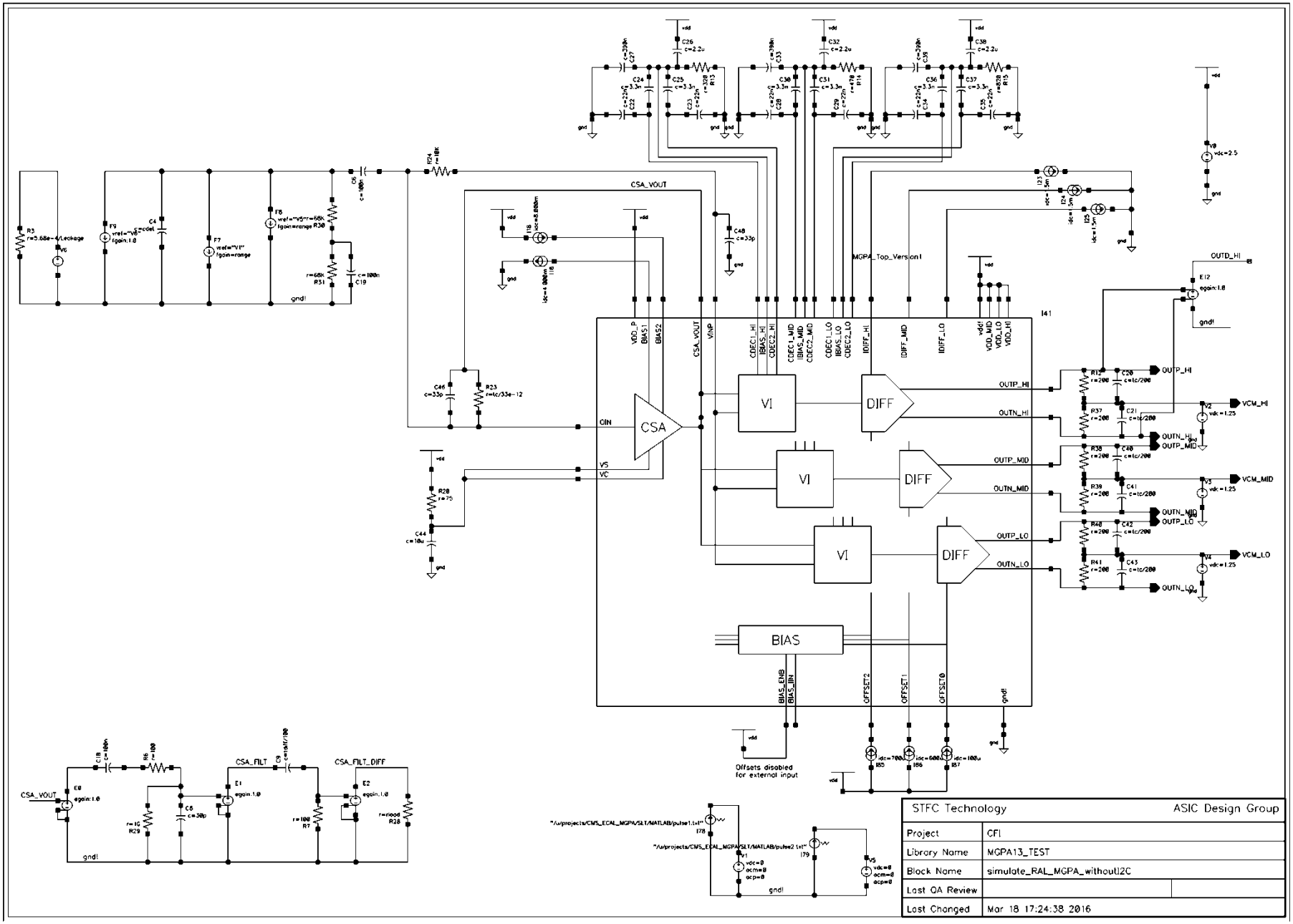


MGPA - top level

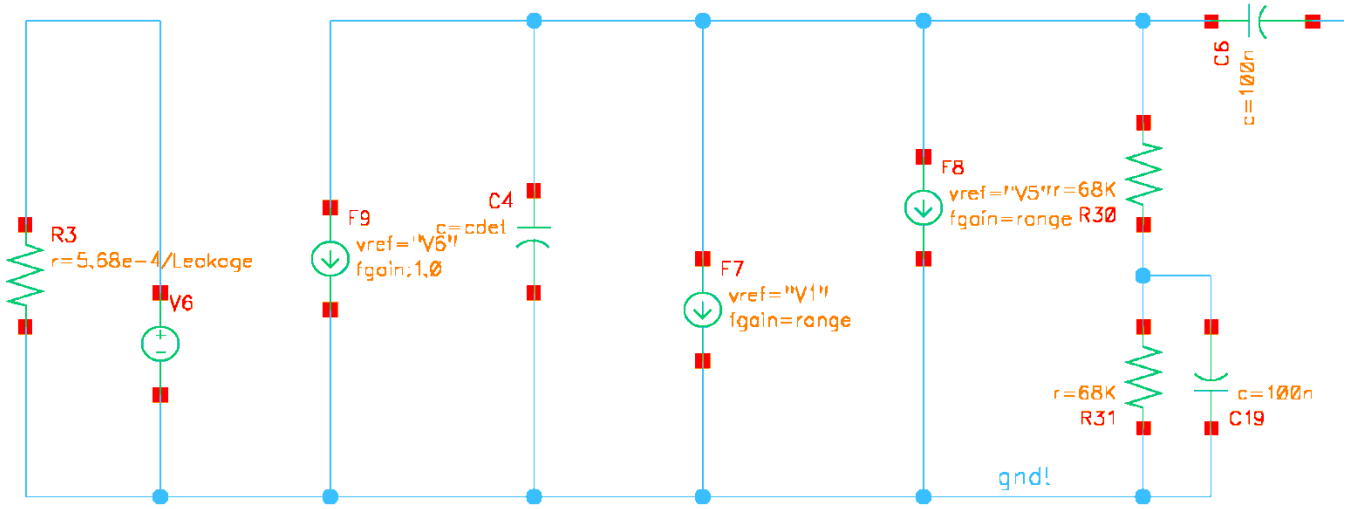
MGPA – architecture detail



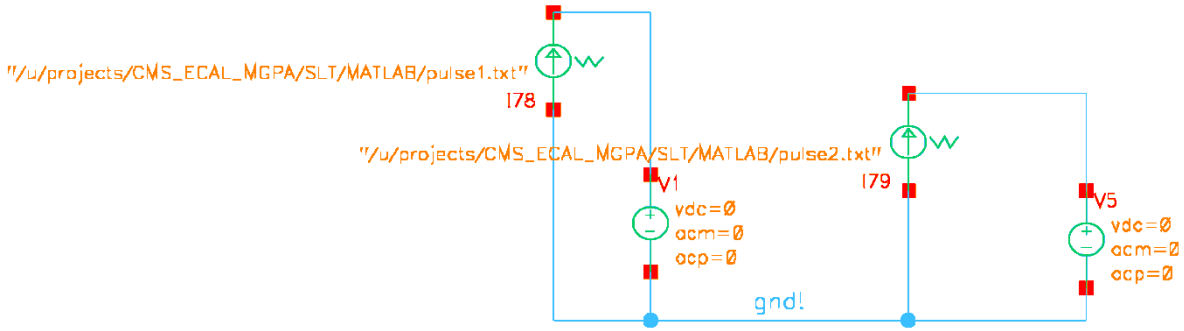
I2C interface → offset & CAL pulse generation


CSA_VOUT
MGPA_Top_Version1
CSA
VI
DIFF
BIAS
OUTP_HI
OUTN_HI
OUTP_MID
OUTN_MID
OUTP_LO
OUTN_LO
VCM_HI
VCM_MID
VCM_LO
CSA_FILT
CSA_FILT_DIFF
Offsets disabled
for external input
STFC Technology
ASIC Design Group
Project
CFI
Library Name
MGPA13_TEST
Block Name
simulate_RAL_MGPA_without12C
Last OA Review
Last Changed
Mar 18 17:24:38 2016

Simulation environment



Detector noise sqrt(4kT/R)=5.4e-9sqrt(Leakage), R=5.68e-4/Leakage

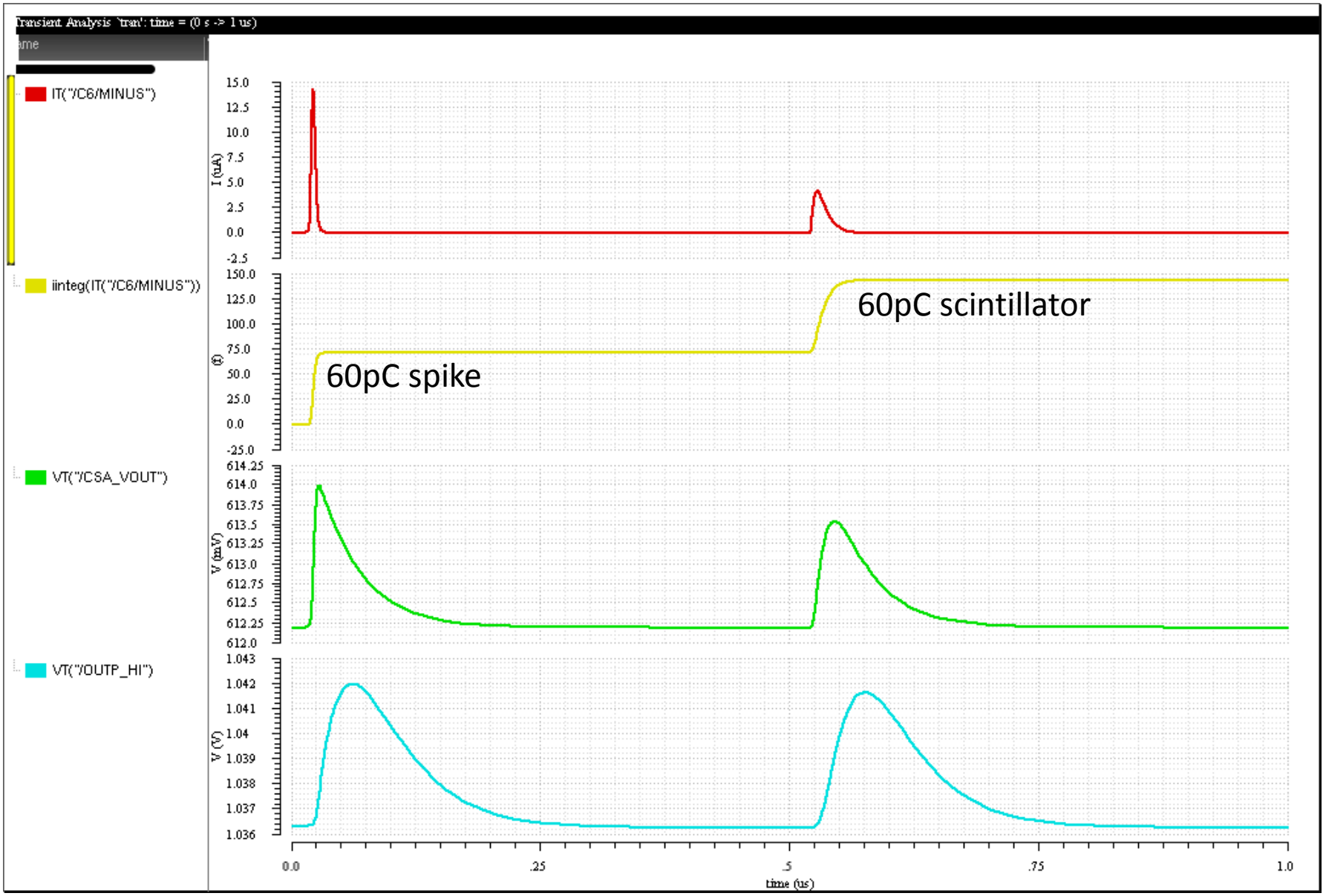


Piecewise linear current waveforms from MATLAB script

MATLAB Detector pulse modelling

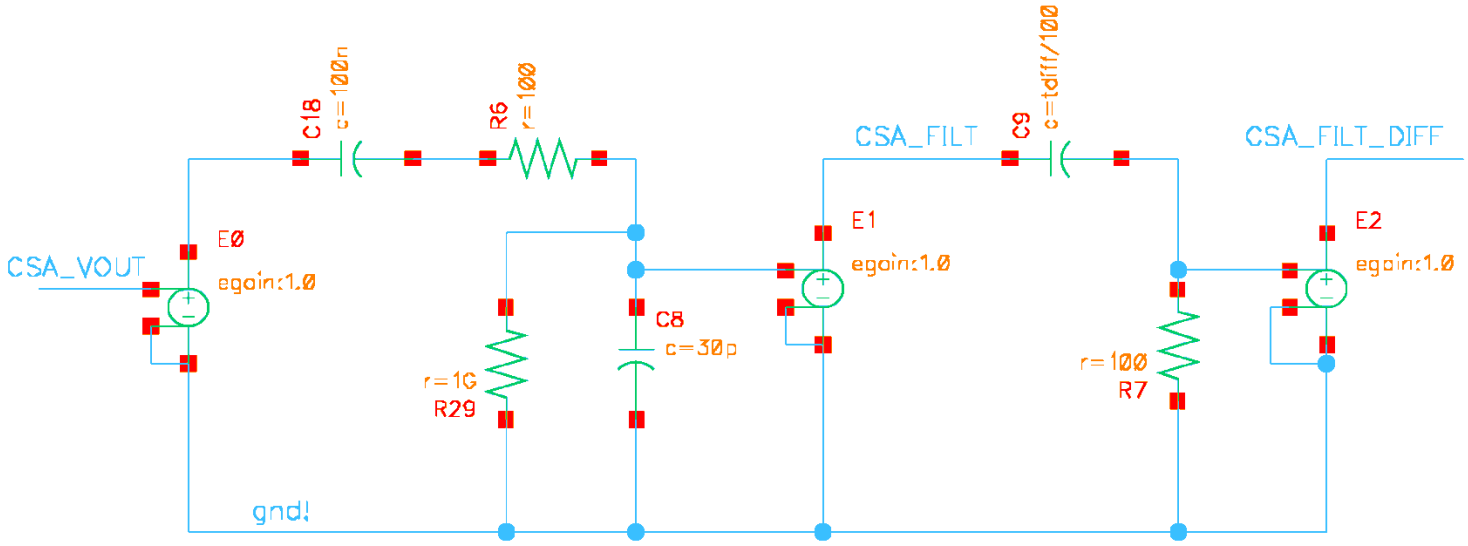
```
t=[0:1e-10:2e-7]; %200ns window, 2001 points
qin=60e-12; %full scale range
t0=20e-9; %delay for first (spike) pulse
tlpf=3.5e-9; %low pass filter
tscint=8.4e-9; %decaying scintillator light
sigma=1.5e-9; %resolution term
v1=exp(-(t-t0).^2/2/sigma^2); %spike signal
v1=qin*v1/trapz(t,v1); %normalisation for qin total charge
v2=-exp(-t/tlpf)+exp(-t/tscint); %scintillator
v3=conv(v1,v2); %scintillator convolution
v3=v3(1:2001); %reduce to 2001 points
v3=qin*v3/trapz(t,v3); %normalisation
f1=fopen('pulse1.txt','w');
f2=fopen('pulse2.txt','w');
for i=1:2001
    fprintf(f1,'%e %e\n',5e-7+t(i), v3(i));
    fprintf(f2,'%e %e\n',t(i), v1(i));
end
```

Preamp current input, integral, output and shaper high-gain output



Pre-amp filters:

- Implemented with voltage controlled voltage sources, not transistor-level designs.
- Resistors are noise free (both AC and transient noise)
- Low pass RC = 3ns
- High pass CR variable from 1ns to 10ns

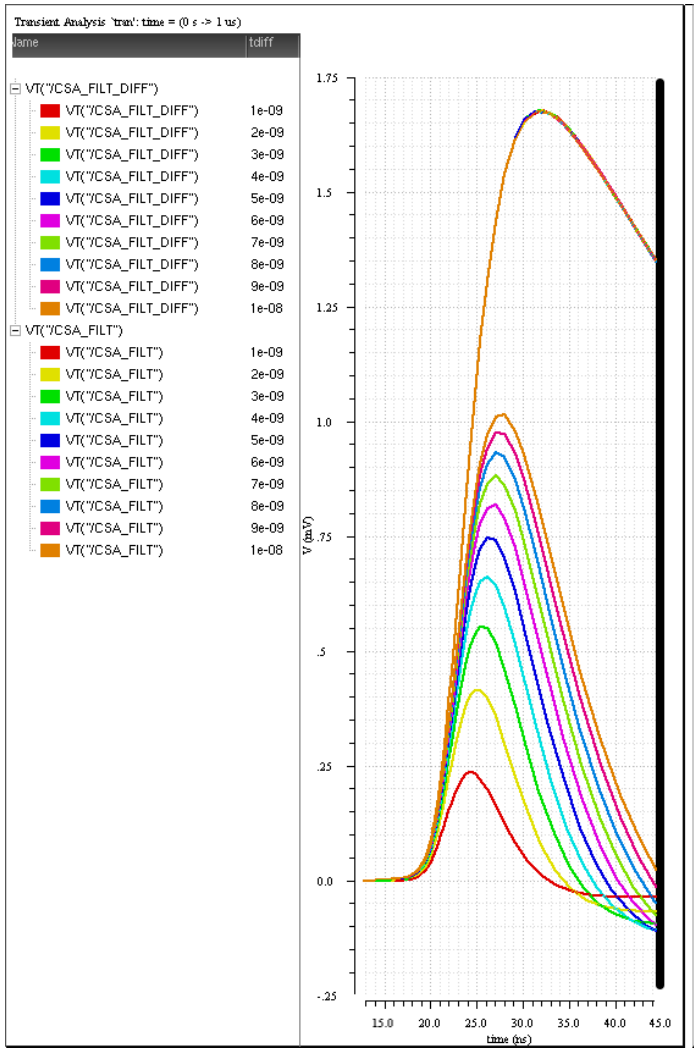


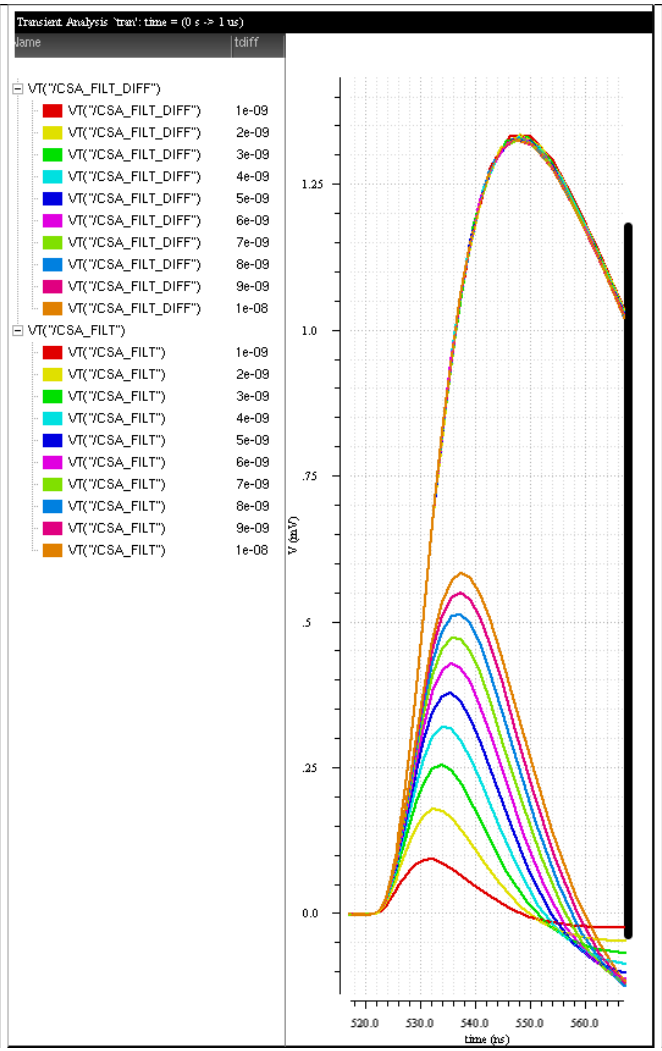
Preamp output before and after high-pass filter (RC from 1-10ns)

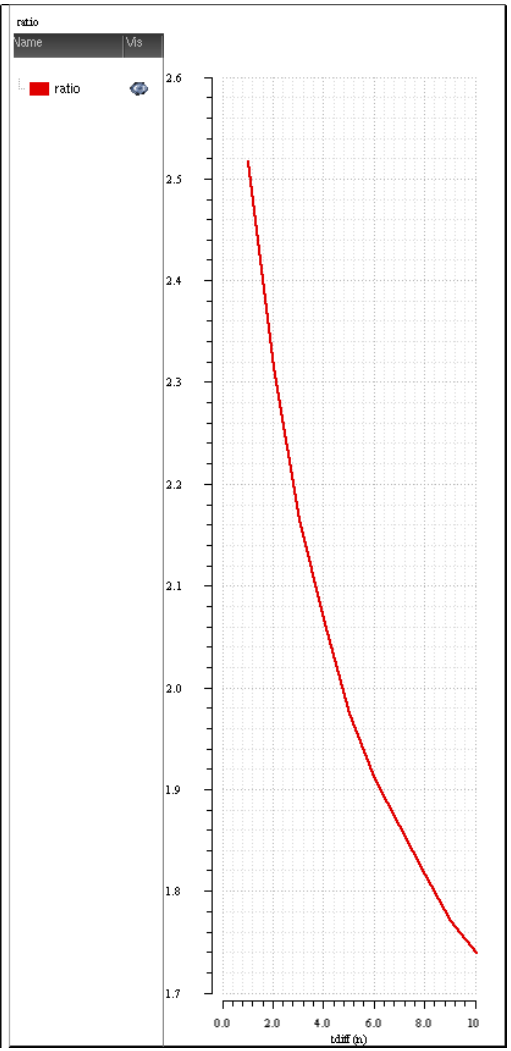
72fC Spike

72fC (2GeV) Scintillator

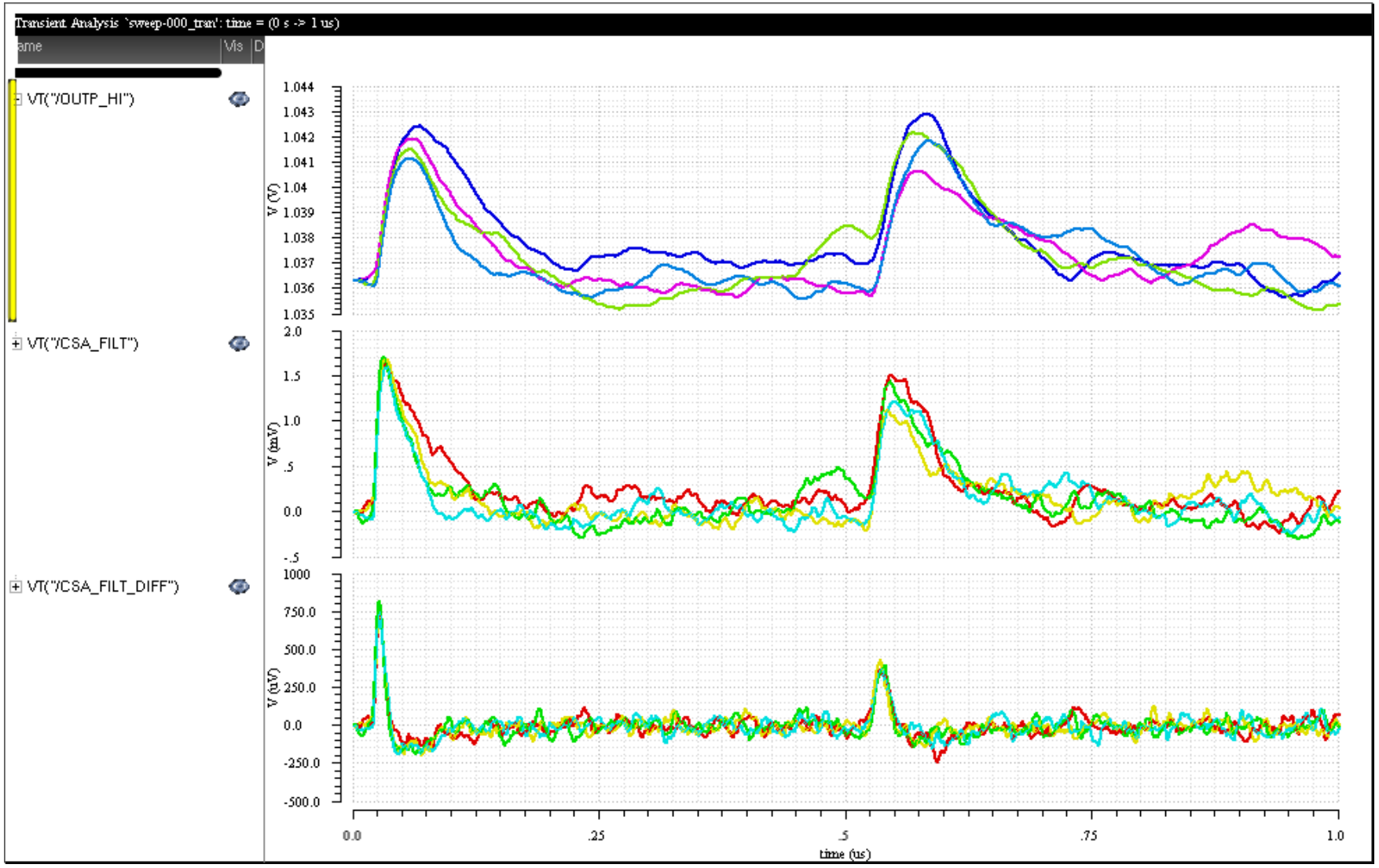
Ratio of peaks after filter





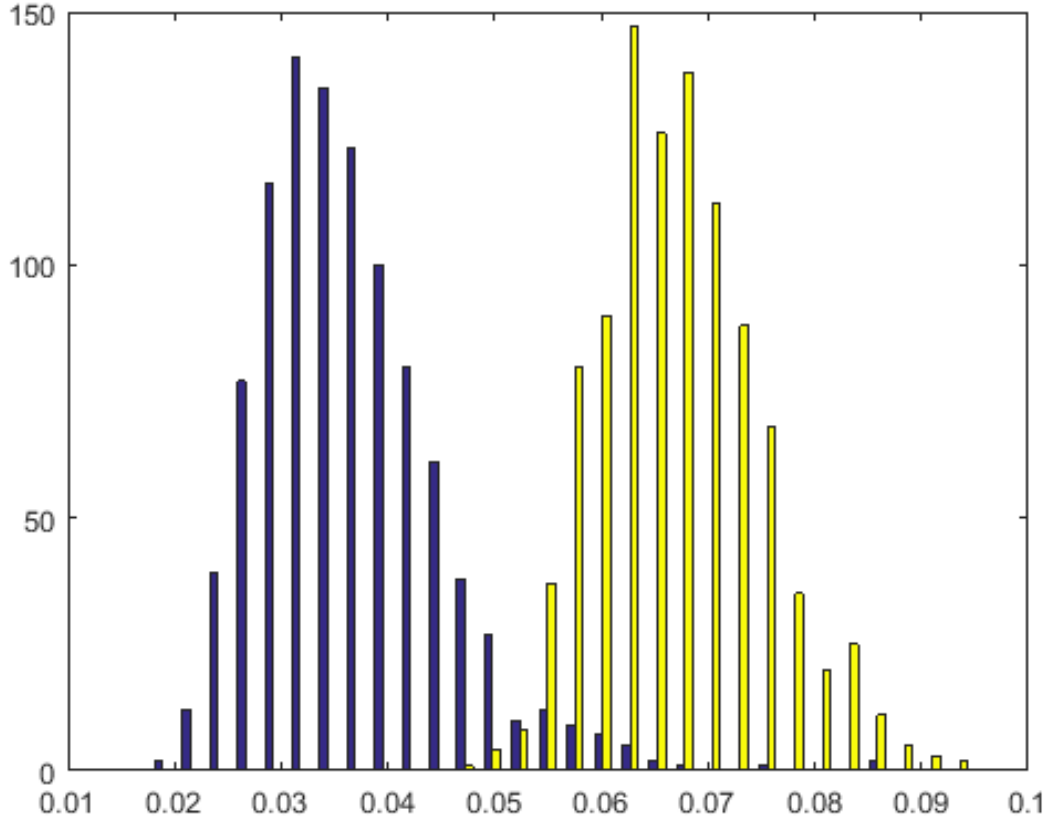


Transient noise: Leakage=100uA, 72fC signals



Histograms of high-pass filter peak divided by shaper peak

Scintillator Spike

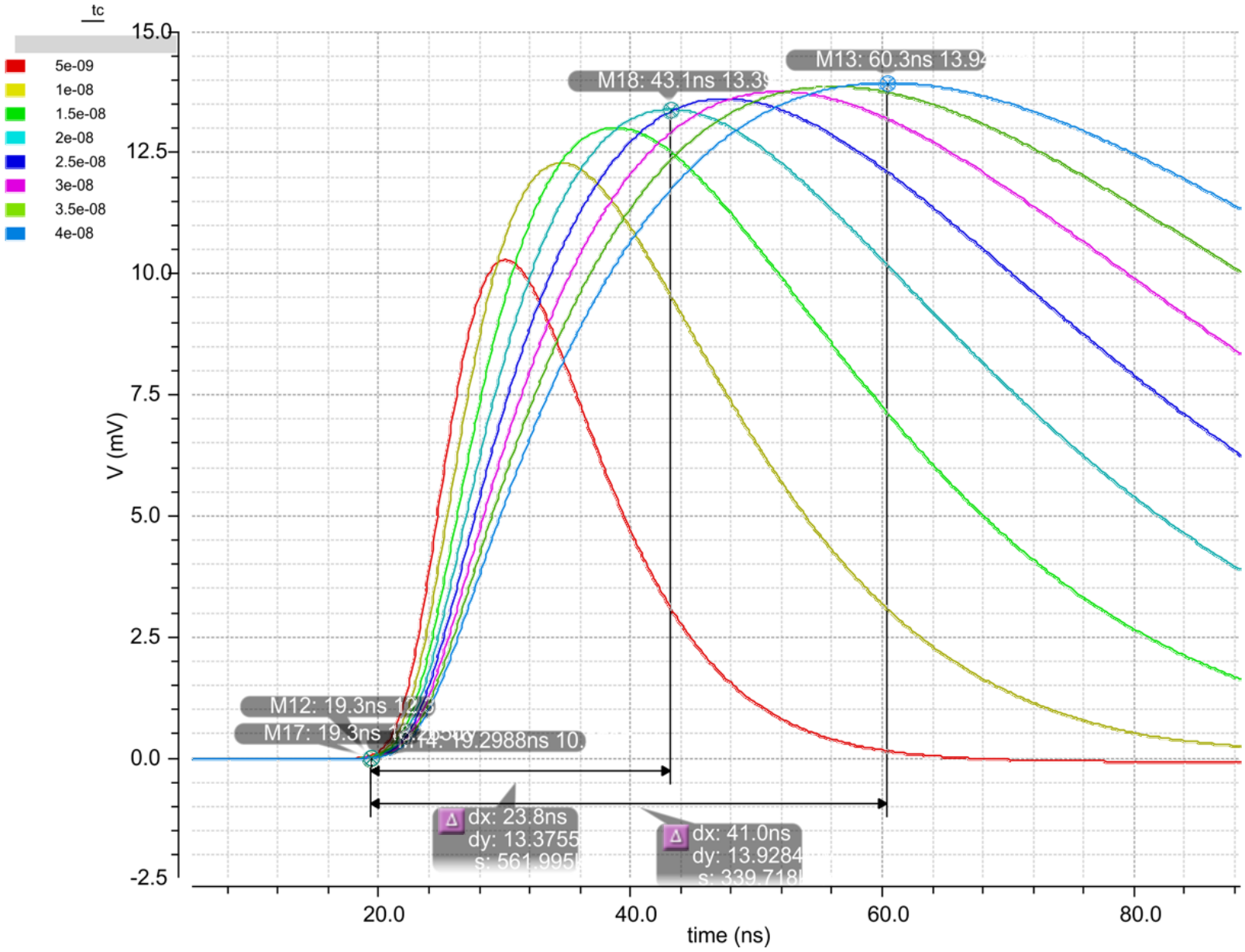


Leakage 200uA
Shaper 40ns
72fC (2GeV scintillator)

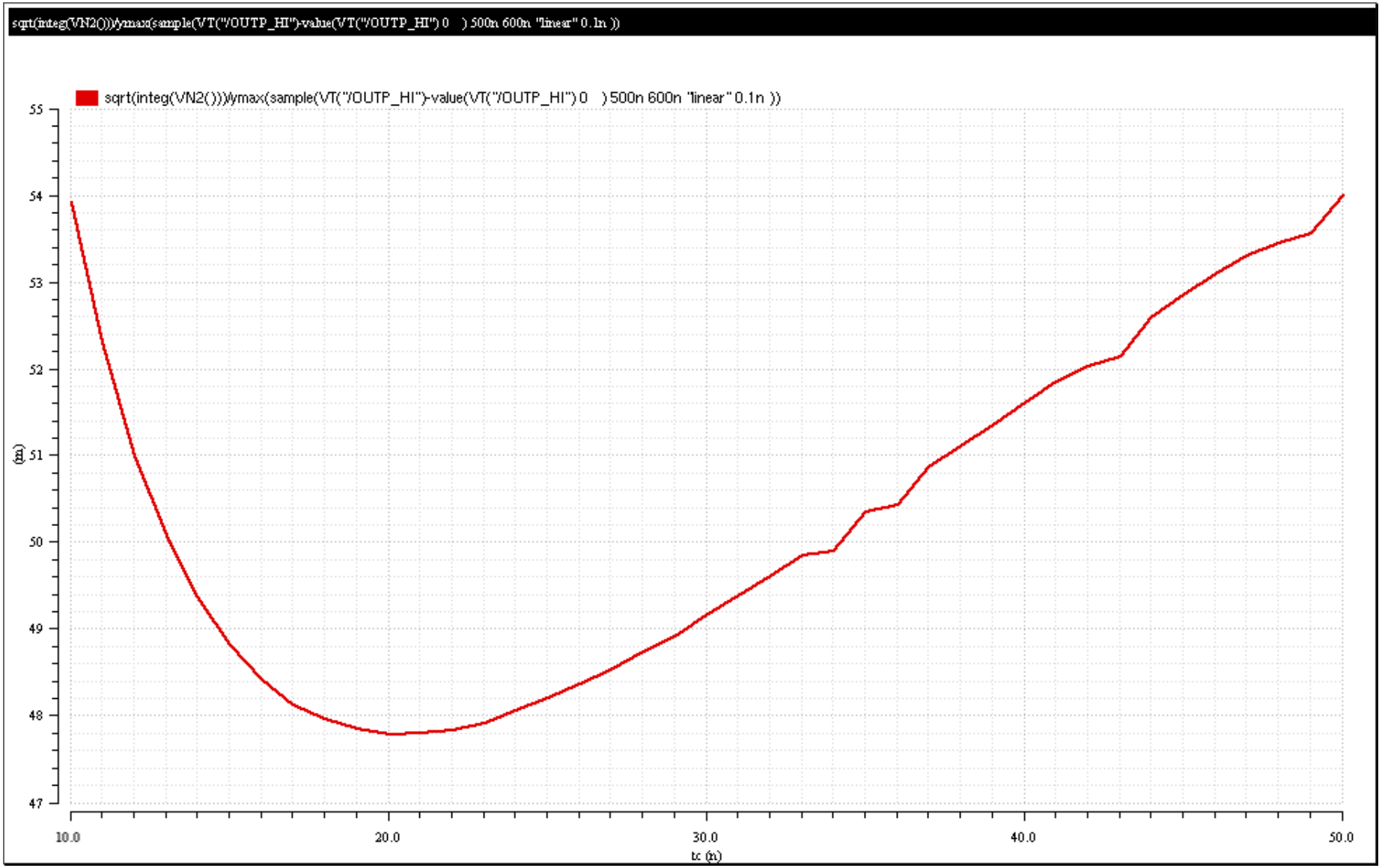
Overlap of plots results in failure of spike discrimination

Spike: histogram of ymax(sample(VT("/CSA_FILT_DIFF") 0.0 1e-07 "linear" 1e-10)) / (ymax(sample(VT("/OUTD_HI") 0.0 1e-07 "linear" 1e-10)) - value(VT("OUTD_HI") 0)))")

Transient responses for different shaper RC time constants 10-40ns

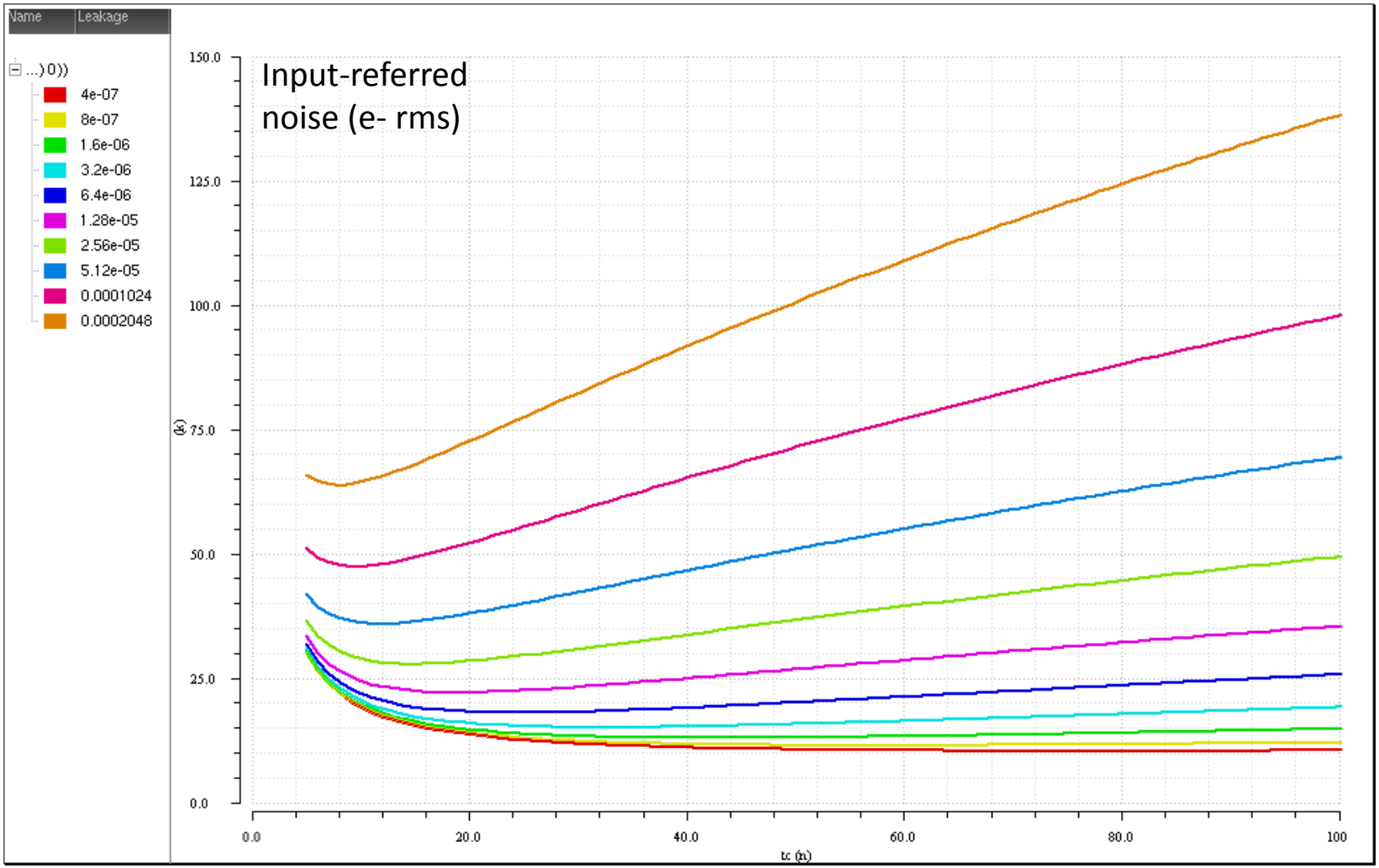


Noise optimisation for leakage 10uA, variable RC time constant



Note shallow gradient near minimum (7% difference between 20ns and 40ns)
Noise is input referred (output noise/scintillator pulse gain)

Noise optimisation for different leakages 0.4uA- 204.8uA

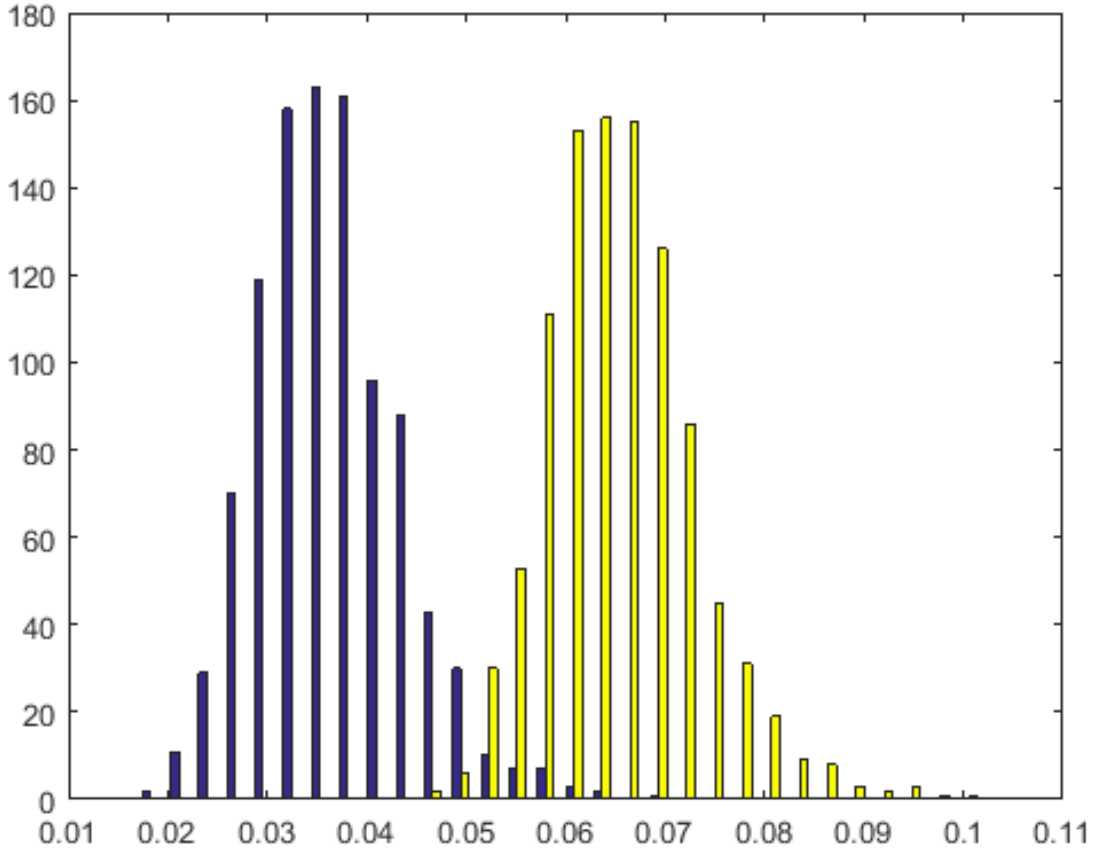


CR-RC time constant (ns)

Baseline noise ~10000 electrons rms, 44MeV rms

Histograms of high-pass filter peak divided by shaper peak

Scintillator Spike

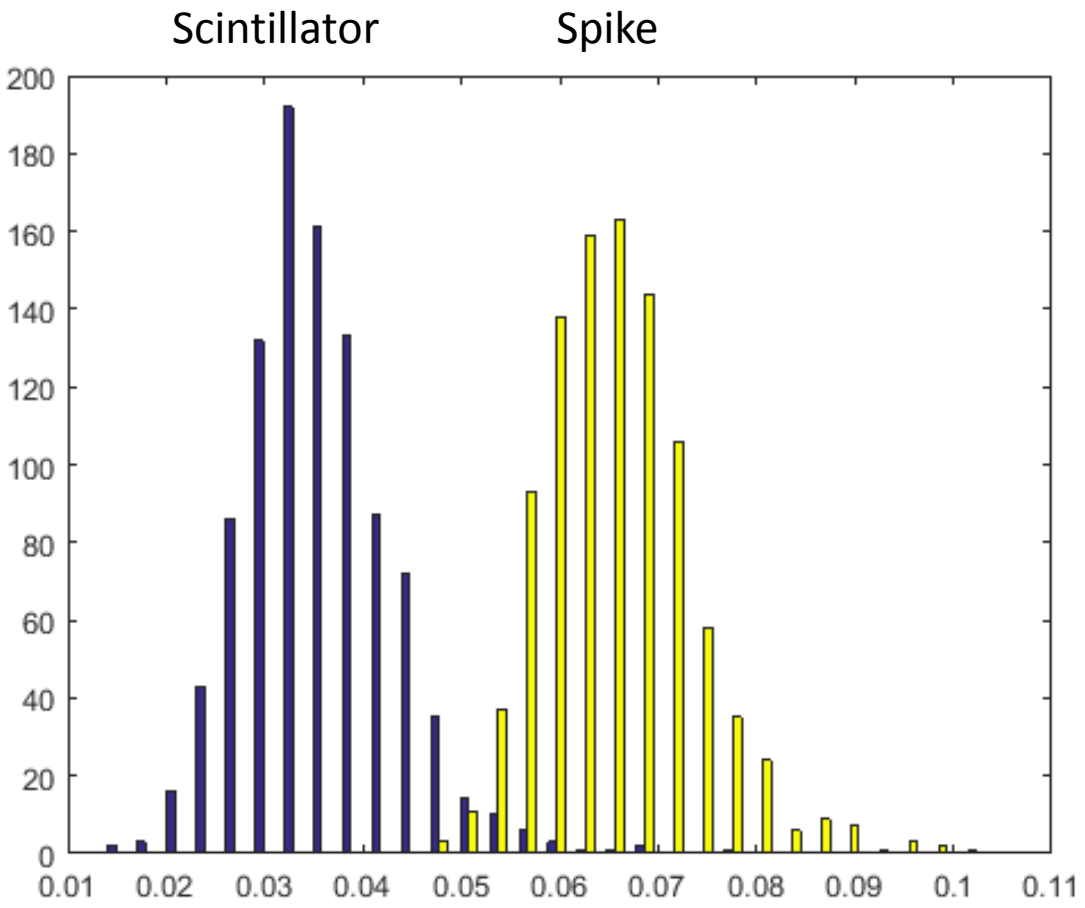


Leakage 200uA
Shaper 20ns
72fC (2GeV scintillator)

Asymmetry in curves looks significant

Spike: ymax(sample(VT("/CSA_FILT_DIFF") 0.0 1e-07 "linear" 1e-10)) / (ymax(sample(VT("/OUTD_HI") 0.0 1e-07 "linear" 1e-10)) - value(VT("OUTD_HI") 0)))")

Histograms of high-pass filter samples divided by shaper output samples



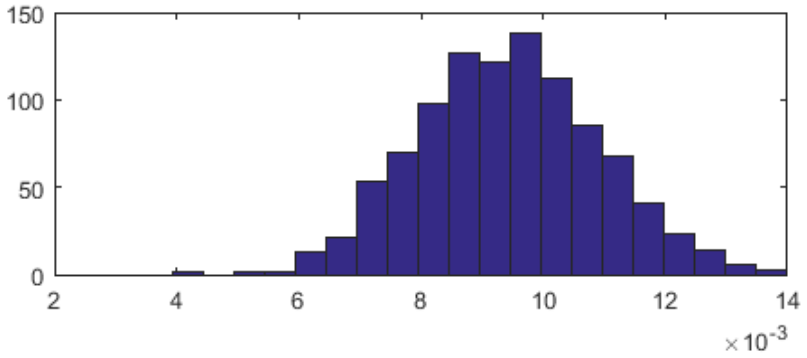
Sample points are the peaks in the noise-free transient response

Fixing the sample points in time avoids skewing the Normal distribution

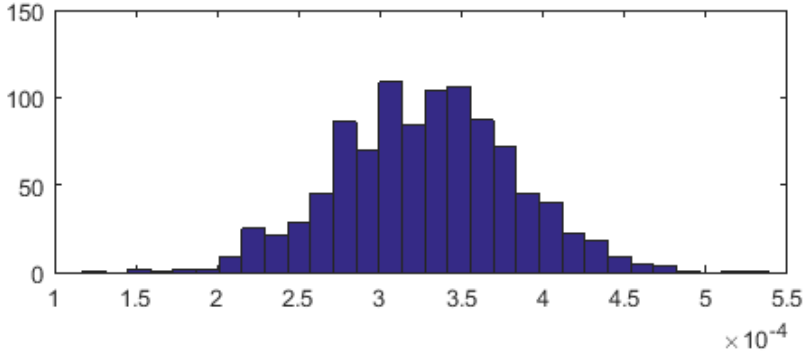
However there is no significant difference in asymmetry, compared to the peak-hold

Spike: value(VT("/CSA_FILT_DIFF") 25.8e-9) / (value(VT("/OUTD_HI") 43.1e-9) - value(VT("OUTD_HI") 0))")

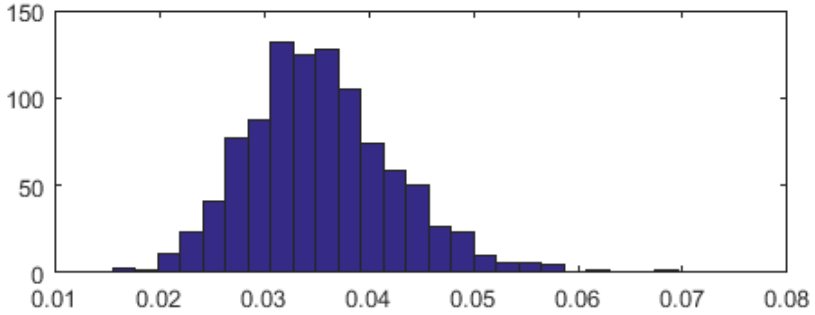
Noise histograms



Shaper output



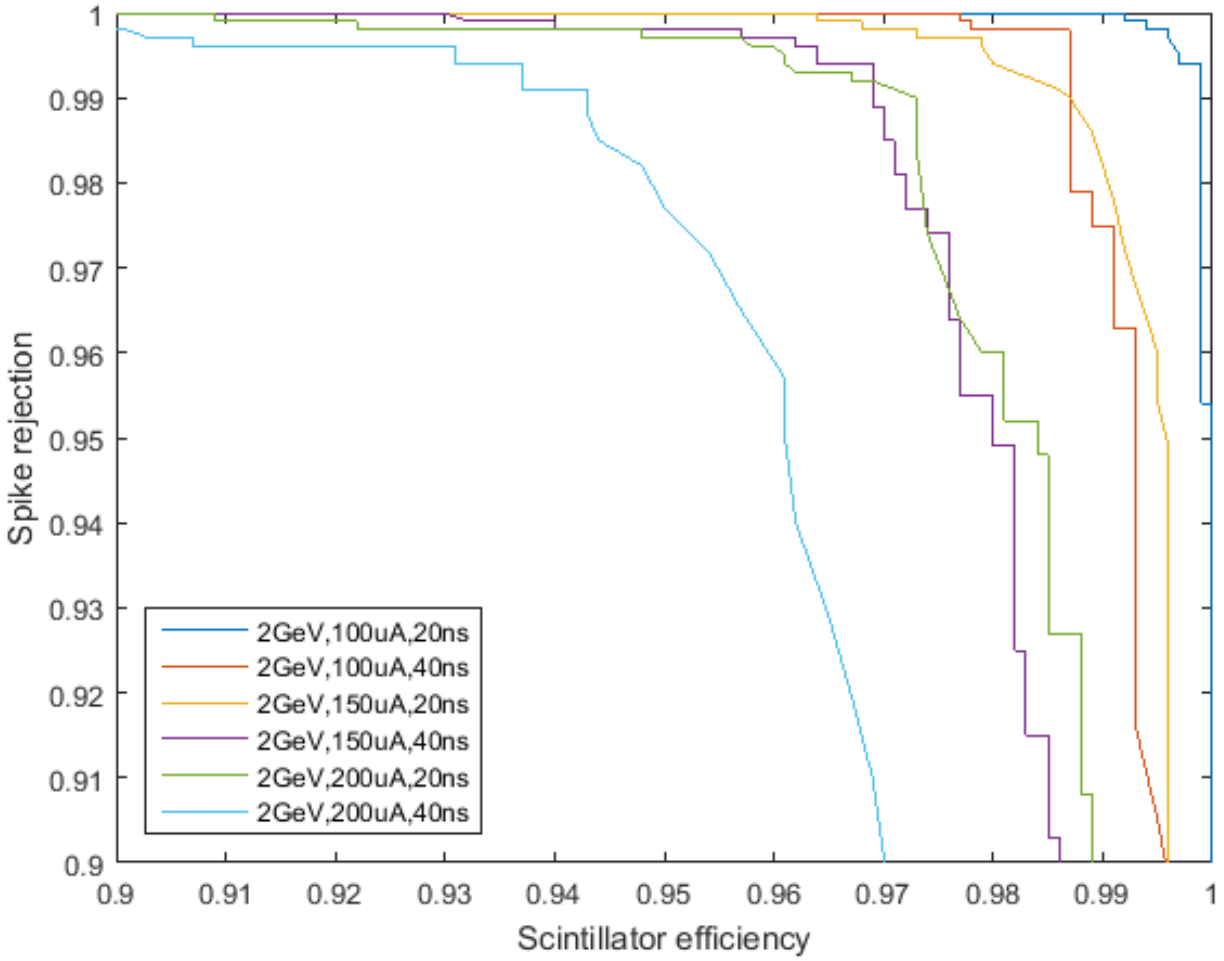
High-pass filter output



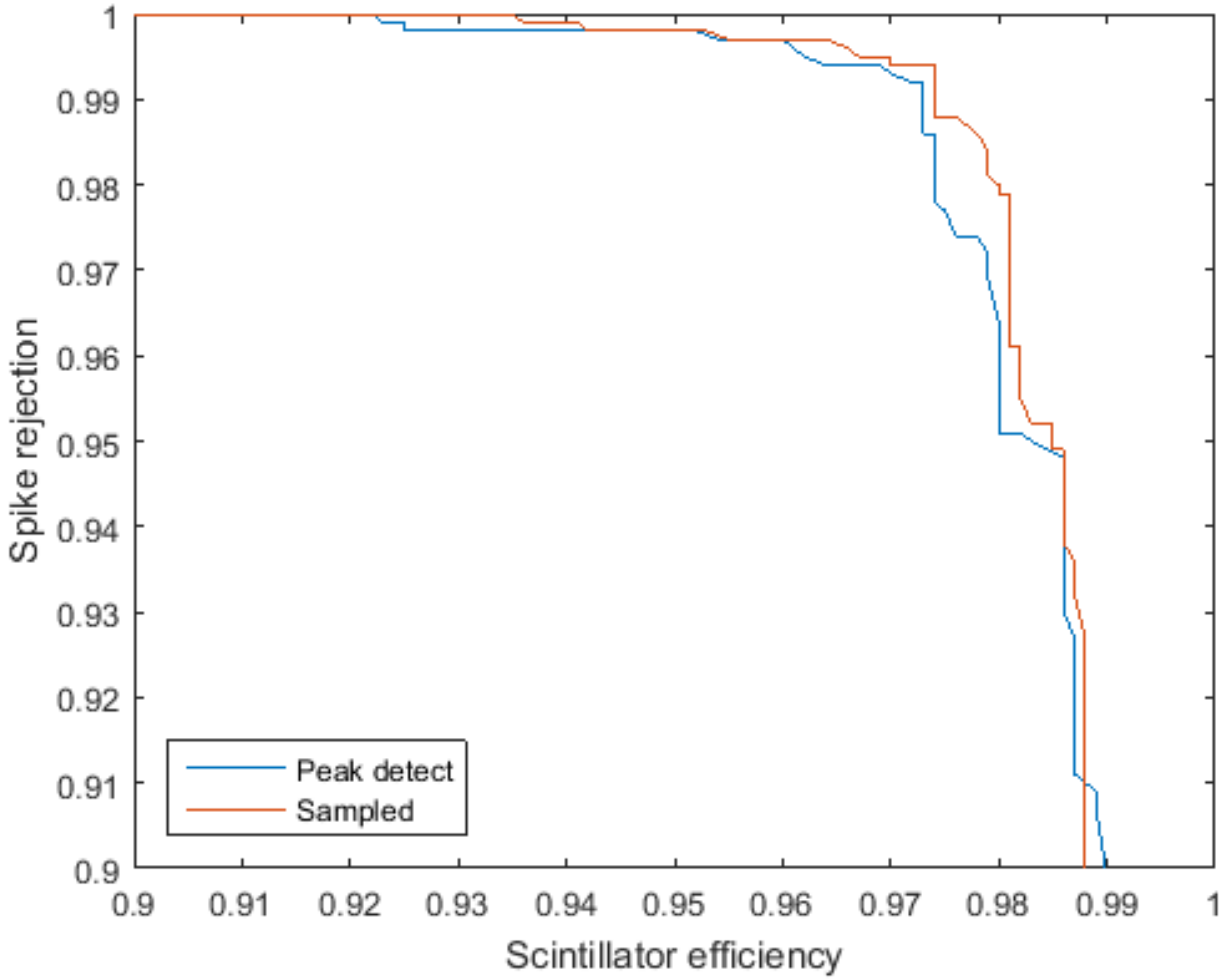
Ratio of filter to shaper
Asymmetry arises from dividing one
Normal distribution by another
It is not related to the peak-hold function

Optimisation of shaper noise would help reduce asymmetry.

Efficiency plots 2GeV

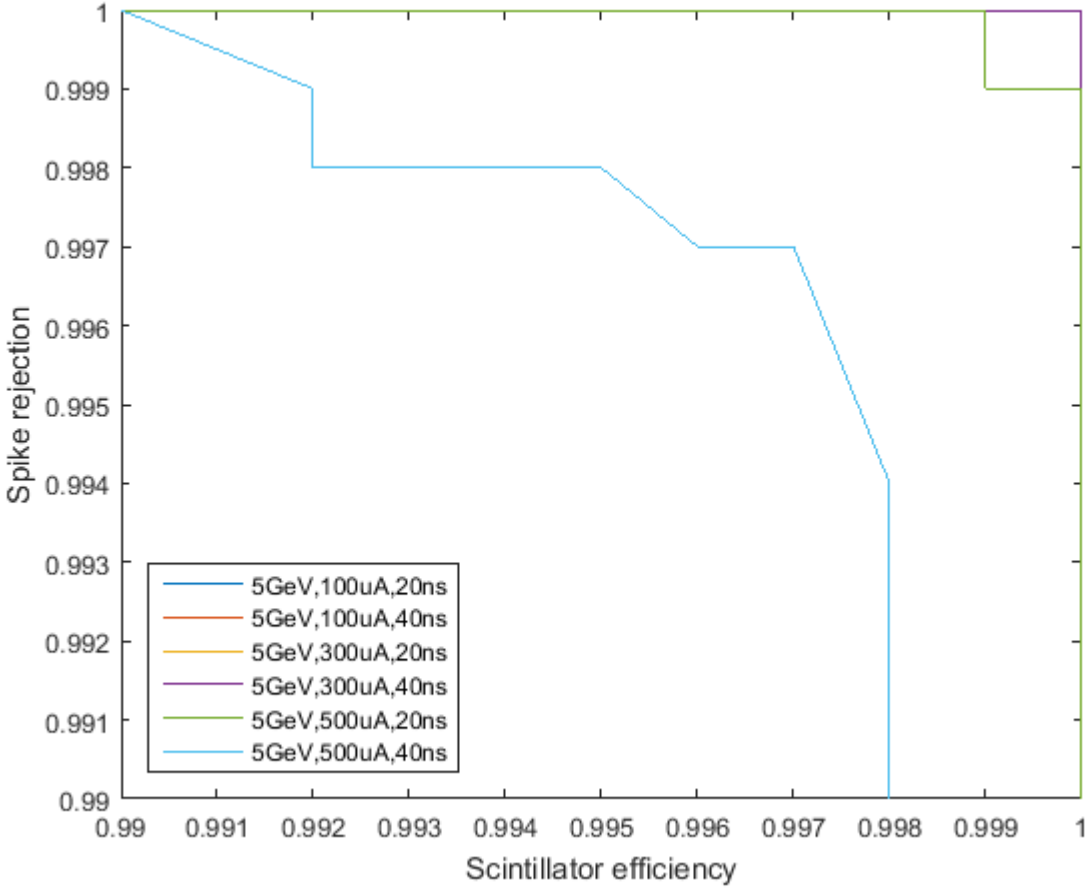


Efficiency plots 2GeV, 200uA leakage, 20ns time constant

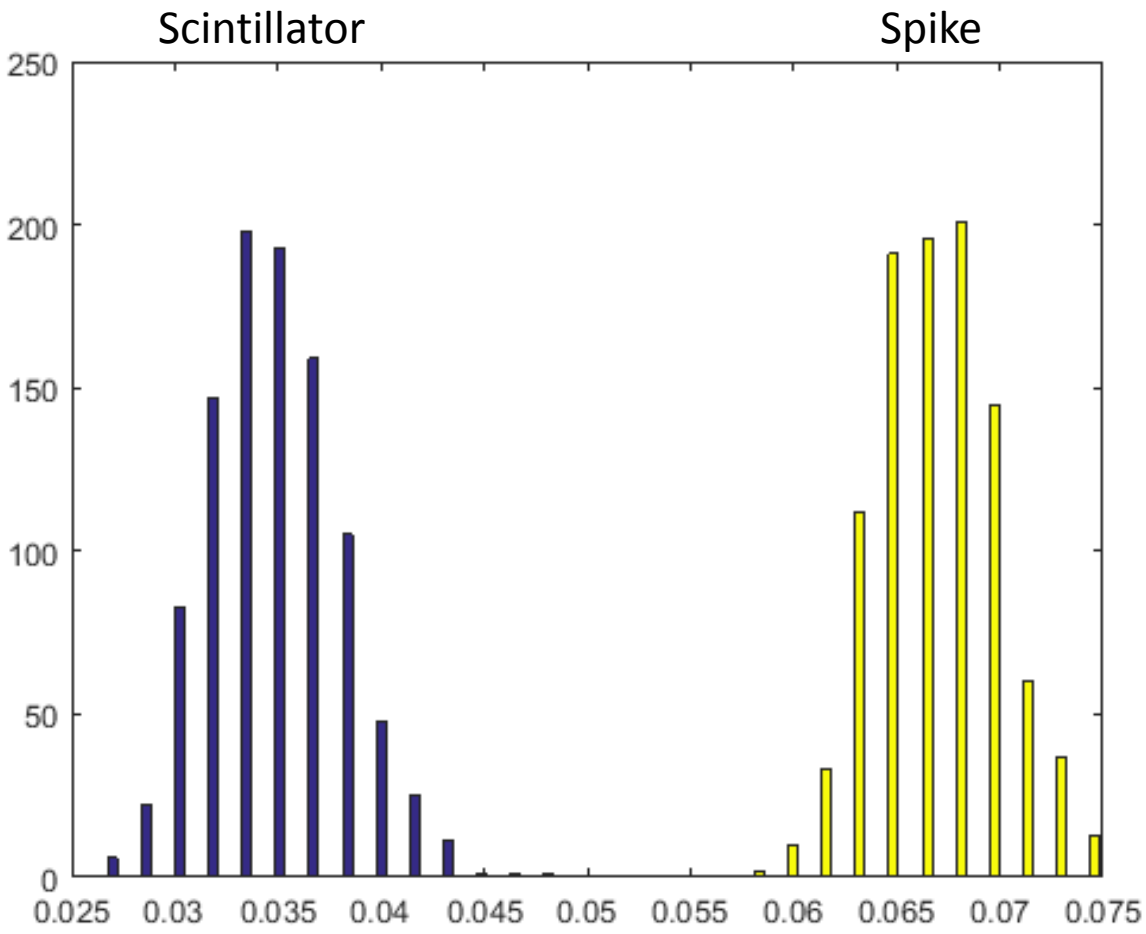


Comparison between peak hold and sampling

Efficiency plots 5GeV



Histograms of high-pass filter peak divided by shaper peak



Leakage 200uA
Shaper 40ns
180fC (5GeV scintillator)

Other design considerations

- Large signal response (so far all simulations are for small signal/noise)
- Linearity of shaper peak and consistency of shaper rising edges
- Choice between peak-hold and sampling
- External power supply factors (mixed rail, local regulation?)
- ADC voltage range and functionality of the fourth ADC analogue input
  do we keep the three gain ranges?
- Digital control - extended functionality with on-chip RC components
  to trim time constants

Conclusions and next steps [from March 2016]

- Spike discrimination can be implemented with a small amount of additional circuitry, retaining the existing pre-amp/ shaper architecture
- Simulations have not included any optimisation of the MGPA or fine-tuning of filter time constants
- Large-signal response needs to be studied, with adjustments where necessary to the existing circuits
- Option of thin-oxide conversion can be considered, if the preference is to avoid a mixed power supply (2.5/1.2V).

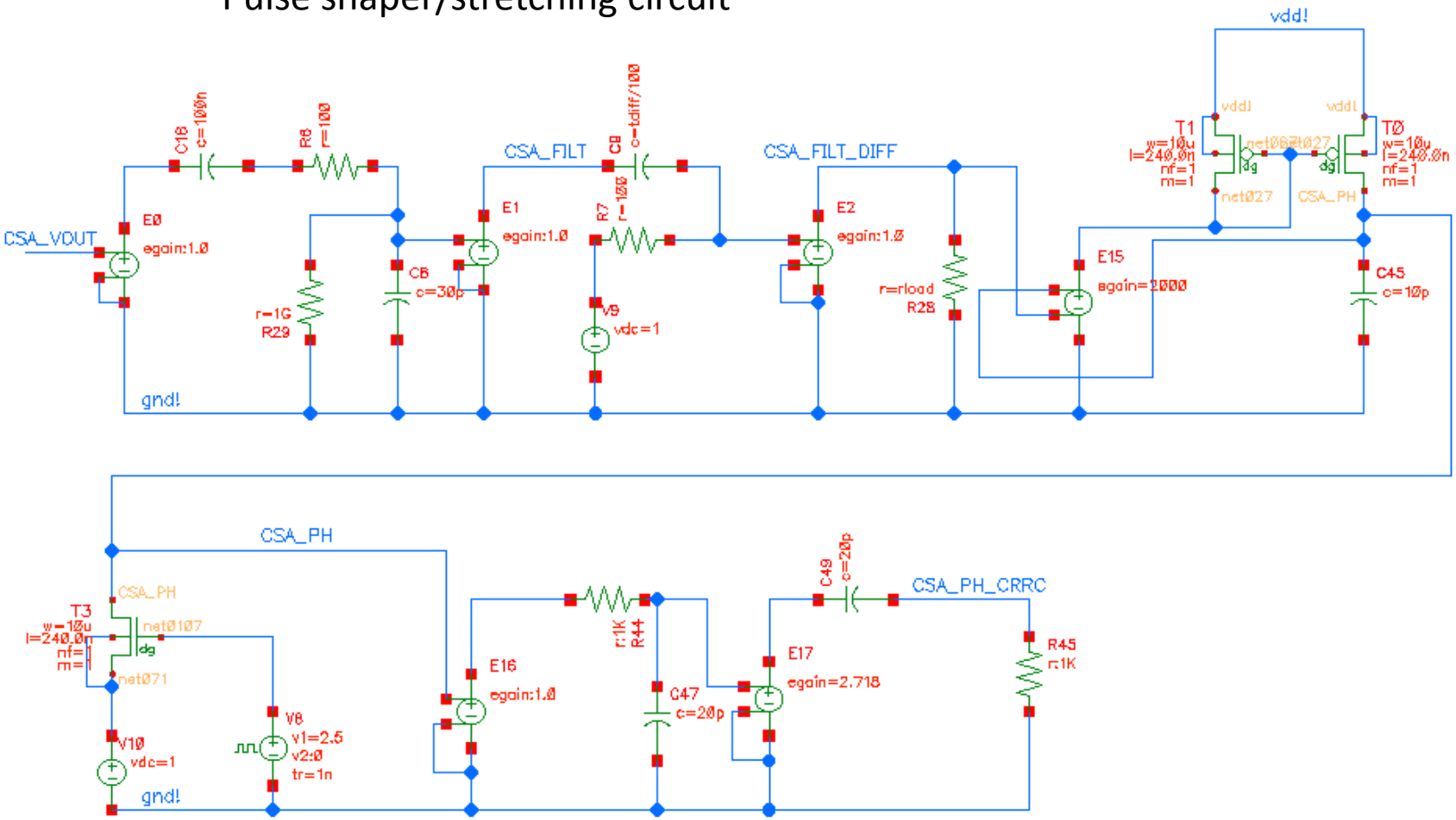
Additional analysis for statistical timing variations

- Previous plots relied on a mathematical peak function or sampling at a predetermined exact time.

- The differentiated waveforms are fast compared to the proposed 80MS/s sample rate, so cannot be reliably captured

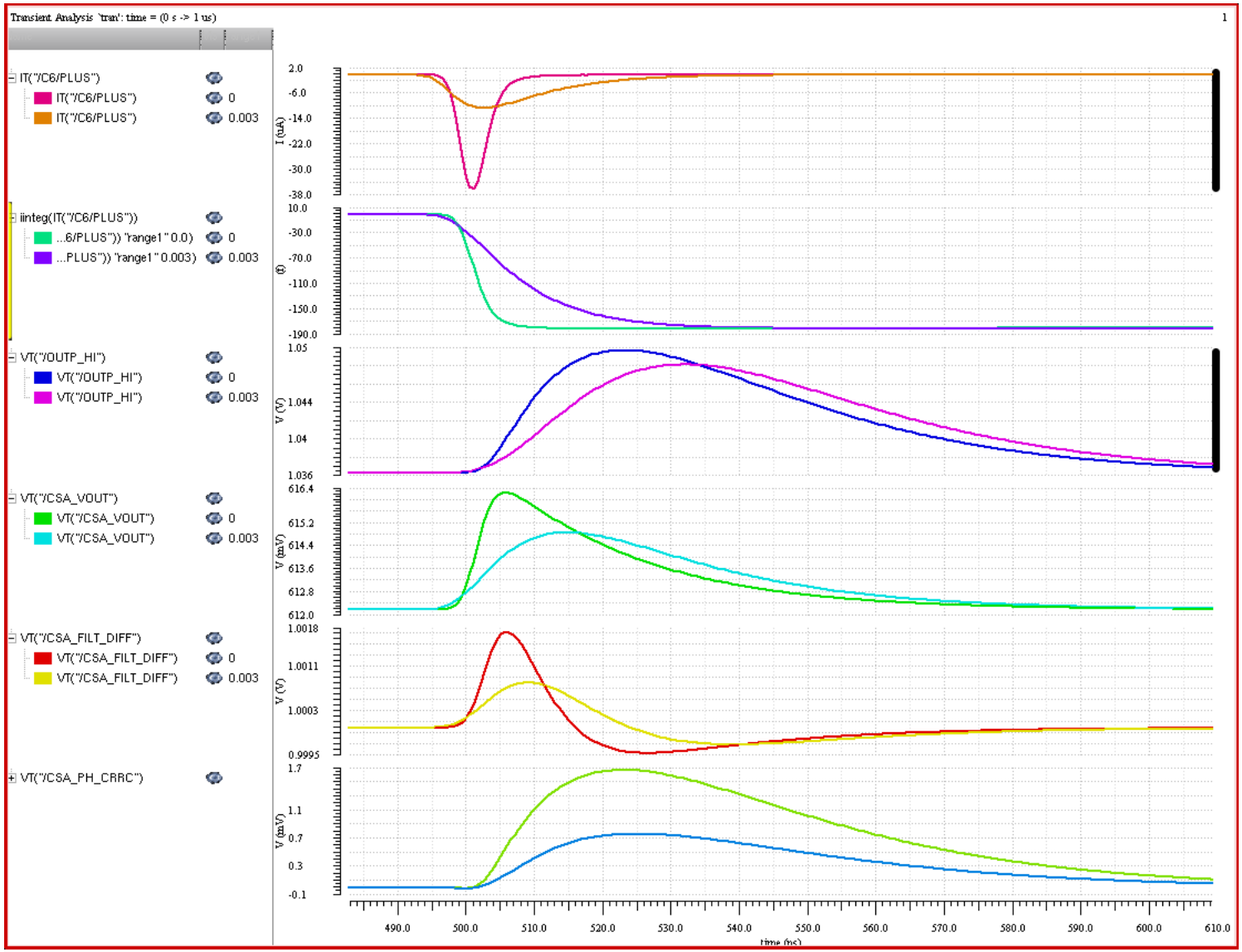
- The timing of spikes is not predictable, so there needs to be circuit to provide a pulse-stretching function, without excessive dead time

Pulse shaper/stretching circuit



Preliminary design - pulsed reset to be replaced by baseline restoration

Waveforms for spike/scintillator currents with differentiator/stretcher output



input current
spike/scintillator

current integral
(180fC=5GeV)

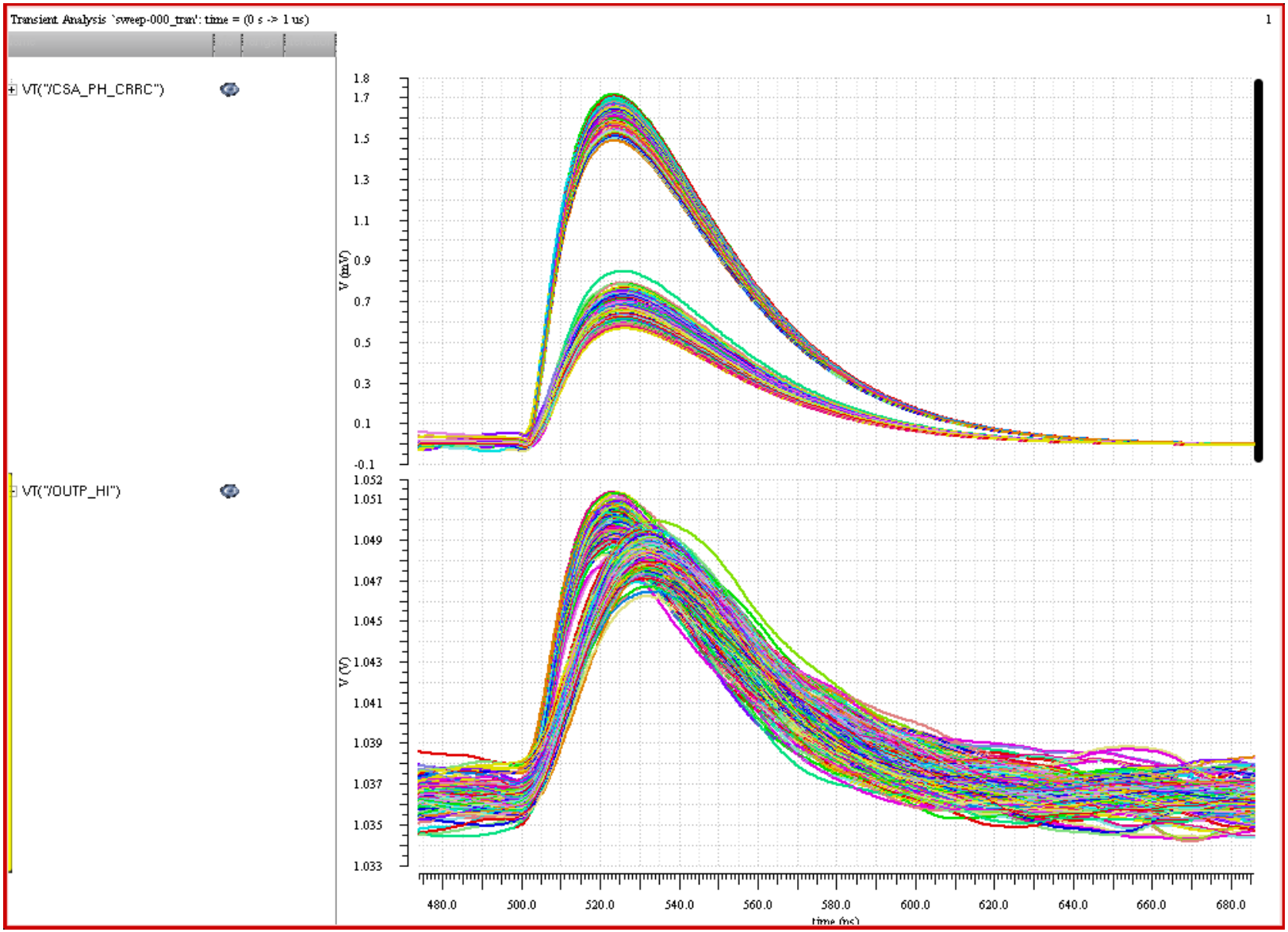
shaped
output

preamp
output

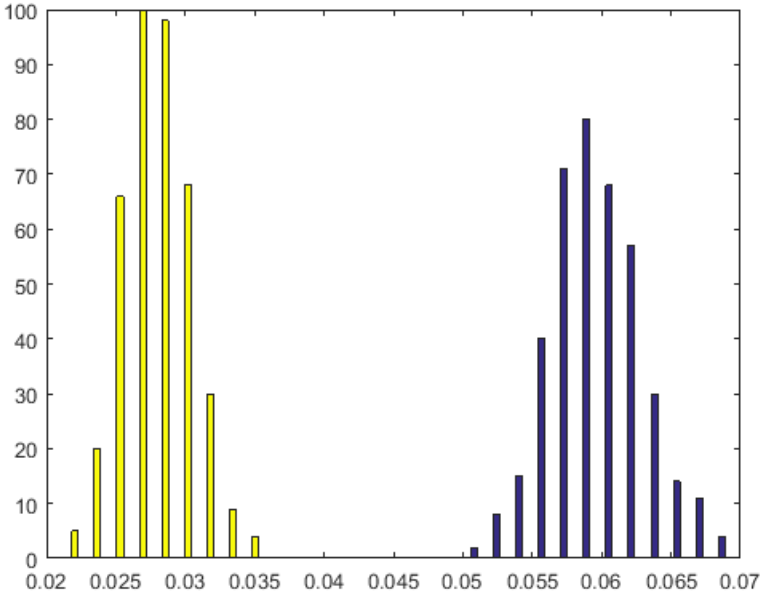
differentiated
output

pulse stretcher
(peak hold+CRRC)

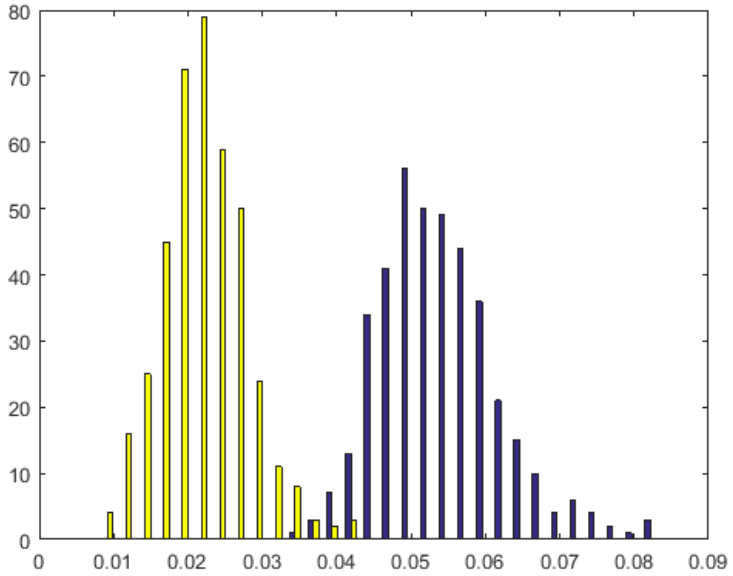
Differentiated/stretched pulse (top) with shaper output



Scintillator Spike



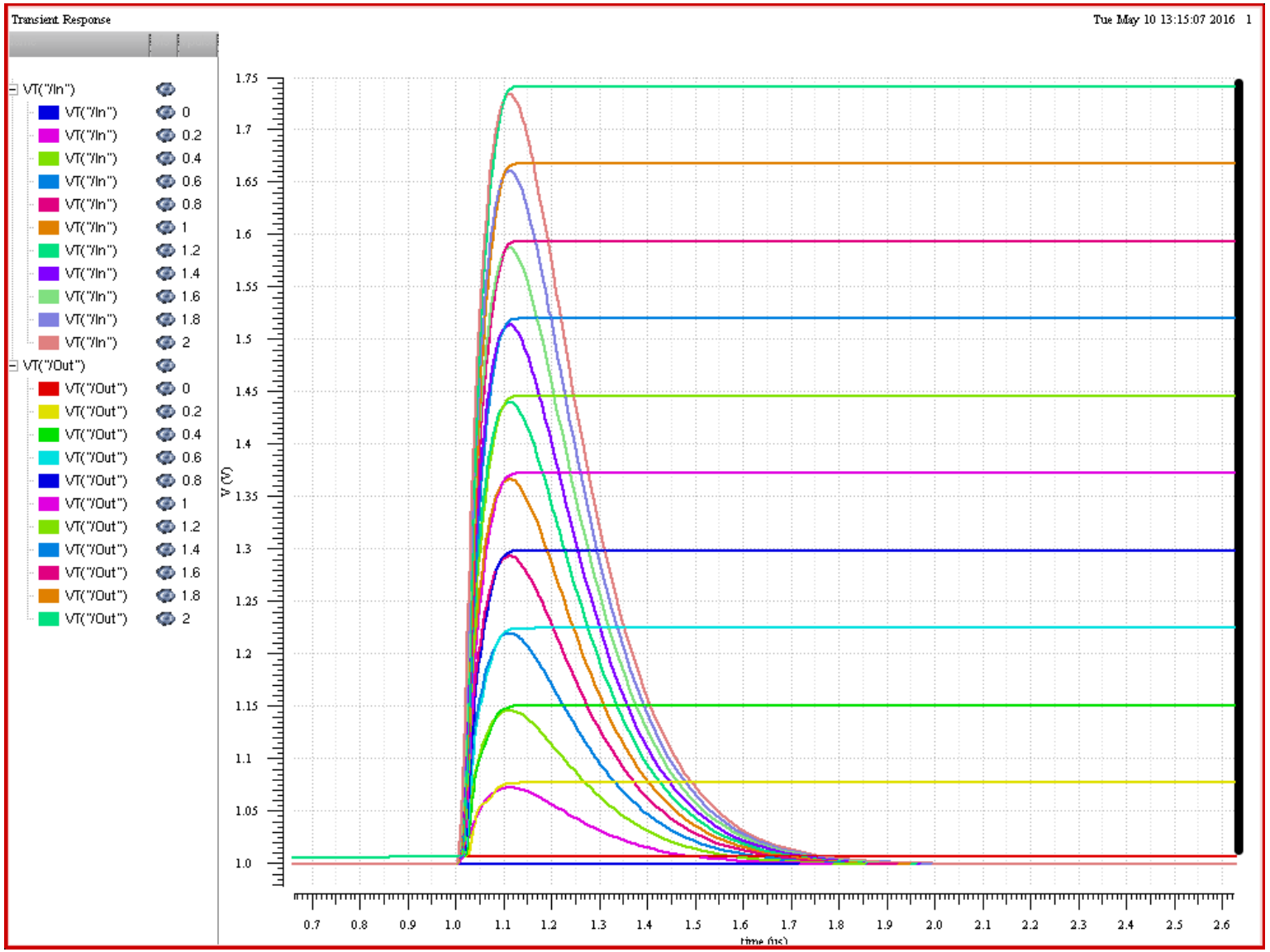
5GeV ratio of differentiated/stretched pulse to shaper output



2GeV ratio of differentiated/stretched pulse to shaper output

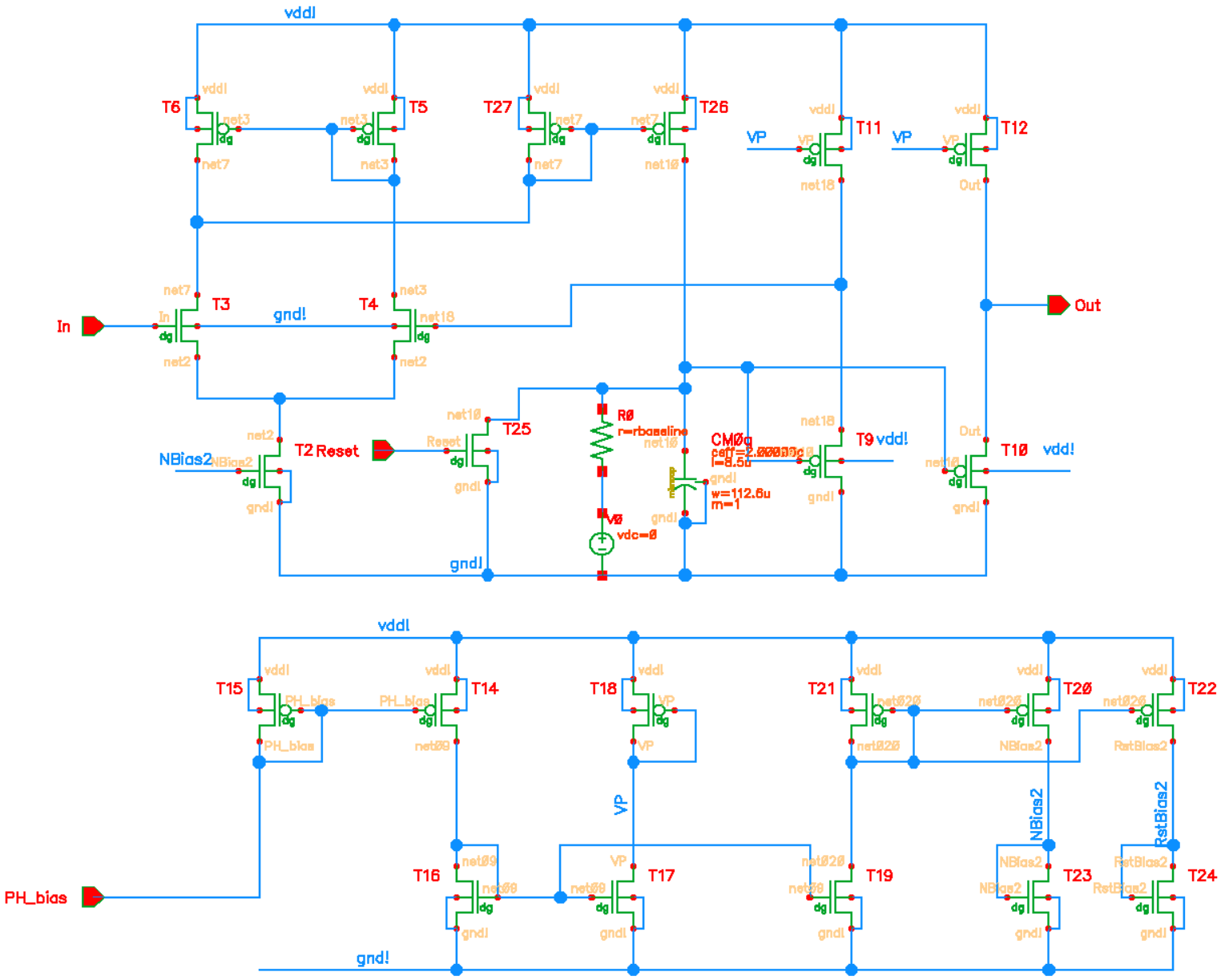
Results assume optimal sample points (at the peaks of the noise-free waveforms). However, pulses are wide compared to the 12.5ns sample interval, so at least one sample will be close to the peak.

Transistor level peak hold (without reset)

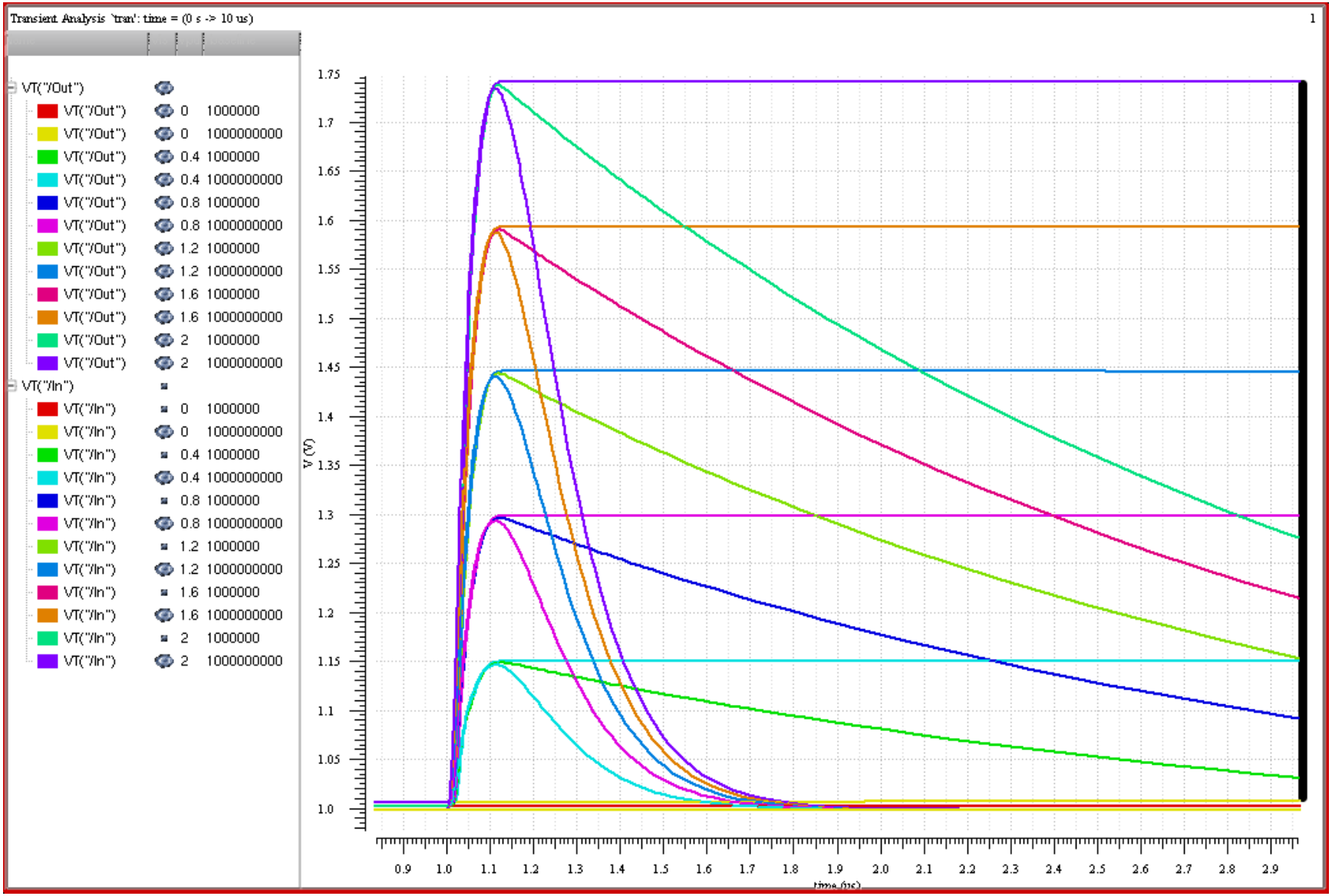


Design based on slow shaper/PH : not yet optimised for speed

Peak hold circuit, with baseline restoration resistor



Peak hold with baseline restoration resistor



Further work:

- Optimisation for peak hold speed and small signal response
- Inclusion of fast peak hold filtration for CR-RC pulse shape
- Replacement of all mathematical blocks by real circuits, including thin-oxide designs if necessary
- Check that random sample timing does not affect the amplitude accuracy too much - if necessary slow down the timing to allow more 12.5ns samples over the shaped/stretched pulses (the spike discrimination is likely to be less clear-cut with full transistor level blocks).
- Check the recovery of the peak hold with pile-up signals and statistical spreads of pulse amplitude/timing.

Conclusion:

- Simulations show clean spike/scintillator discrimination is achievable at 5GeV with waveforms slow enough for 80MS/s sampling, based on an extended MGPA design