Session Program

11–13 May 2016

CMS ECAL VFE phase II upgrade workshop

VFE ASIC Design

CEA-Saclay INSTN, 112

Thursday 12 May

14:00

VFE ASIC Design

Session | **Location:** CEA-Saclay INSTN, 112 | **Convener:** Marc Dejardin

14:00–15:00 **VFE ASIC technical requirements**

Speaker
Marc Dejardin

15:00–15:40 **TIA**

Speaker
Pascal Baron

15:40–16:20 **ADC requirements and plans**

Speaker
Joao Varela

16:20–16:50 **Coffee/discussion**

16:50–17:30 **QIE**

Speaker
Jim Hirschauer

17:30–18:00 **Discussion**

18:00