VFE - up to TDR

- **Current high-priority task: investigate architectures for readout ASIC**
  - ***Focus on:***
    - *Limiting effects of APD noise increase, and improving out-of-time pileup rejection*
    - *Anomalous signal rejection*
    - *Ability to provide precise timing measurement for high energy photons*
  - ***Three reports due by summer 2016 (for CMS internal review):***
    - *Detailed technical appraisal of architecture options (engineering study)*
    - *Physics performance of architecture options (simulations study)*
    - *Ultimate timing performance of lead tungstate crystals and physics benefit of precise timing (test beam + simulations study)*
    - *Milestone:* ***Q2 2016: Draft initial VFE ASIC specifications***
  - ***Progress expected by TDR***
    - *Milestone:* ***Q4 2016: VFE specifications defined and architecture chosen***
    - *Detailed simulations results of expected performance*
    - *First iteration of ASIC design commenced, MPW expected* ***end-2017***
    - *Proof of principle tests (using discrete components) completed*

ADC/LVR/VFE board

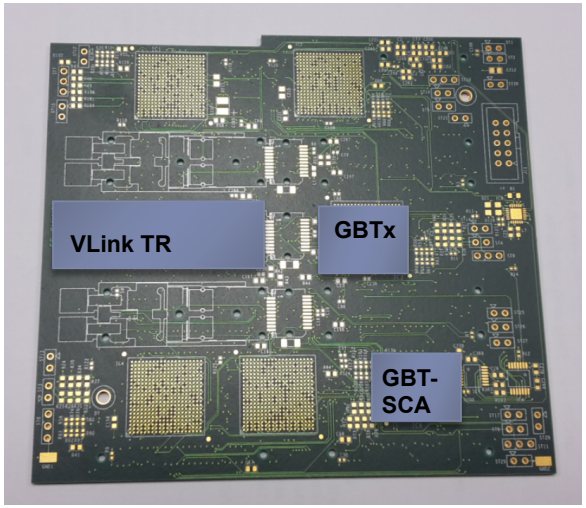
- **ADC:**
  - Now: Investigating use of commercial ADC core
    - *This year: **evaluate performance** of currently available ASICs*
      - ***Specify modifications** needed to ensure radiation tolerance at HL-LHC by **end-2016** [radiation in EB, up to: 1 Mrad, 2.4x10^{14} n/cm for 3000fb^{-1}]*
    - *First prototype ASIC available by **end-2017***
- **LVR:**
  - Now: evaluating performance of proof-of-principle demonstrator
    - *Using CERN-developed FEAST DC/DC convertors*
    - *Promising results from initial tests @ CERN. Now preparing test @ 3.8T at U. Virginia in June. Results expected by end of 2016. Feed back results into VFE and ASIC design*
    - *First prototype board expected **end-2017***
- **VFE board:**
  - *Design will commence once VFE ASIC specifications defined (**end 2016**)*
  - *First board will become available in **Q2 2018** when first prototype ASICs are ready*
  - *Design will be qualified with series of bench tests and test beam exposures up to EDR*

VFE board - from TDR to EDR

- Two iterations of VFE ASIC foreseen
  - ***1st iteration: Q1 2018***
    - *integrate into new VFE board, with 1st generation ADC ASIC*
    - *Test beam appraisal of new VFE board with new ASICs in 2018*
  - ***2nd iteration: Q1 2019***
    - *Key milestone in Q3 2019:* ***Full validation of prototype VFE board (with new ASICS) + new LVR board*** *- bench test and test beam evaluation campaigns*
    - *Sufficient level of testing to validate overall concept in time for EDR.*
- From EDR to ESR
  - ***Accelerated ageing and radiation exposure of all 3 boards during 2020***
  - ***Test beam verification of all components in spare SM by end-2020***
    - *Assess readiness for production*

FE/OD readout

- **FE board:**
  - Now: Investigating performance of demonstrator
    - ***Gain experience with new CERN-developed chipsets. First results expected this Summer***
    - *Prototype uses: GBTx (data transfer), GBT-SCA (clock, control). Will test:*
      - ***Data transmission in streaming mode***
      - ***Ability to control legacy VFE cards***
      - ***Clock distribution (granularity and jitter)***
- **OD readout:**
  - ***Initial FE tests to be carried out using existing CMS trigger boards***
  - *OD readout specs and trigger algorithms to be developed once VFE/FE output is defined (**early 2017, for TDR**)*
  - *Commencing design studies for common back-end card and firmware R&D*



FE demonstrator PCB indicating location of VL, GBT components

FE/OD schedule to EDR

- **FE board:**
  - Series of prototypes following development of GBT, Versatile link chipsets
    - ***Final design will use 10Gb/s links for data transfer***
    - *These should become available* ***end-2018****.*
    - ***Milestone: First test of FE prototype with 10Gb/s links: Q1 2019***
- **OD readout:**
  - ***Trigger concept, OD requirements and architecture should be defined in TDR***
  - *OD prototype, using common firmware and hardware developments, should be available* ***early 2019***
  - *series of system tests, and test beam evaluations (with new prototypes of VFE,FE) should take place* ***prior to EDR (Q3 2019)***
  - ***Final validation of OD readout design: Q2 2020***

Cooling/Mechanics

- Supermodule cooling
  - ***Tasks between now and TDR***
    - *Requirements of cooling plant (once FE electronics power consumption known). By **Q1 2017***
    - *Feasibility of low-temperature operation (including supermodule cooling performance tests using spare SM). By **TDR.***
  - ***Tasks between TDR and EDR***
    - *Specification and design of cooling plant and layout of YB0 services*
- Supermodule refurbishment
  - ***Clear definition of tasks and resources by TDR***
    - *Overall schedule of work*
    - *Define requirements and layout of SM integration area at Pt5*
    - *Define infrastructure and manpower requirements*
    - *SM extraction and tooling*
  - ***Progress expected by EDR***
    - *Full definition of SM integration area, schedule, manpower and responsibilities*
    - *Enforneur design, schedule and manpower for SM extraction should be fully defined*

Reminder of overall plan

- Summer 2016: First Comprehensive review (CMS internal)
  - **Evaluate concept of VFE upgrade**
- Q3 2017: Technical Design Report (TDR)
  - **Evaluate technical specification and expected performance of VFE,FE,LVR**
  - **Evaluate feasibility of SM cooling**
  - **Evaluate trigger strategy and expected online/offline performance**
- Q3 2019: Engineering Design Report (EDR)
  - **Technical validation of VFE,FE,LVR prototypes**
- Q1 2021: Electronics Systems Review (ESR)
  - **Assess readiness for production**

VFE - up to TDR

VFE
FE
LVR
OD electronics
Cooling/Mech
Simulations
Reviews

Q2 2016	VFE.LL.2016.1: Report on test beam evaluation of $PbWO_4$ ultimate timing
Q2 2016	VFE.LL.2016.2: Report on simulation studies of VFE ASIC performance
Q2 2016	VFE.LL.2016.3: Report on technical feasibility of VFE ASIC architecture options
Q2 2016	**VFE.HL.2016.1: Draft initial VFE ASIC specifications**
Q2 2016	VFE.LL.2016.4: Define feasible ADC ASIC core
Q2 2016	REV.LL.2016.1: First Comprehensive Review
Q4 2016	VFE.LL.2016.5: Complete evaluation of ADC ASIC using test samples
Q4 2016	**VFE.HL.2016.2: Define final VFE ASIC specifications - commence design**
Q4 2016	VFE.LL.2016.6: Define ADC ASIC specs and commence design
Q4 2016	VFE.LL.2016.7: Define VFE board specs and commence design
Q2 2017	VFE.LL.2017.1: Proof of principle test of key VFE ADC functionality (bench tests)
Q2 2017	REV.LL.2017.1: Second Comprehensive Review
Q3 2017	**REV.HL.2017.1: Technical Design Report**

VFE - post-TDR

VFE
FE
LVR
OD electronics
Cooling/Mech
Simulations
Reviews

Q4 2017	VFE.LL.2017.2: First prototype ADC available
Q1 2018	VFE.LL.2018.1: First prototype VFE ASIC available
Q1 2018	VFE.LL.2018.2: Start design of 2nd iteration of VFE ASIC
Q2 2018	**VFE.HL.2018.1: First prototype of VFE board available with new ASICs**
Q2 2018	REV.LL.2018.1: Third Comprehensive Review
Q4 2018	VFE.LL.2018.3: Test beam appraisal of prototype VFE board
Q1 2019	VFE.LL.2019.1: Second iteration of VFE ASIC available
Q1 2019	[VFE.LL.2019.2: Second iteration of ADC ASIC available - if required]
Q2 2019	REV.LL.2019.1: Fourth Comprehensive Review
Q3 2019	**VFE.HL.2019.1: Validation of overall concept (VFE+FE+LVR)**
Q3 2019	**REV.HL.2019.1: Engineering Design Report**
Q2 2020	**VFE.HL.2020.1: Accelerated ageing and radiation exposure of all 3 boards**
Q4 2020	**VFE.HL.2020.2: Test-beam verification of all components in SM, at lower temperature.**
Q1 2021	**REV.HL.2021.1: Electronics Systems Review**

Spike rate estimates

- Use scaling laws to estimate spike rates for 2025+ running:
  - **Measured in 2010 for E_T> 20 GeV: 1 spike in ~ 6000 events at 7 TeV**

Spikes scale:

linearly with PU

logarithmically with c.m. energy

- **<u>2025 conditions:</u>** 14 TeV, 140 PU, 25ns bunch spacing:
  - Spike rate = 1/6000 * ln(14)/ln(7) * 140 * 40x10^6 = **<u>1.2 MHz</u>**
    - assume L1 spike killing effic = 96%* → L1 spike rate = **50kHz**
    - if L1 spike killing effic = 99.9% → L1 spike rate = **1.2kHz**

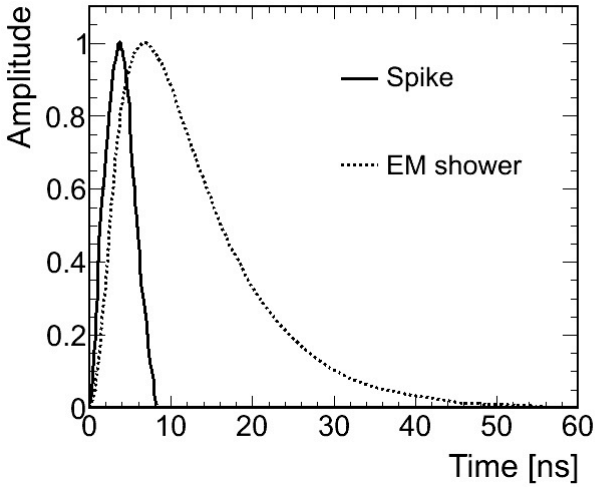
* measured in Run 1

<u>Spikes will be a major contributor to L1 rate if no additional mitigation is performed</u>

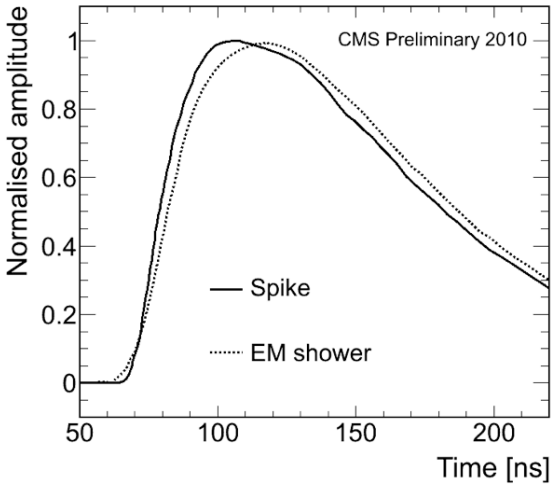
<u>Spike killing effic at HL-LHC should be better than 99.5% to keep L1 fake rate below 10%</u>
<u>(assuming bandwidth for lowest unprescaled EG trigger ~50kHz)</u>

Spike pulse shapes

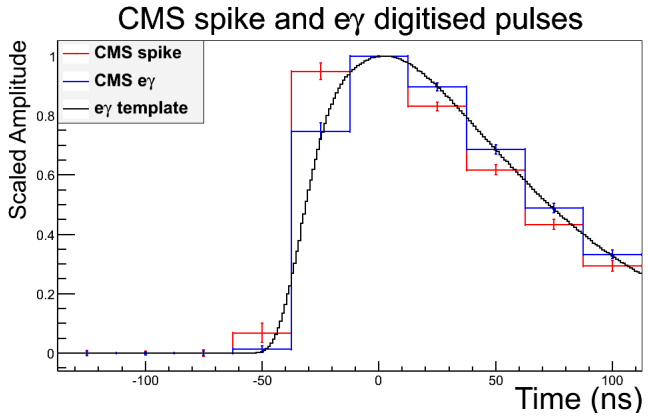
Analogue pulse, before shaping



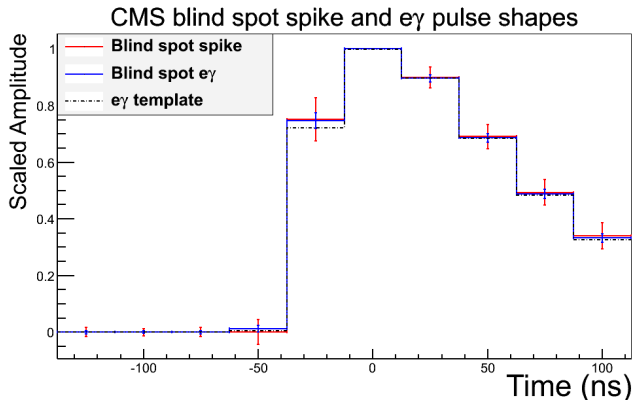
Analogue pulse, after CR-RC shaping (τ=43ns)



Digital pulse, 10 samples



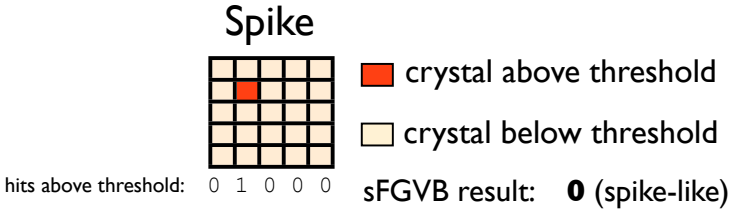
Digital pulse, 10 samples, time shifted



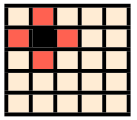
Much better discrimination with analogue (or oversampled) pulse. No “blind spots”

Options for spike killing

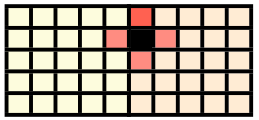
- **Do nothing: use current sFGVB algorithm**
  - **coarse granularity, sensitive to PU, noise, TT boundaries**



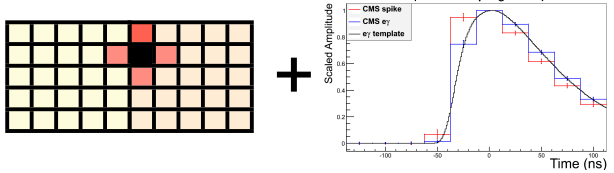
- **Replace FE, compute Swiss-cross on-detector**
  - **finer granularity, still sensitive to PU, noise and TT boundaries**



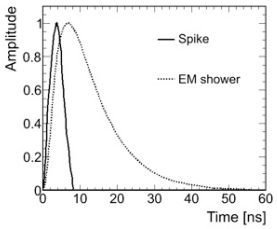
- **Replace FE, compute Swiss-cross off-detector**
  - **finer granularity, still sensitive to PU, noise, no TT boundaries**



- **Replace FE, compute Swiss-cross off-detector + use timing (offline algo)**
  - **finer granularity, less sensitive to PU, noise, no TT boundaries**

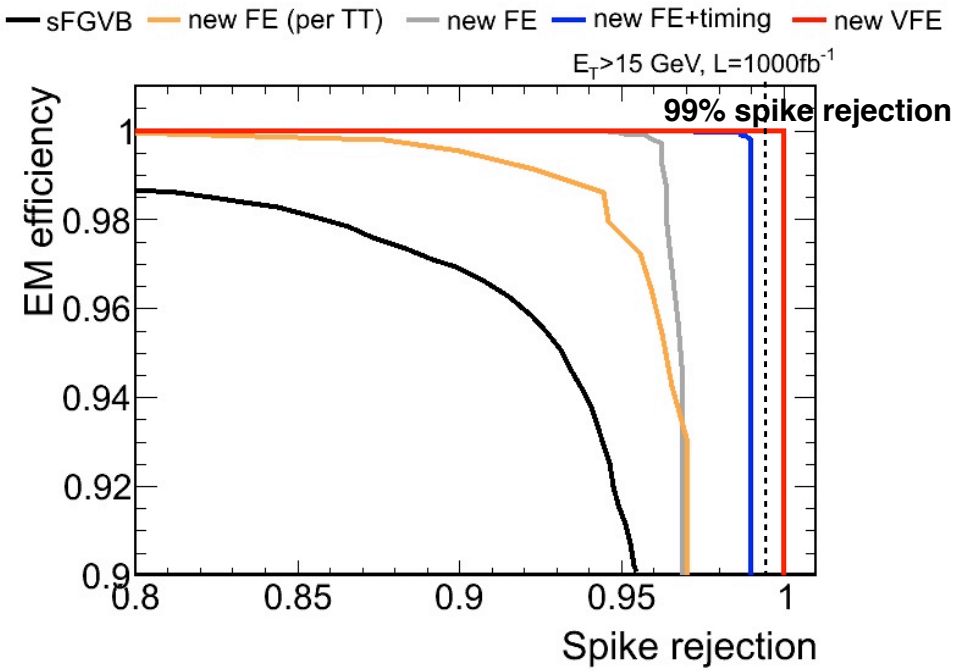


- **Replace VFE, discriminate analogue shape**
  - **large shape difference between pulses, much less sensitive to PU, noise, no TT boundaries**

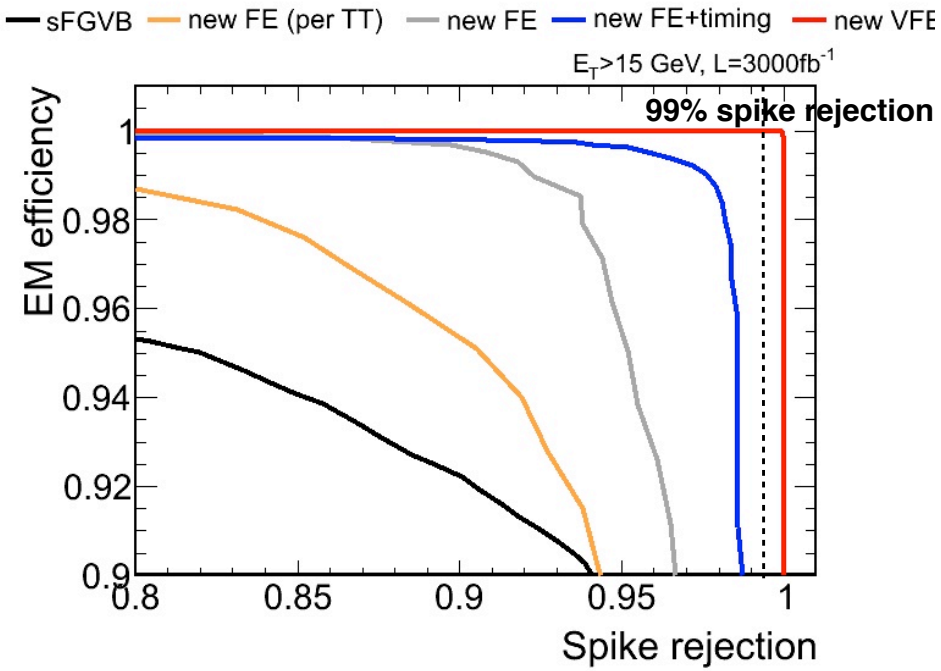


Spike killing performance

1000 fb^{-1}



3000 fb^{-1}



Spike efficiency vs EM efficiency curves for various algorithms

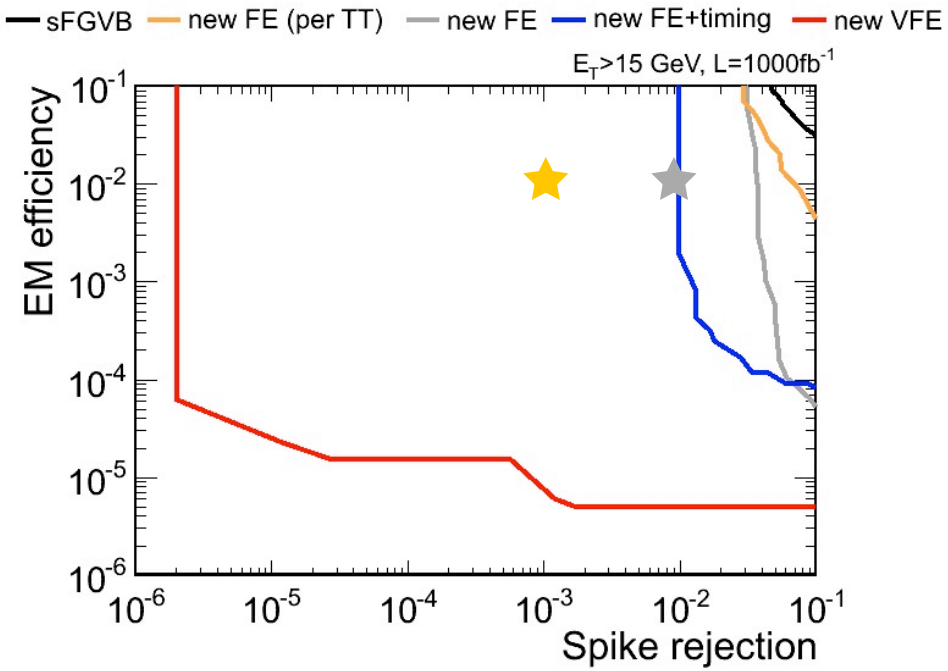
Black: Current algo →unacceptable performance at HL-LHC

Blue: offline algorithm (best you can do only if FE card is replaced) → better, but does not reach required spike rejection performance

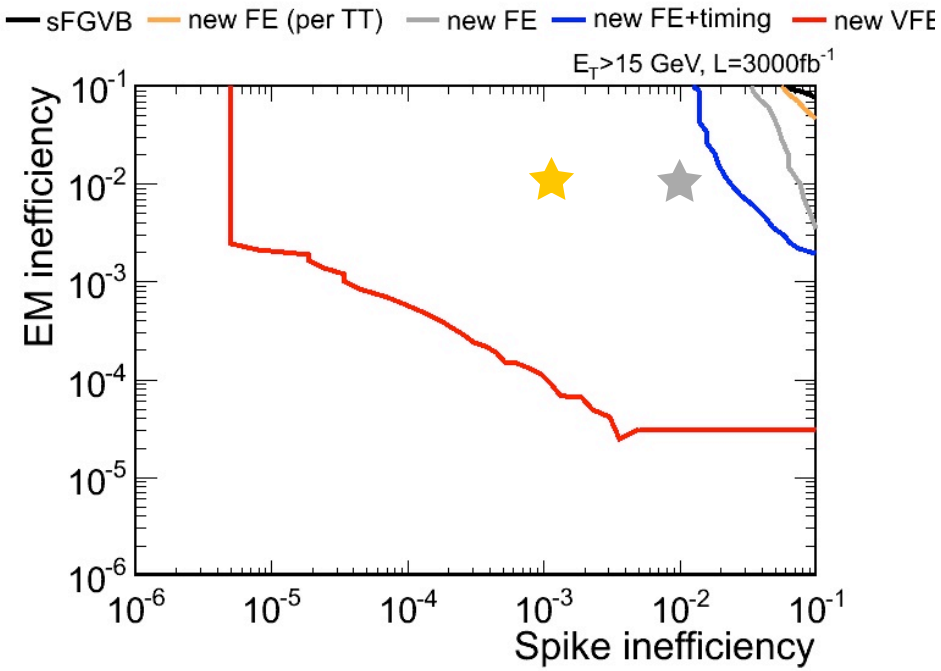
Red: use analogue pulse shape in new VFE → spike problem reduced to negligible level

Spike killing performance - log scale

1000 fb^{-1}



3000 fb^{-1}



Spike inefficiency vs EM inefficiency on log scale

Stars represent required performance:

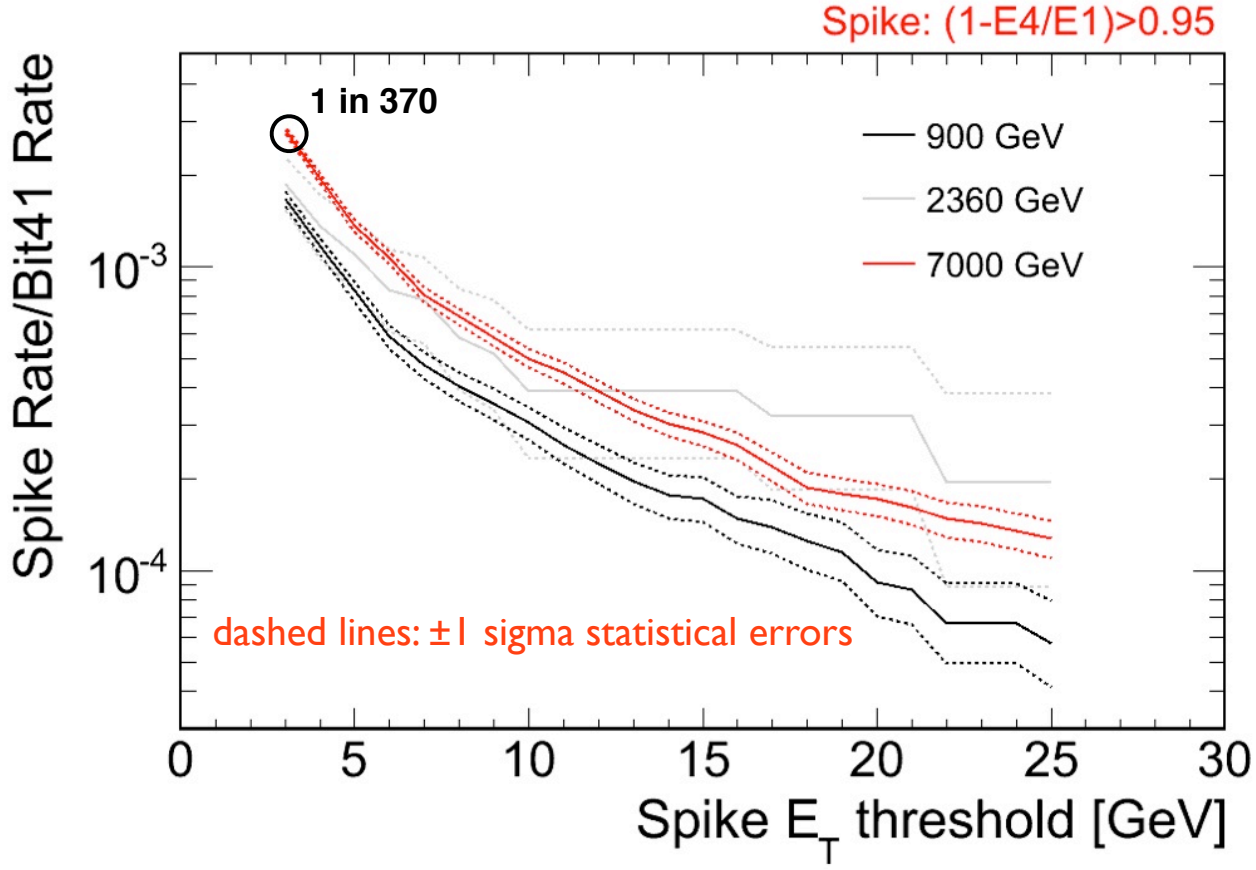
SILVER: 99% spike rejection, 99% EM efficiency

GOLD: 99.9% spike rejection, 99% EM efficiency

Only the red lines (VFE is replaced) provide the needed performance

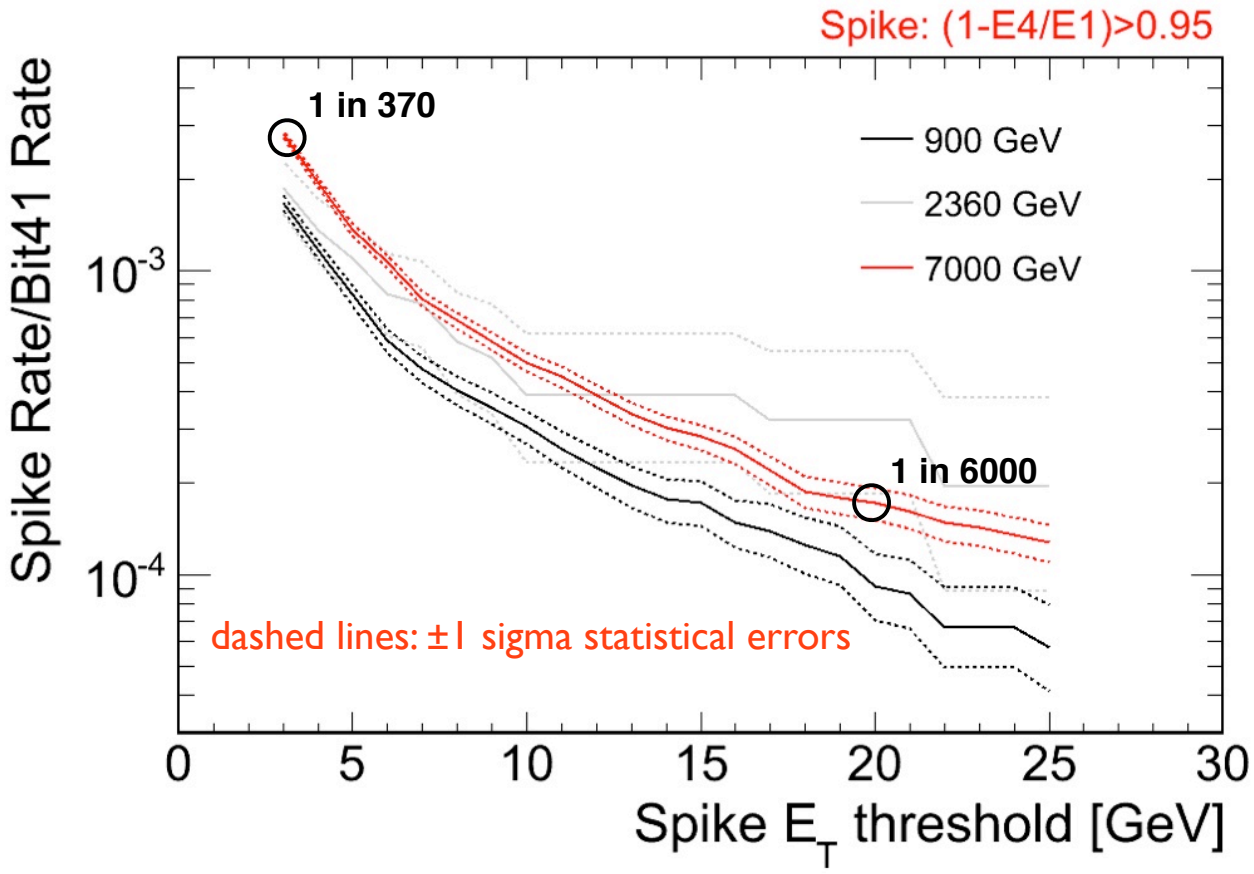
Spike rate/minbias event vs E_T

How to predict rates at higher lumi?



- This plot produced from 2009-2010 data
  - source of the canonical: *"1 spike with E_T>3 GeV in every 370 minimum bias events at √s=7 TeV"*

Spike rate/minbias event vs E_T



- What happens at higher thresholds?
  - E_T> 3 GeV: **1 spike in 370 events at 7 TeV**
  - E_T> 20 GeV: **1 spike in ~ 6000 events at 7 TeV**