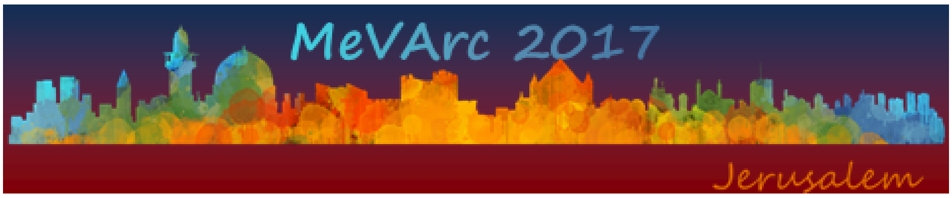

Contribution ID: **38**

Type: **oral**

Dielectric Surface Breakdown in Sub-100 nm Metal-Insulator-Metal Fins with Exposed SiOx and Si3N4 Sidewalls

Wednesday, 22 March 2017 16:30 (30 minutes)

The study of surface flashover behavior in nanoscale dielectrics has broad application in nano- and micro-fabricated on-chip electronics such as energy converters, logic/memory, mass spectrometers, field emission devices, and compact accelerators. Most microscale devices incorporate planar dielectric architectures (e.g. gate oxides in transistors) without exposed surfaces. Therefore, relatively few studies have evaluated flashover in 3D nanoscale electronics with exposed surfaces. Here, we present an evaluation of dielectric breakdown across nanoscale width (<100nm) metal-insulator-metal (MIM) devices with vacuum-facing SiOx and Si3N4 sidewalls fabricated using standard microfabrication techniques. We evaluated the effects of dielectric material, contact metal, exposed dielectric surface area, and surface treatment on the breakdown strength of nanoscale dielectric surfaces. Electrical measurements indicate that optimizing dielectric and metal geometry, dielectric deposition parameters, and microfabrication-compatible surface cleaning procedure yields surface breakdown thresholds up to 0.30 V/nm in MIM devices consisting of up to thousands of exposed nanoscale dielectric sidewalls. Furthermore, we present electron microscopy studies that suggest breakdown modes unique to nanoscale devices. Our results inform techniques to sustain high surface fields on nanoscale dielectrics, which is imperative for reliability and performance of compact vacuum electronic devices, especially in light of the recent trend toward nano- and microfabricated vacuum electronics.

Type of contribution

Oral

session

Applications - materials and devices

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