CMS HG-CAL

FEE 2016 - Krakow

Damien Thienpont on behalf of the HGC collaboration

June 3, 2016

Organization for Micro-Electronics desiGn and Applications

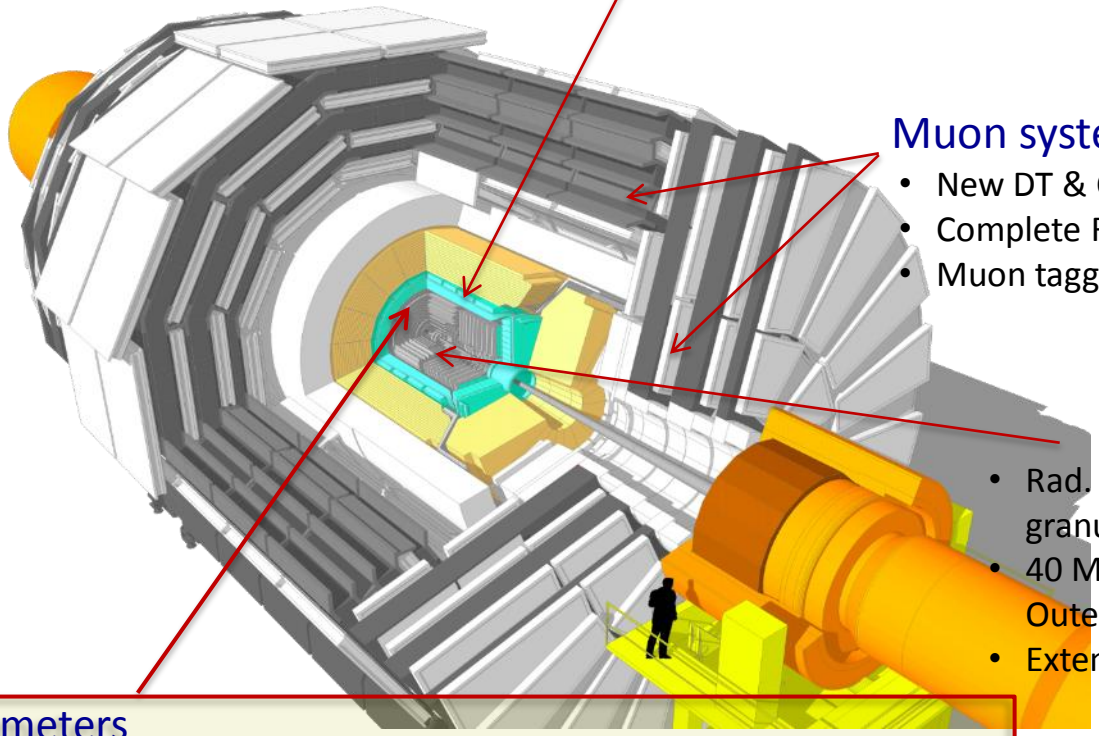
CMS Phase-II upgrades

Trigger/HLT/DAQ

- Track information in Trigger (hardware)
- Trigger latency 12.5 μs - output rate 750 kHz
- HLT output 7.5 kHz

Barrel EM calorimeter

- New FE/BE electronics with improved time resolution
- Lower operating temperature (8∘)



Muon systems

- New DT & CSC FE/BE electronics
- Complete RPC coverage $1.6 < \eta < 2.4$
- Muon tagging $2.4 < \eta < 3$

New Tracker

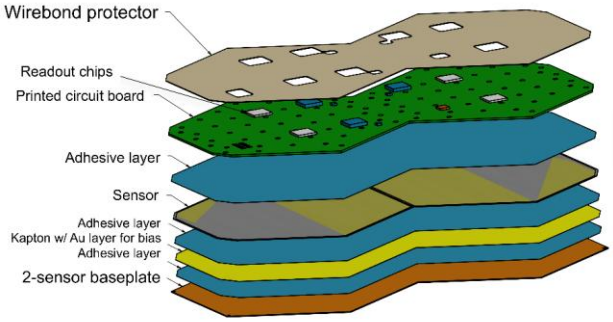
- Rad. tolerant - increased granularity - lighter
- 40 MHz selective readout in Outer Tracker for Trigger
- Extended coverage to $\eta \simeq 3.8$

New Endcap Calorimeters

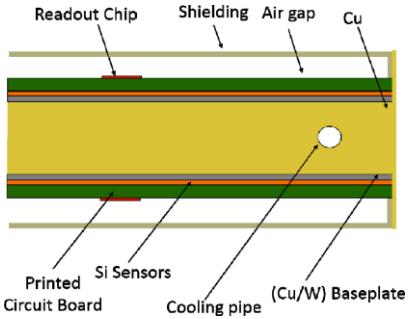
- Rad. tolerant
- High Granularity: increased transverse and longitudinal segmentation, needed to mitigate pileup effects to select events with a hard scatter process at L1-Trigger and to identify the associated vertex and particles
- precise timing capability: further mitigation of pileup effects

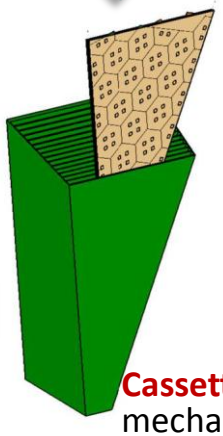
Modules, Cassettes and Mechanics (technical proposal)

Modules
With 2x 6 - 8" Hexagonal Si sensors, PCB, FE chip, on W/Cu baseplate

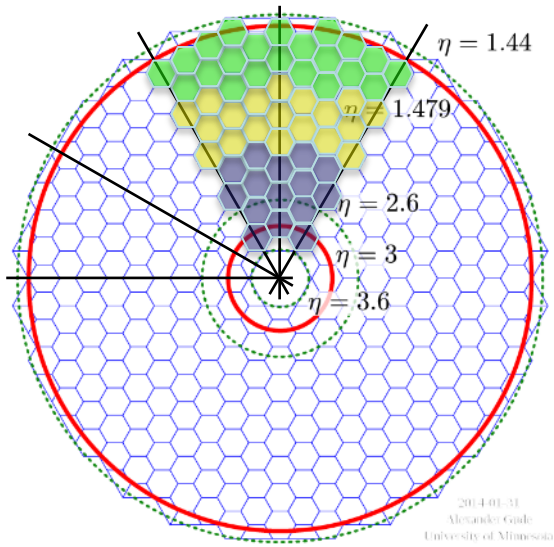


Modules mounted on Cu Cooling plate with embedded pipe
=> **Cassettes**

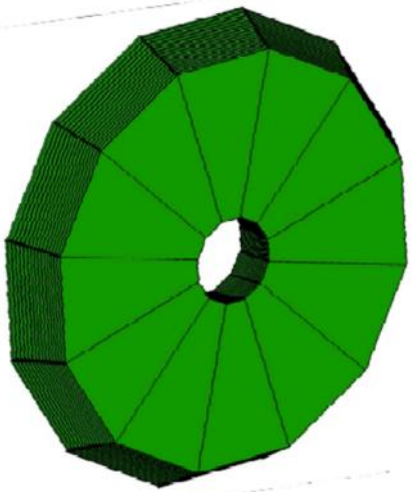




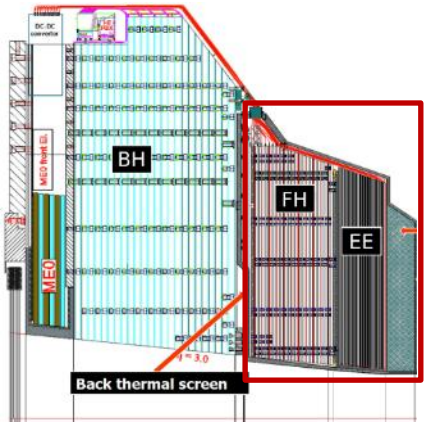
Cassette inserted in mechanical structure (containing absorber)



3 sensor active thicknesses 100-200-300 µm
0.5(1) cm^2 pads for 100(200/300) µm



12 **Cassettes** mounted together to form the **ECAL (EE)** **and** **Front HCal (FH)**



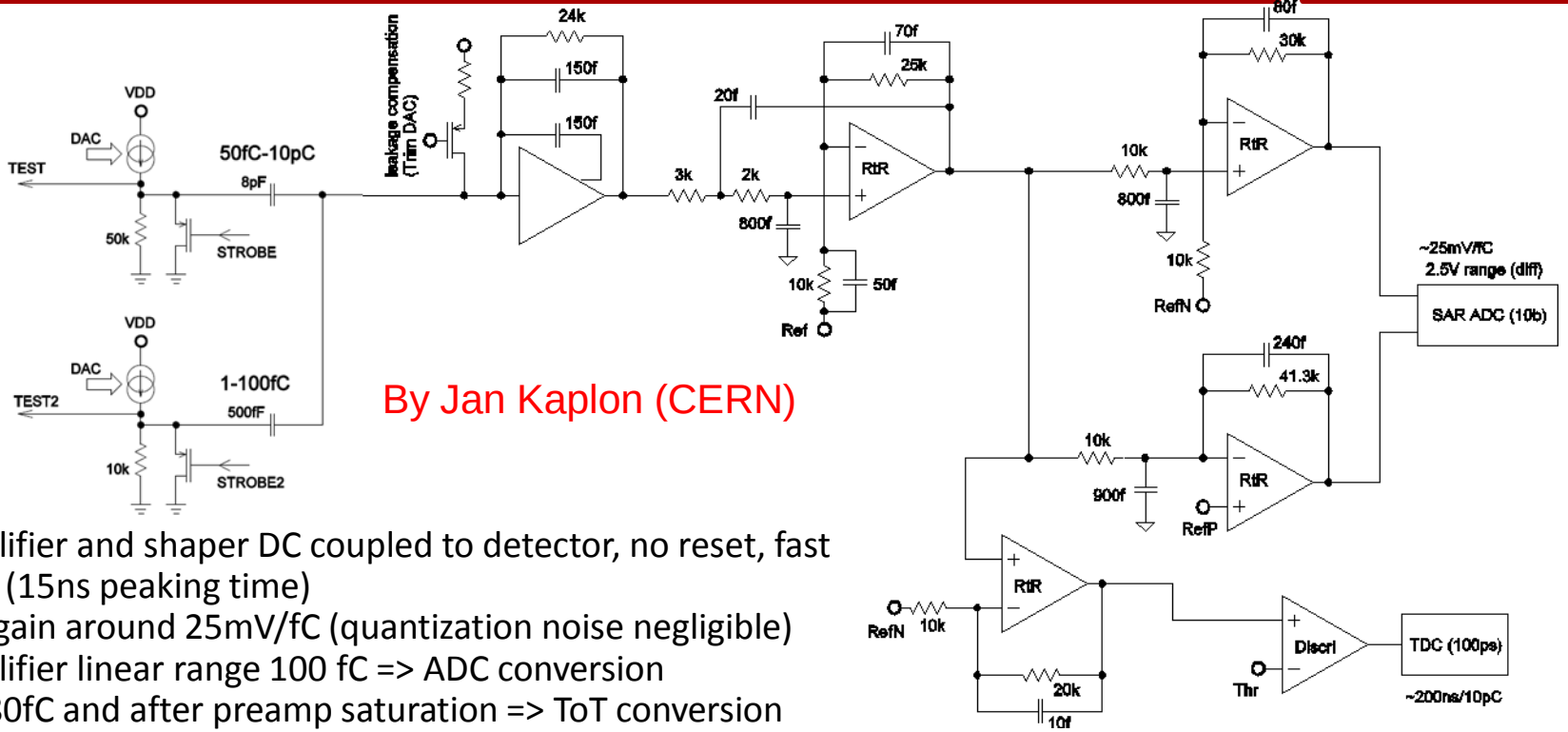
Replaced EndCap (maintained at -30°C

Challenges for electronics

- Reading out full data or largest possible sub-set at 40 MHz for L1-Trigger

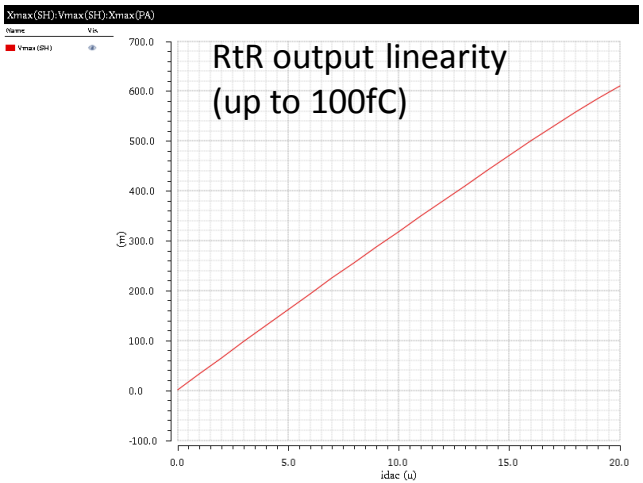
- Stringent requirements for Front-End Electronics
  - Low power (~5 mW for analogue channel), ~ 92 000 FE chips, 130 nm or 65 nm
  - Low noise: <2000 e- (0,32 fC)
  - MIP: 7k – 20k e- (1 – 3 fC)
  - Dynamic range up to 3000 MIP (10 pC), 17 bits required with 0,1 fC resolution
  - Detector capacitance 40-60pF, detector leakage: up to 10 µA
  - System on chip (charge, time, digitization, data and trigger processing, on-chip zero supress, …)
  - High speed readout (5-10 Gb/s)

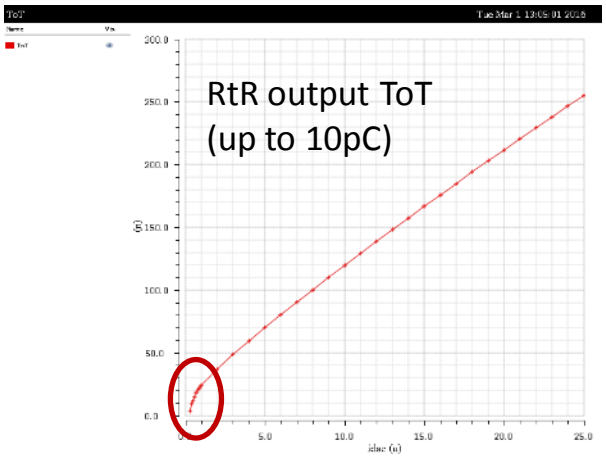
Baseline architecture (Technical Proposal)

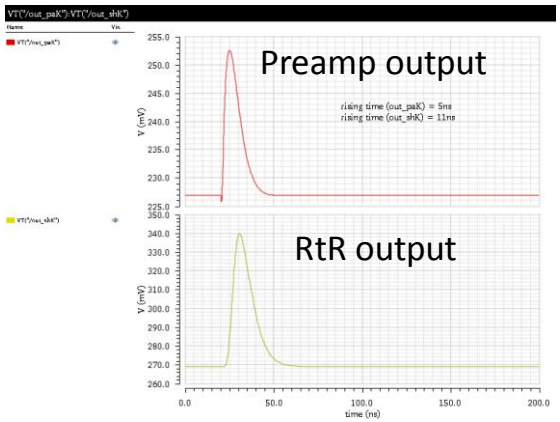


By Jan Kaplon (CERN)

- Preamplifier and shaper DC coupled to detector, no reset, fast shaping (15ns peaking time)
- Analog gain around 25mV/fC (quantization noise negligible)
- Preamplifier linear range 100 fC => ADC conversion
- Above 80fC and after preamp saturation => ToT conversion







Milestones for electronics

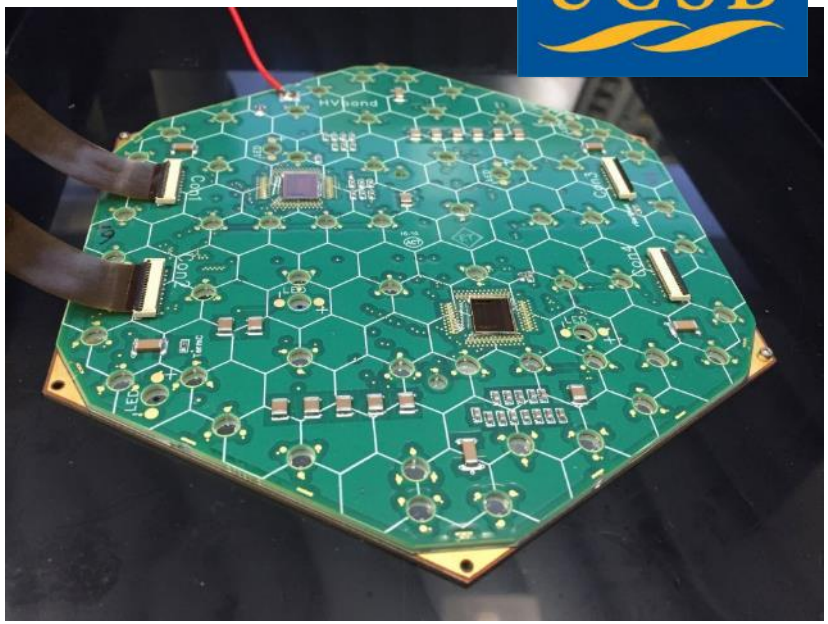
15-Feb-16	**Submit v0 FE chip (SKIROC2-CMS) in 0,35 µm** ⇒ Part 1
Mid-May-16	**Submit FE test vehicles in TSMC130 nm technology** ⇒ Part 2
1-Jun-16	1st Comprehensive Review
30-Sep-16	**1st results from FE test vehicles and second test vehicle submission**
31-Oct-16	Confirm choice of front-end electronics (130 nm)
15-Dec-16	Define architecture & specs for LV/HV supply
15-Dec-16	Define location of DC-DC converters
15-Dec-16	Define location of electrical/optical links
31-Mar-17	**Submit V1 ASIC** ⇒ First 32/64 ch ASIC with full functionnality
31-Mar-17	Choice of Si sensors type: all n-on-p or mixed (i.e. n-on-p and p-on-n)
1-Jun-17	2nd Comprehensive Review
30-Sep-17	1st results from tests of V1 ASIC
1-Nov-17	Submit TDR
30-Jun-18	**Submit V2 ASIC**

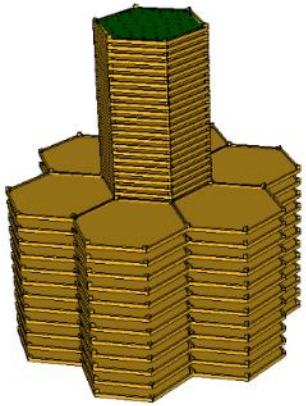
Part 1: SKIROC2-CMS

SKIROC2-CMS: Electronics for testbeam

- Testbeam electronics
  - Use SKIROC2 to exercise system issues (low noise, large range)
  - Complex front-end boards designed at UCSB, Minnesota, FNAL : delicate routing
  - Evolutive readout designed at FNAL

- Development of **SKIROC2-CMS**
  - **Optimized version for CMS test beams**, pin to pin compatible
  - Dual polarity charge preamplifier
  - Faster slow shaper (25ns instead of 200ns)
  - SCA in roll mode (sampling of slow shapers @ 40MHz, depth = 300ns)
  - ToT for high input charge
  - TDC (TAC) for ToA (~20 ps binning, ~50ps jitter)
  - Will replace SKIROC2 on modules for **timing and ToT studies**





This “little” setup has ~14k ch. to read out !

SKIROC2-CMS analogue architecture

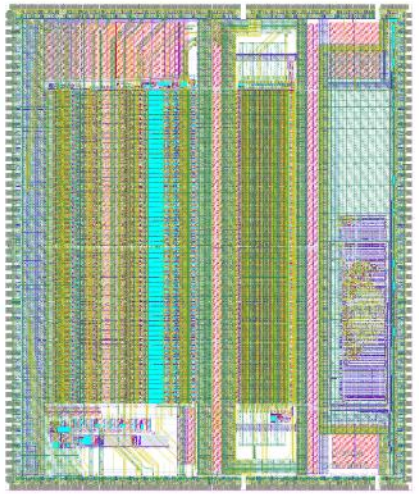
- Input DAC and 3pF calibration Cap.
- Versatile preamplifier
  - Dual polarity: single first stage with input PMOS transistor (available NMOS are directly on substrate), one feedback for each polarity (likely better for positive input charge), high dynamic range optimization
  - 60 dB Open loop gain, 4 GHz GBWP
  - Variable Rf: global 8 bits, from 10k to 2,55M
  - Variable Cf: global 6 bits, from 62fF to 4pF
- Charge measurement in 12 deep SCA
  - Slow shapers: gain 1 and 10, CRRC2; variable shaping time: global 4 bits, from 10ns to 150ns; output buffer
  - 2 measurements by BX, HG and LG
  - Nominal: roll mode @ 40MHz; custom mode: managed by external trigger
- Charge measurement with ToT for signal after peamp saturation
  - Discriminator connected to the preamp output
  - Fast ramp dedicated to the special study of the non-linear part
  - Slow ramp for the entire range (up to 10pC)
  - ToT data are memorized into the feedback capacitance of the integrator, rising edge starts the ramp and falling edge stop it
- Time measurement
  - Fast shaper: CRRC, gain 6, shaping time: 3bits, 1,25 to 9ns
  - Fast discri
  - Ramp: 35ns, rising edge starts the ramp
  - Time SCA: 2 holds done on rising and falling edges of the 40MHz
- Analogue to digital conversion
  - 12 bits Wilkinson ADC, common ramp

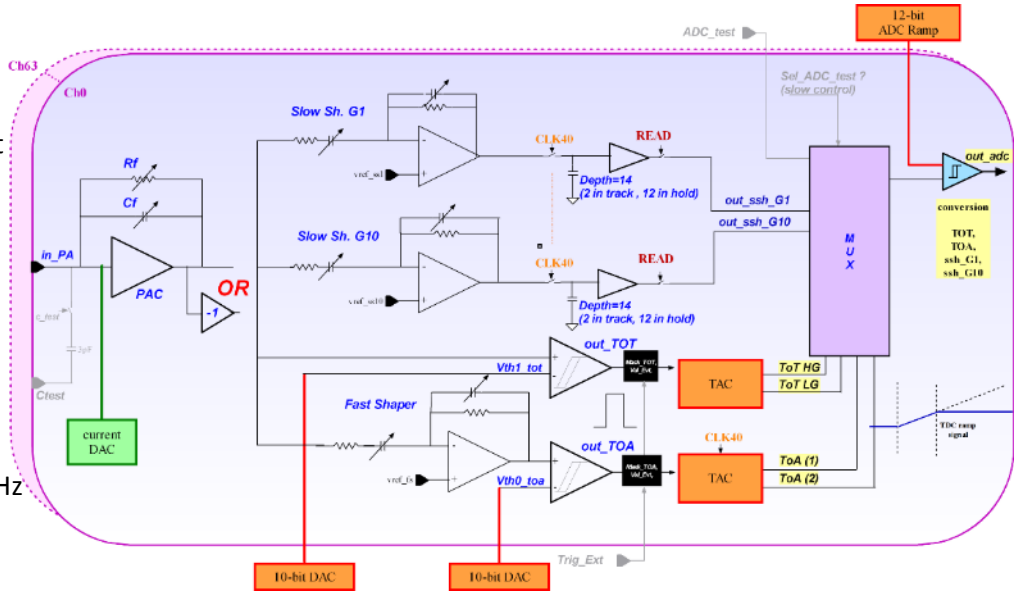
POWER CONSUMPTION

Preamplifiers (positive / negative)	5,3 mW / 5,6 mW
Slow shapers	1,94 mW
ToT	0,1 mW
ToA	2,6 mW
TDC	1,93 mW
Total analog (/channel)	12 – 13 mW

Assuming 20mW power dissipation for the digital part, we expect 850 mW for the entire chip

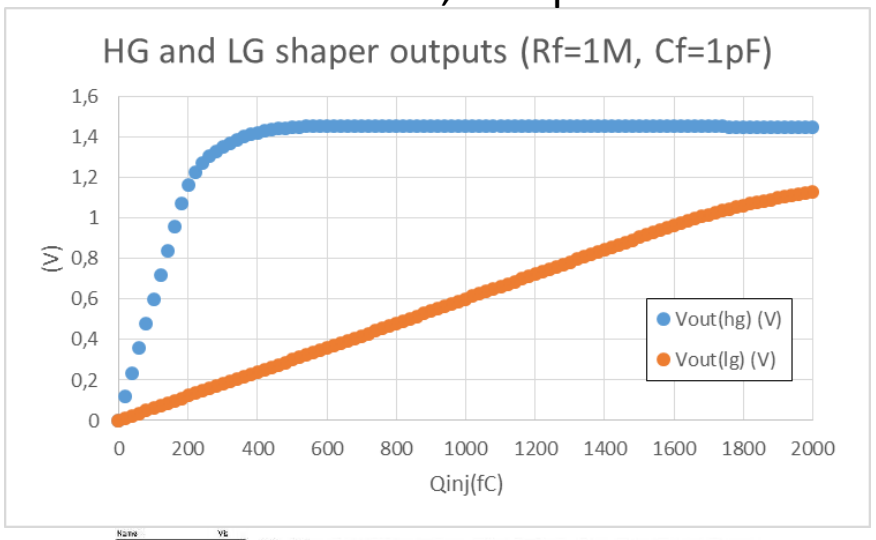
SKIROC2-CMS



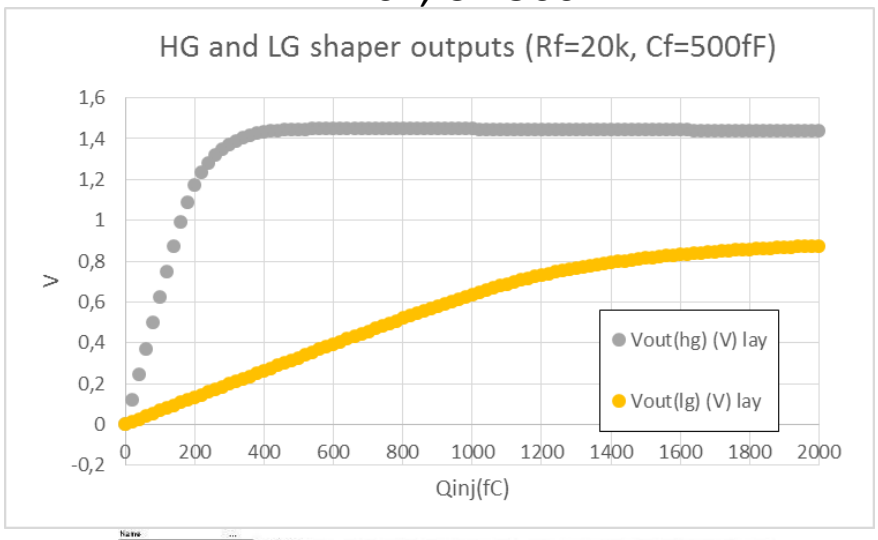


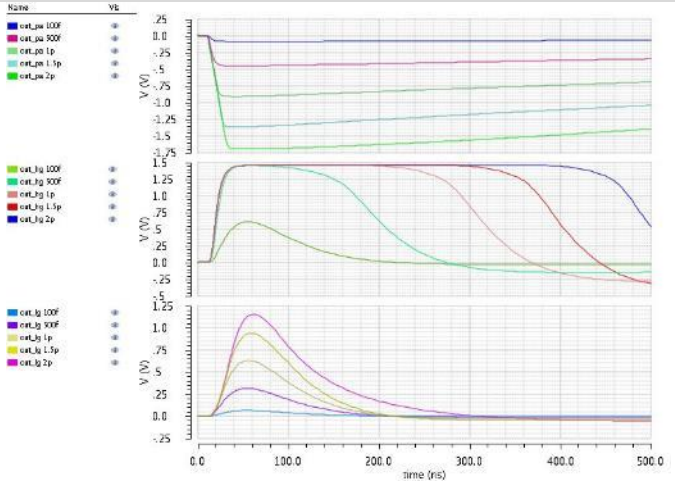
Positive input: HG and LG linearity post-layout simulated

Charge PA
Rf=1M, Cf=1pF



Current PA
Rf=20k, Cf=500fF

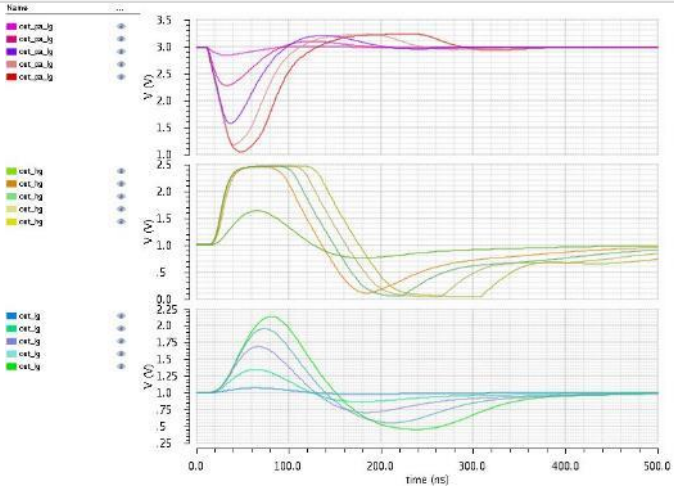




Preamp output

HG shaper output

LG shaper output

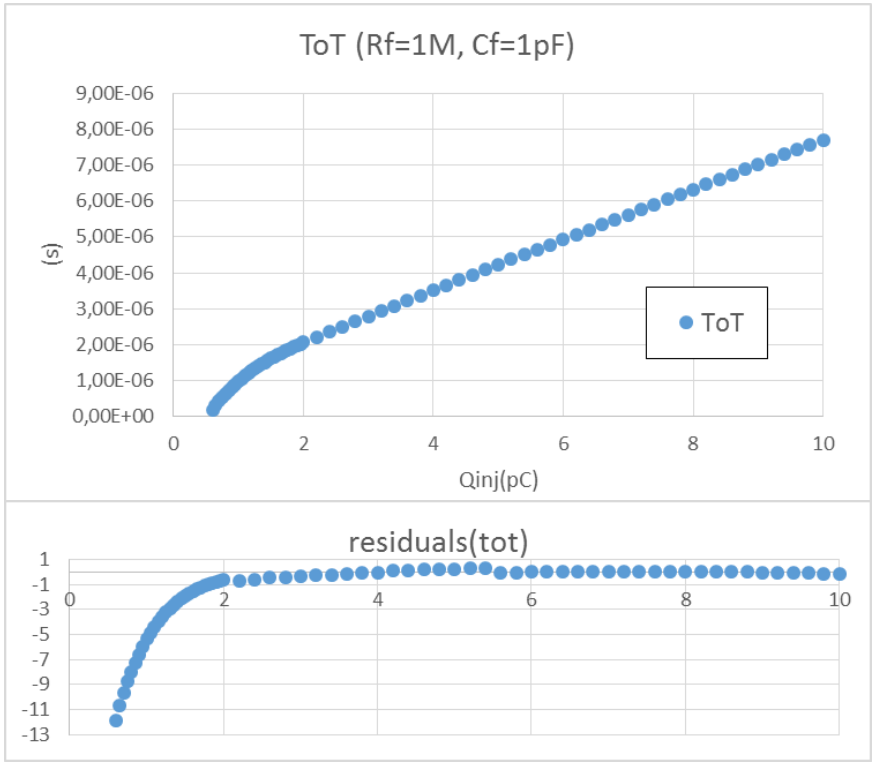


- HG linearity: from 0 to 180 fC
- LG linearity: from 0 to 1750 fC

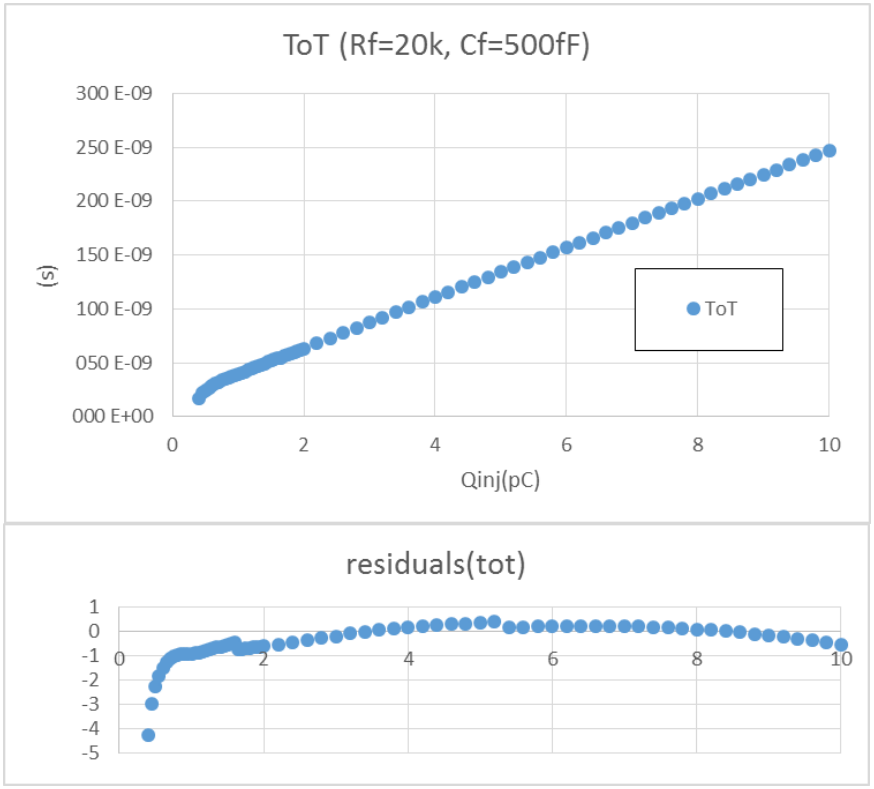
- HG linearity: from 0 to 160 fC
- LG linearity: from 0 to 950 fC

Positive input: ToT post-layout simulated

Charge PA
Rf=1M, Cf=1pF



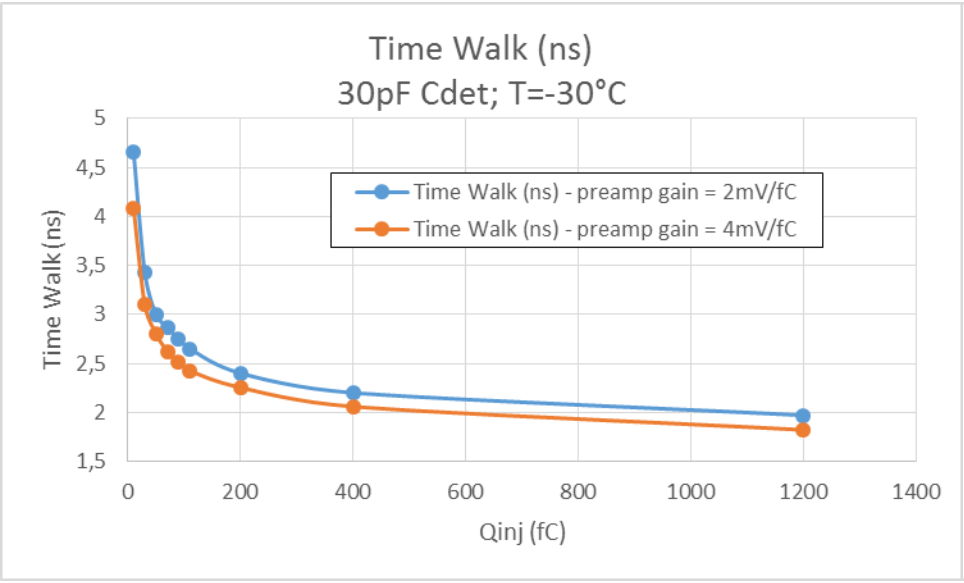
Current PA
Rf=20k, Cf=500fF

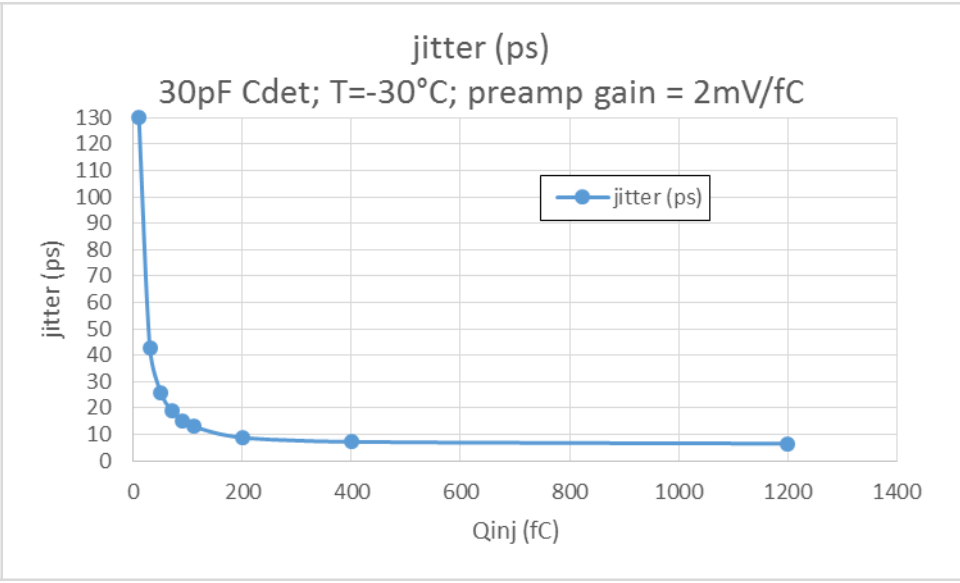


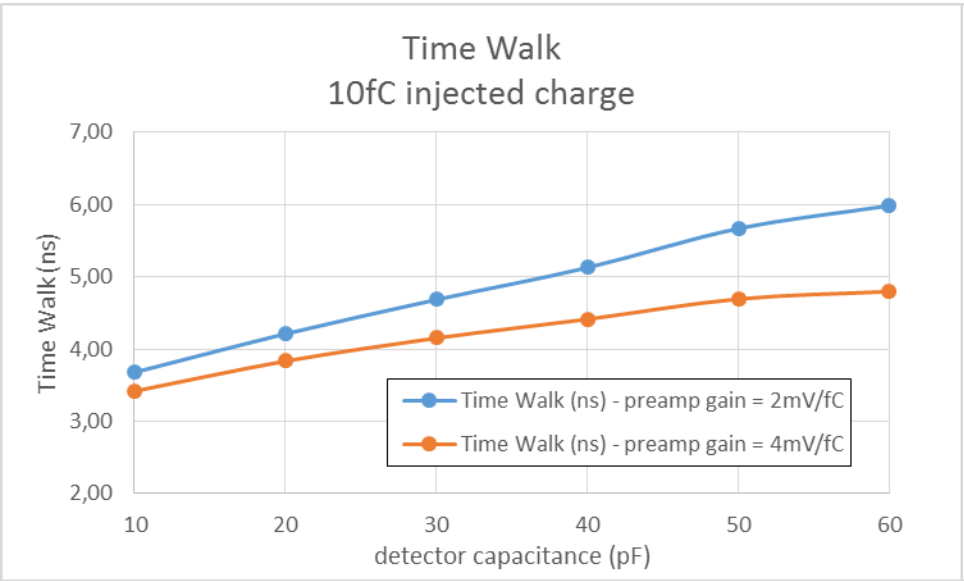
- Threshold @ 700 fC
- Good ToT linearity: from 1,75 pC to 10 pC

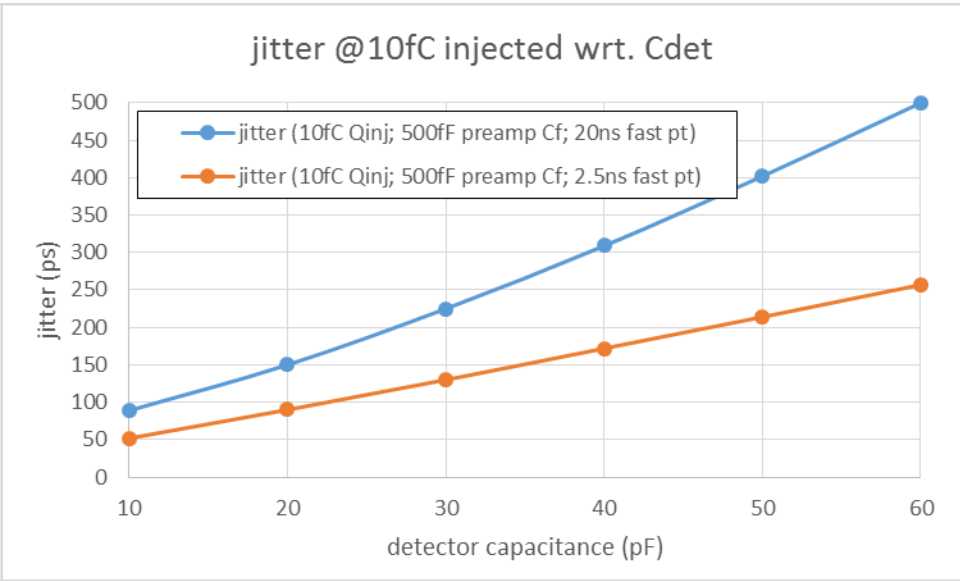
- Threshold @ 450 fC
- ToT linearity: from 1,7 pC to 10 pC

Some time measurement simulated









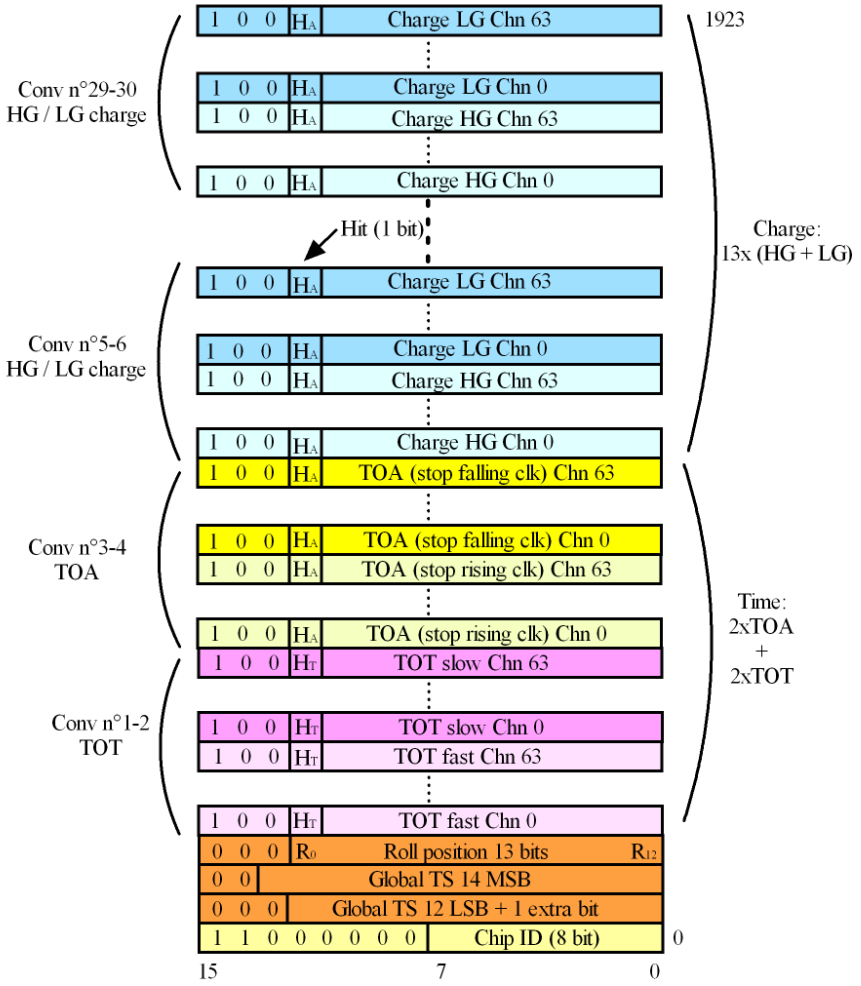
Digital readout scheme

- Based on Calice chips readout scheme

- Roll mode @ 40MHz
- depth 12x25ns=300ns

- 12-bit Wilkinson ADC, starts on external Trigger
- 2 ToT (fast & slow); 2 ToA; 2x12 HG & LG Charge
- Duration (worst case)=2^{12} x 25n x 30 = 3 ms

- OC @ 5MHz (SK2) to LVDS @ 40MHz (SK2-CMS)
- Cst. 1924x16x25 = 770µs

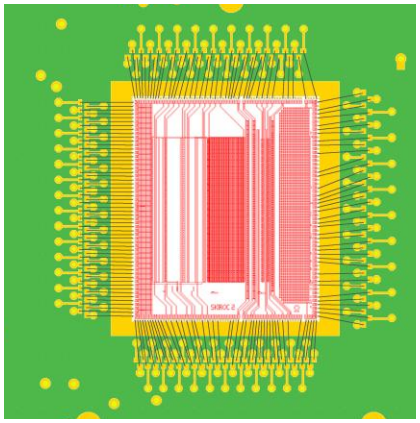


Summary of the SKIROC2-CMS chip

Omega

- HGC targeted Skiroc2-CMS chip variant with
  - n-on-p as well as p-on-n read-out
  - LHC-like ~ 20ns shaping time
  - Leakage current compensation for irradiated sensors
  - Key features and variants of HGC FE architecture
    - Including TDC for precision timing and ToT
  - Pin-to-pin compatible
    - Design submitted, expect chips back in Spring

Landing of SKIROC2(-CMS)
Designed at UCSB



- SKIROC2-CMS aims
  - ToT scheme non linear in region 100-200fC: needs precise calibration and demonstration in Test-beam
  - Will be studied with SKIROC2-CMS and test vehicle
    - Backup with bi-gain and ToT above 1-2 pC or dynamic gain switching

- January 2016: first fully functional Si-HGC modules equipped with existing SKIROC2 chips
  - Skiroc2 designed for p-on-n sensors, but too slow shaping time, readout based on Calice requirements
- Spring 2016: test beams at FNAL with Si-HGC EE slice equipped with Skiroc2
  - Enable tests of EM calorimetric response
  - Prepare for more detailed studies using modules equipped with Skiroc2-CMS
- Fall 2016: test beams at CERN with Si-HGC EE and FH slice equipped with Skiroc2-CMS
  - Enable detailed studies of calorimetric response and performances of baseline architecture and variants
  - Aim for timing studies of EM and Hadronic shower evolution with ~50ps calorimeter cell timing resolution

Part 2: test vehicle 1 (TV1)

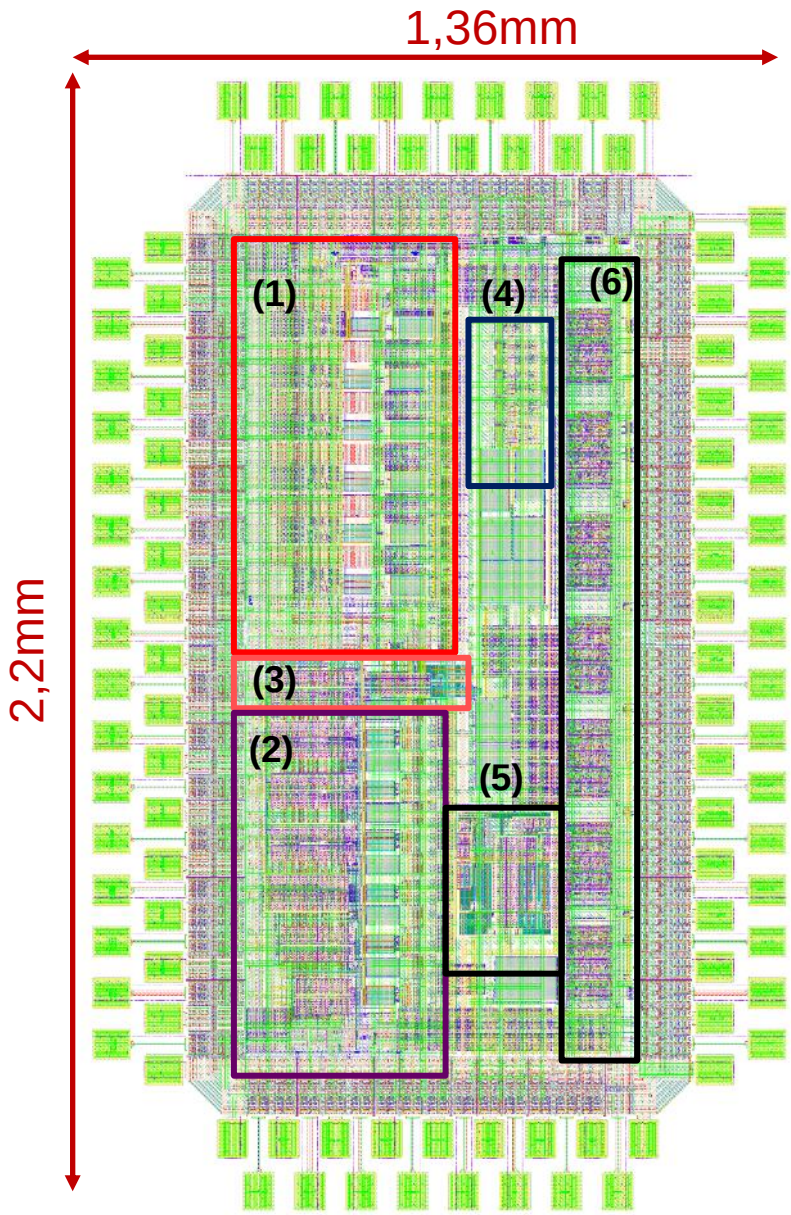
Test vehicle floorplan: 130nm

- Area: 2,2x1,36 mm²
- 101 PADs, 100µm pitch
- Power supply: 1,2 – 1,5 V
- Submission date: mid-may 2016

- Floorplan
  - (1) positive input preamps x6
  - (2) negative input preamps x6
  - (3) baseline channel (CERN) x1
  - (4) discriminators x4
  - (5) CRRC shapers: HG and LG
  - (6) digital part

- Available outputs
  - Direct preamp output
  - Preamp after shaper
  - Preamp after discriminator

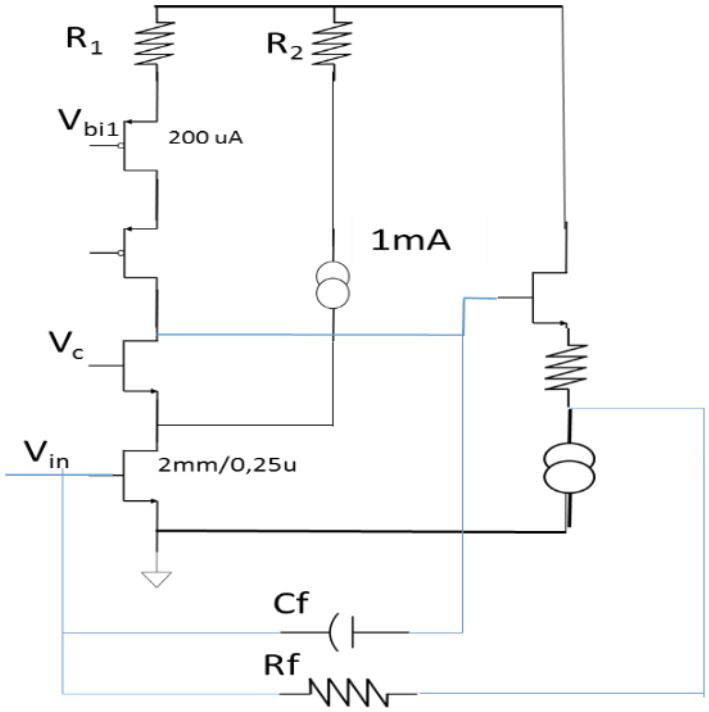
- Dedicated PAD available to characterize the shapers or the discriminators
- All bias can be externally tuned

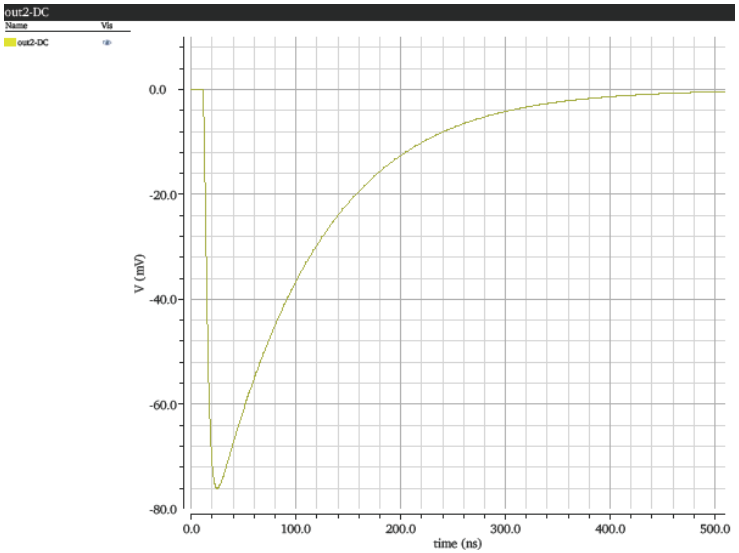


Input NMOS transistor preamplifier for positive signal

- 6 different preamps for positive signals
- Based on a cascode architecture
- Used different NMOS sizes (1200µ, 2400µ, 3600µ) and transistor flavors proposed by the technology (“normal”, “HiVt”, “LoVt”)
- Variable Cf from 100fF to 1,5pF step 100fF
- Variable Rf: 20k, 200k and 1MΩ
- Optimize to get open loop gain above 60dB and minimize noise
- Power consumption: ~2mW

- e_n = 0,4 nV/sqrt(Hz)
- rms noise = 210 µV
- With 50pF Cdet, after 25ns shaper, ENC ~1.3ke-



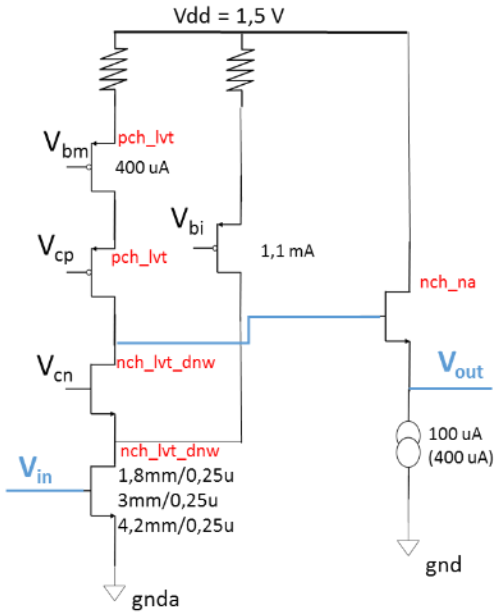


Qinj=100fC; Cd=50pF; Cf=1pF; Rf=20k

Input NMOS transistor preamplifier for negative signal

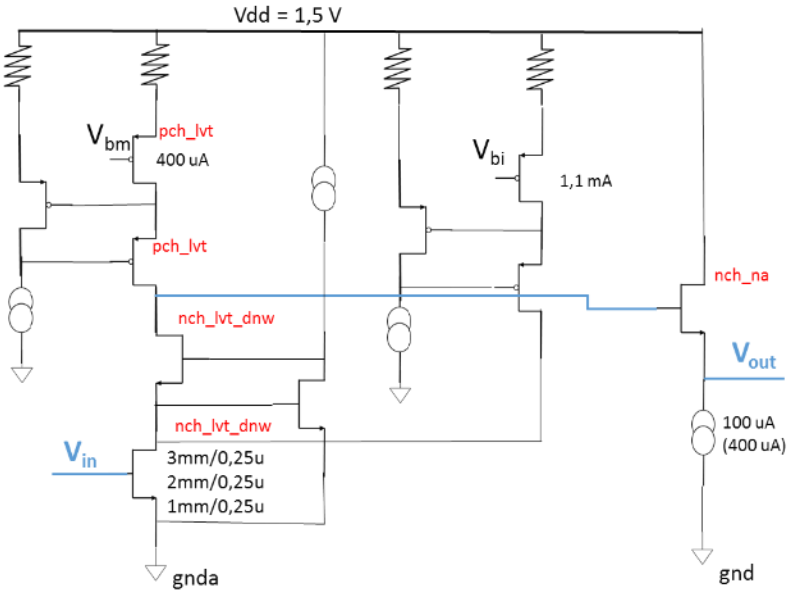
- 6 different preamps for negative signals
- Used different NMOS sizes and architectures
- Variable Cf from 100fF to 1,5pF step 100fF
- Variable Rf: 20k, 200k and 1MΩ

- With 50pF Cdet, 20k Rf, after 25ns shaper, ENC ~1.2ke$^-$
- With 50pF Cdet, 1M Rf, after 25ns shaper, ENC ~ 1ke$^-$



- Input stage: cascode with NMOS input transistor
- Output buffer: source follower with NMOS native transistor biased with 100µA
- 62 dB open loop gain; 2,4 GHz GBP; Input impedance: 16Ω (50Ω @ 50MHz)
- Power consumption: 2,4 mW (@ 1,5V)

- Three sizes of input NMOS transistors



- Input stage: regulated cascode with NMOS input transistor
- Output buffer: source follower with NMOS native transistor biased with 100µA
- 94 dB open loop gain; 3,5 GHz GBP; Input impedance: 0,5Ω (43Ω @ 50MHz)
- Power consumption: 2,85 mW (@ 1,5V)

- Well suited for high loop gain preamp (0,2pF Cf)
- Three sizes of input NMOS transistors

TV1: linearities

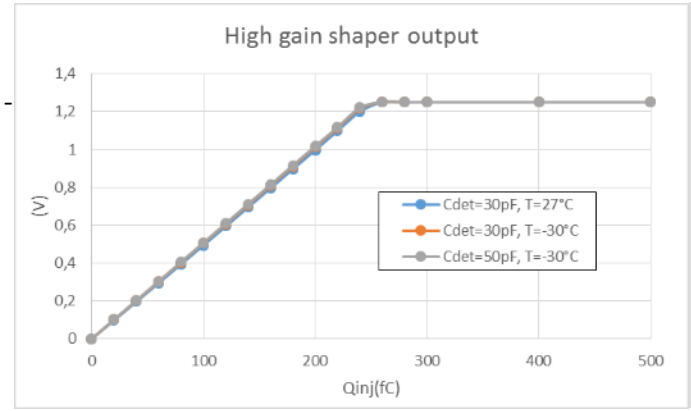
- 1pF Cf, 20K Rf, 30 and 50pF Cdet, 27 and -30 °C

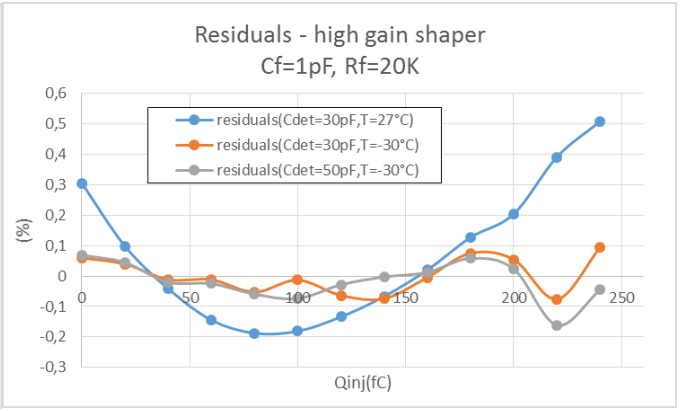
- High gain:
  - linear up to 240 fC
  - Better linearity at low temperature

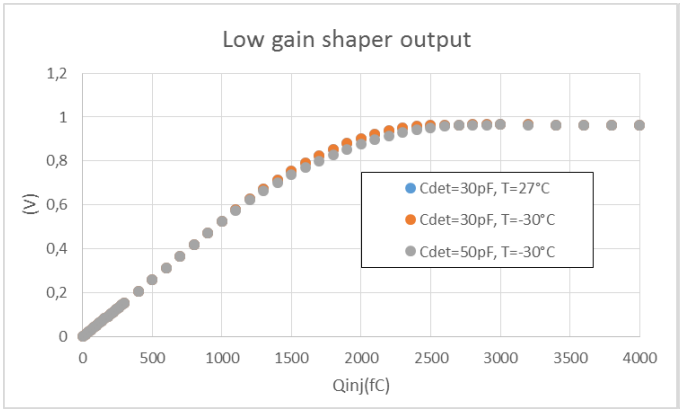
- Low gain:
  - Good linearity up to 1200 fC
  - Saturation occurs before with high Cdet

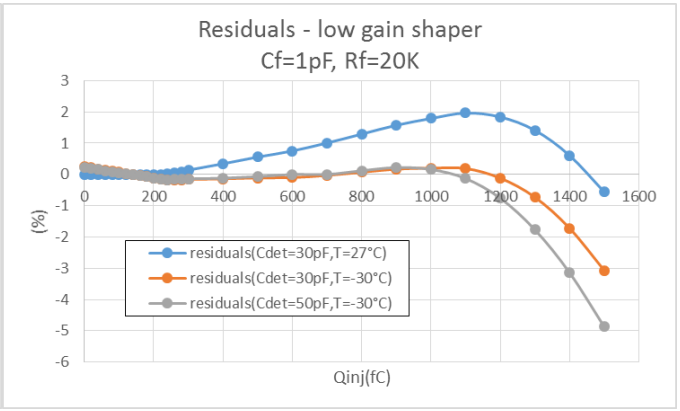
- Time over Threshold:
  - Threshold @ 250 fC
  - Linearity better than 1% begins around 1300 -1600 fC
  - Dependence to the temperature: 26ns/pC @ 27°C and 30ns/pC @ -30°C
  - Low dependence to Cdet: 29ns/pC @ 30pF Cdet and 30ns/pC @ 50pF Cdet

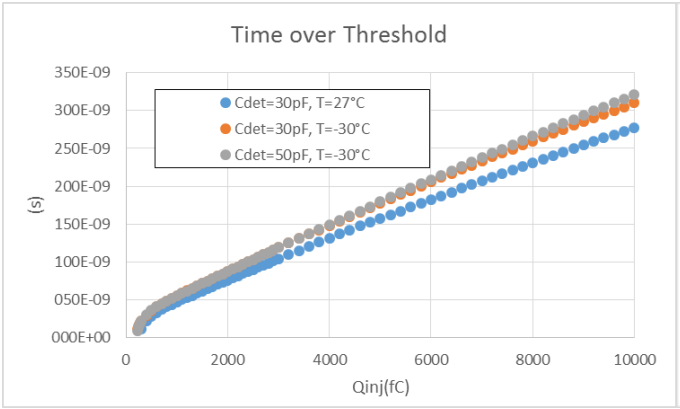
- There is never a good overlap between low gain and ToT, precise characterization is needed. It is due to the non-linear behavior when preamplifier pass through from the non-saturation mode to the saturation mode

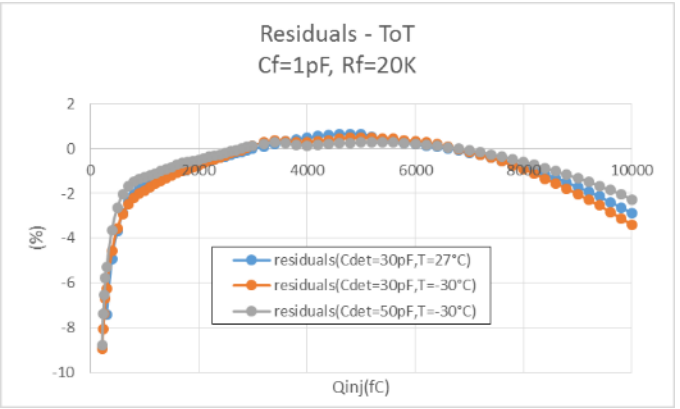






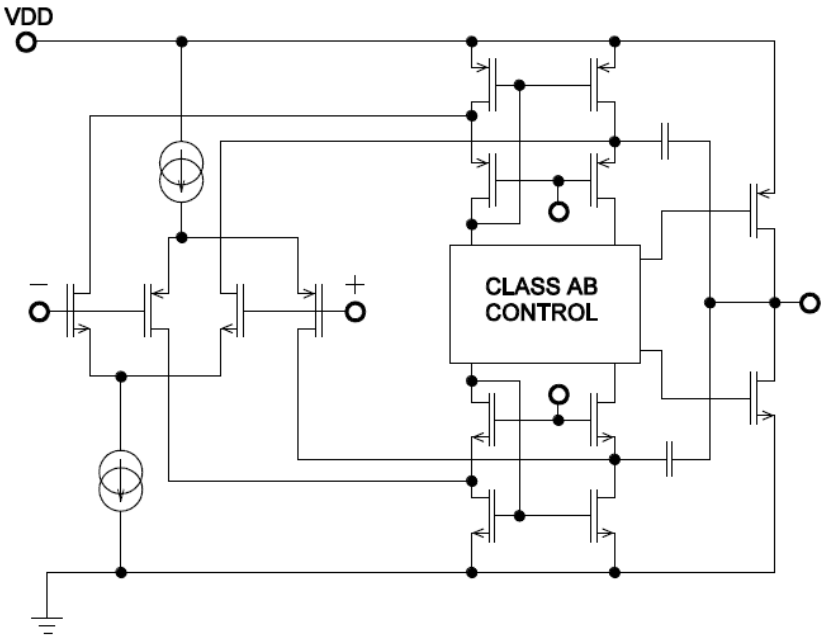






CRRC shapers

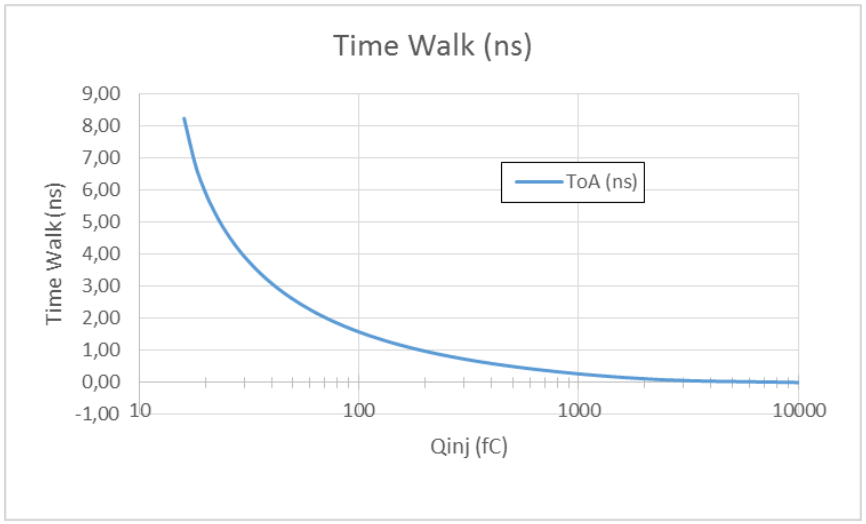
- Rail-to-Rail class AB operational amplifier
  - Cascode-miller compensation tunable on 5 bits
- 2 shapers
  - Gain 1 and gain 10
  - Variable shaping time: global 4 bits, from 5ns to 75ns

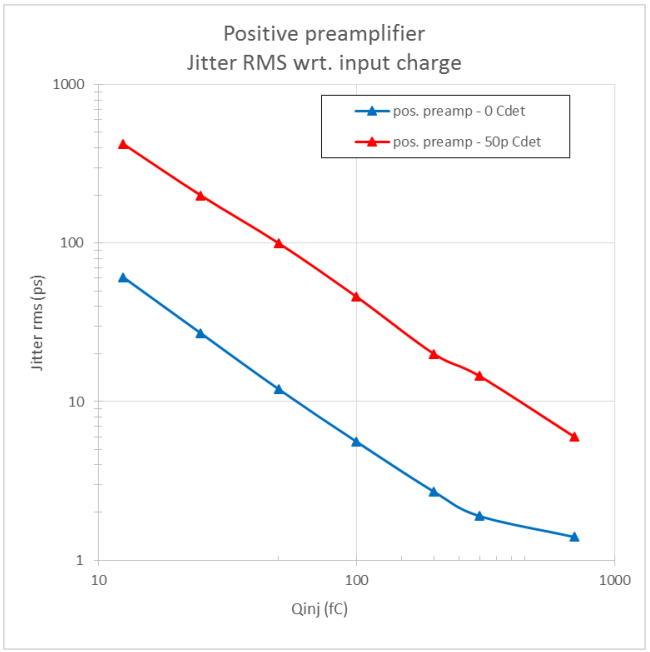


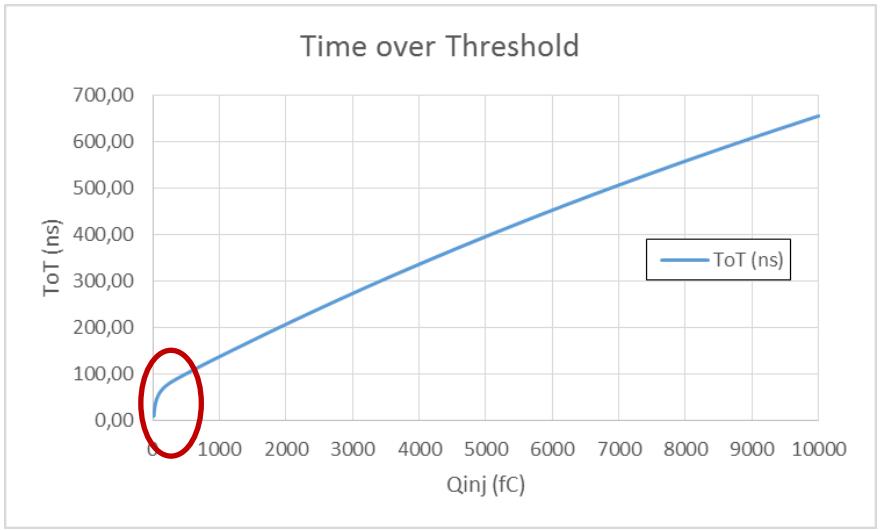
Discriminators

- 4 fast discriminators designed (2 designs for each polarity) for ToA, ToT and ADC
- Power consumption: ~750uW
- Offset: 3,5mV rms

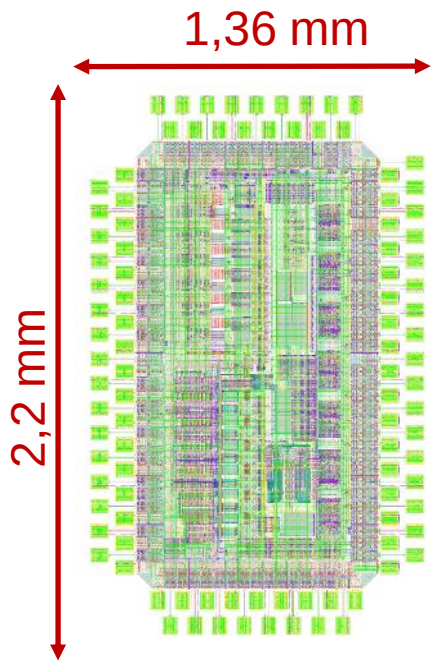
- Time Walk
  - 6ns @ 20fC (~10 MIP)
  - 1,5ns @ 100fC (~50 MIP)
- ToT
  - Linear from 1pC to 10pC
- Jitter
  - Without detector capacitance: 60ps rms @ 10fC (~3 - 6 MIP)
  - With 50pF detector capacitance: 400 ps rms @ 10fC (~5 MIP), 50 ps rms @ 100 fC (~50 MIP)
  - Jitter performances should be improved with a fast and high gain shaper after preamplifier

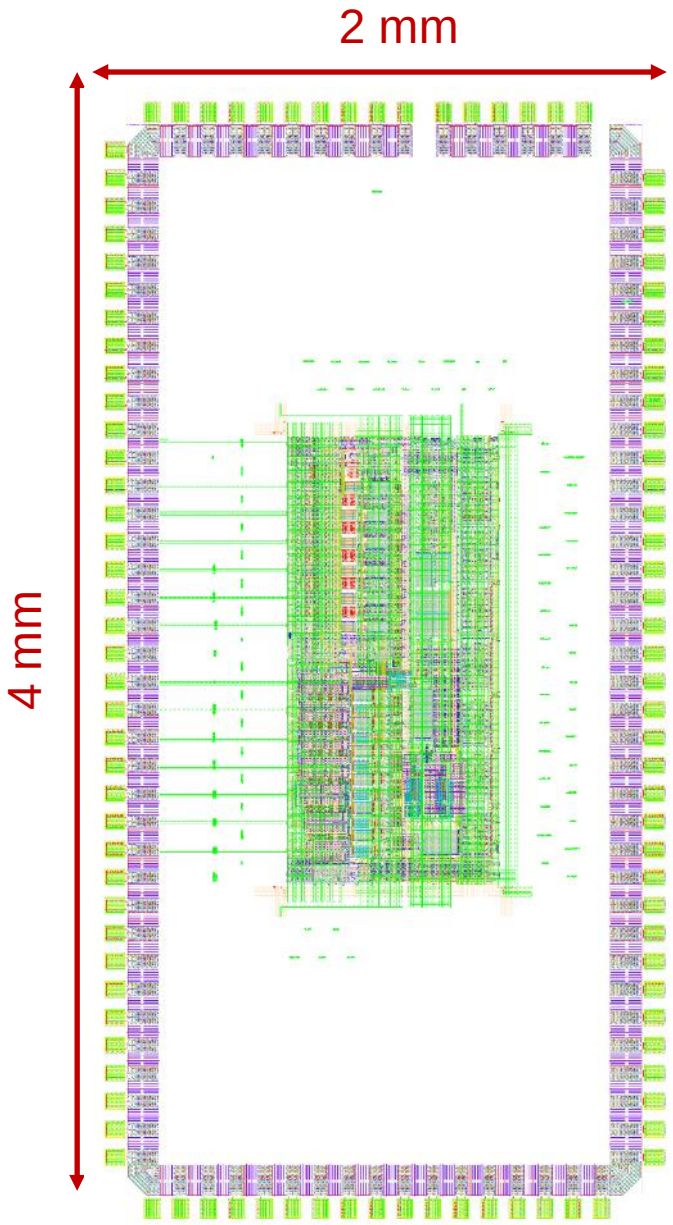






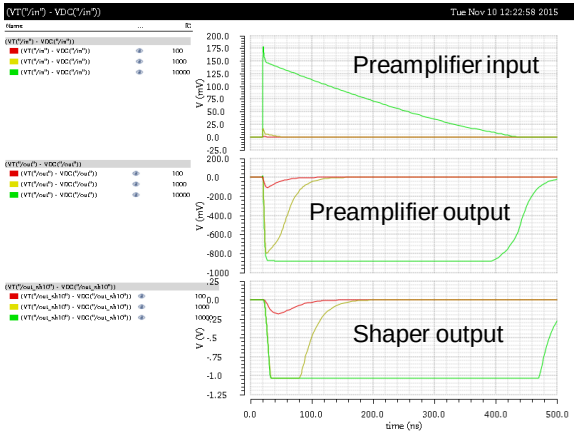
- Packaging issues
  - Wire bond angles between chip pads and package plots cannot be higher than 20°
  - Wire bond length issue
  - Finally enlarged pad ring => 2x4mm single in-line



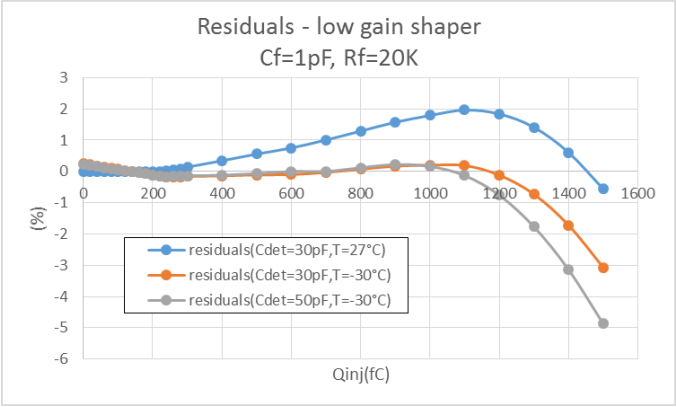


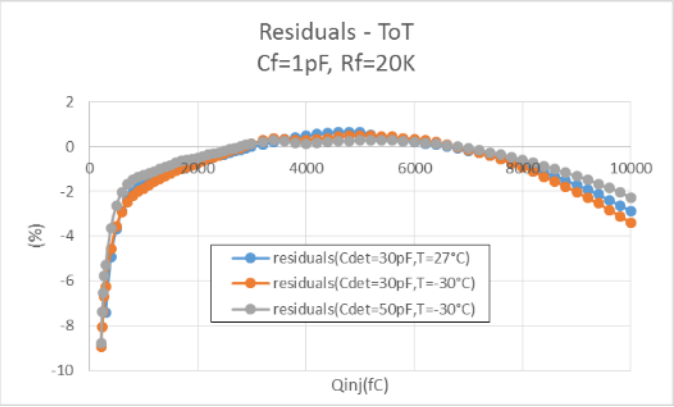
ToT challenges

- High crosstalk when preamplifier is saturating
- Long dead time due to ToT. It depends of preamplifier feedback resistance
- There is never a good overlap between low gain and ToT, precise characterization is needed. It is due to the non-linear behavior when preamplifier pass through from the non-saturation mode to the saturation mode
- Trigger path has to deal with ADC data (mV) and ToT data (ns) and with a non-linear ToT behavior at the first. The ToT data have to be linearized.



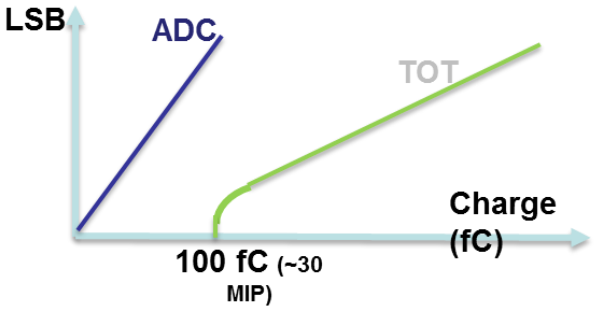
Transient signals for 100, 1000 and 10000 fC injected charge

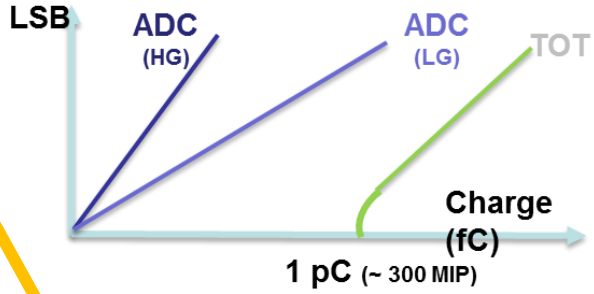


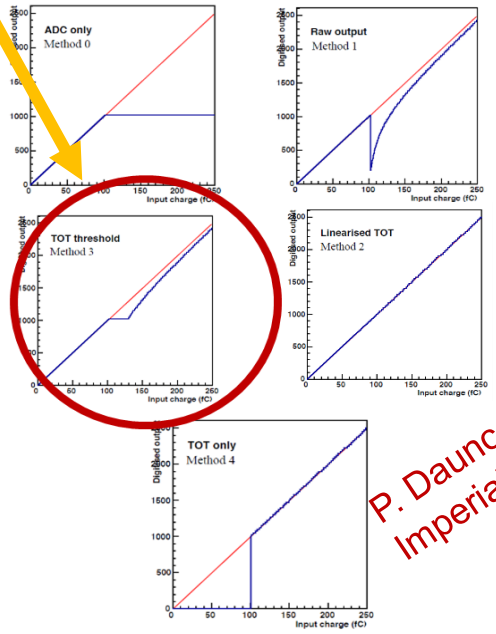


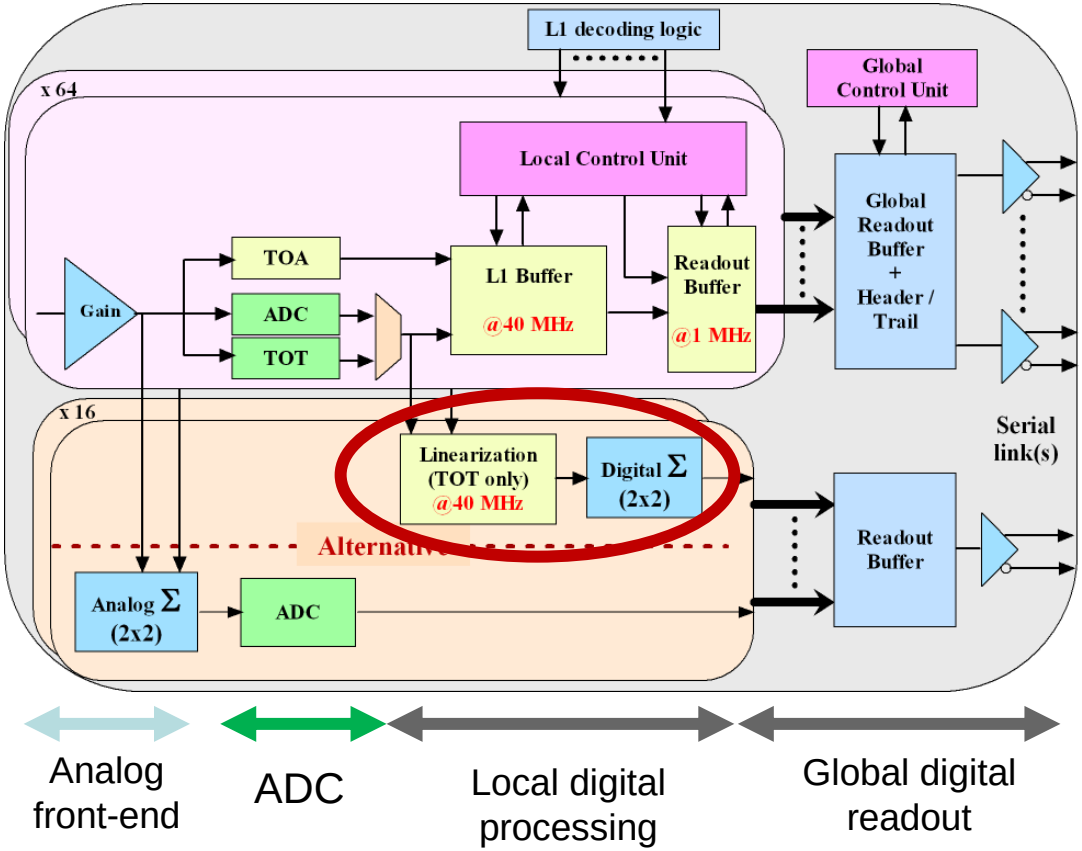
Digital block: 1MHz readout architecture / trigger sums

- Study 2x2 linearization to be ready for 2nd TV:
  - ADC data
  - TOT without non-linear region
- Focusing on "method 3"
- Solution applicable for baseline or bi-gain PA







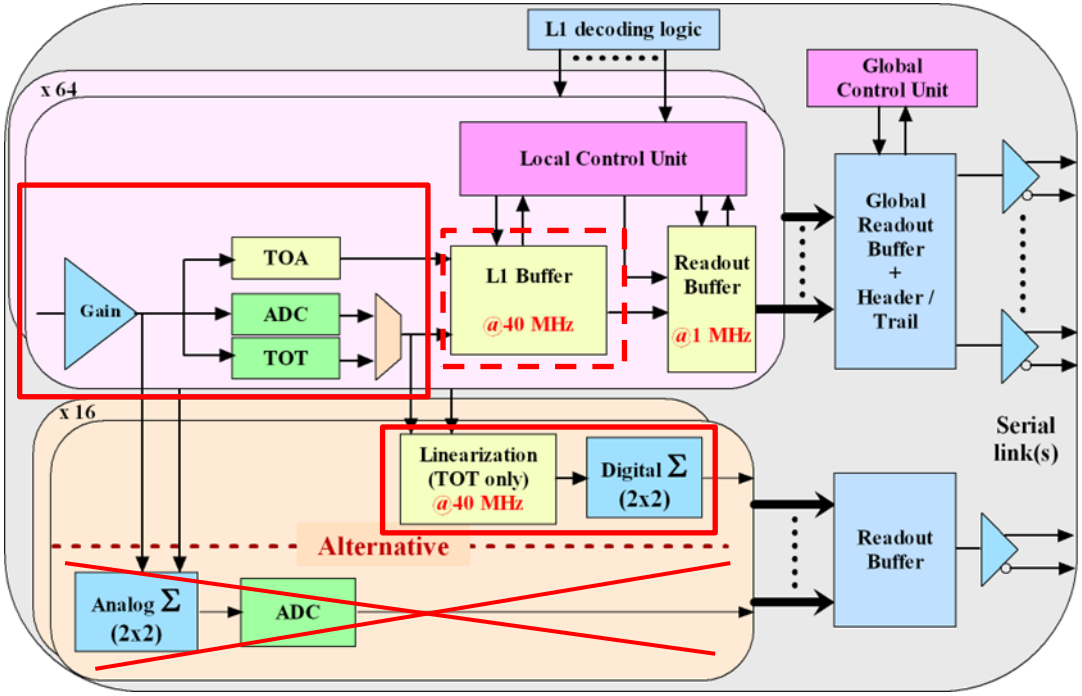


P. Dauncey
Imperial College

What do we plan to submit in TV2 ?

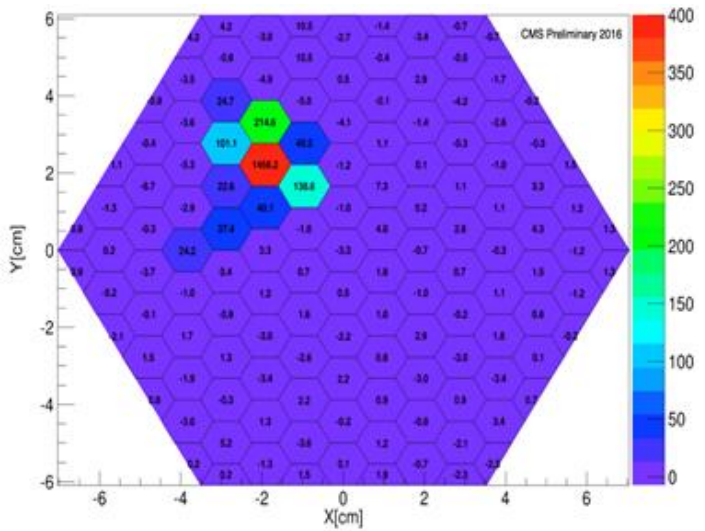
- Full analogue channel
  - Preamplifiers, shapers, comparators, input DAC (leakage compensation)
  - 10-bit ADC, 12-bit TDC
- Digital sum for trigger path
  - Linearization ToT @ 40 MHz
  - Digital sum: 2x2 cluster
  - L1 buffer for 1 MHz readout
- Common services
  - 10-bit DAC, bandgap, LVDS, PLL and DLL

September 2016



Conclusion

- Challenging detector
  - High speed low noise large dynamic range readout
  - High integration and large data output

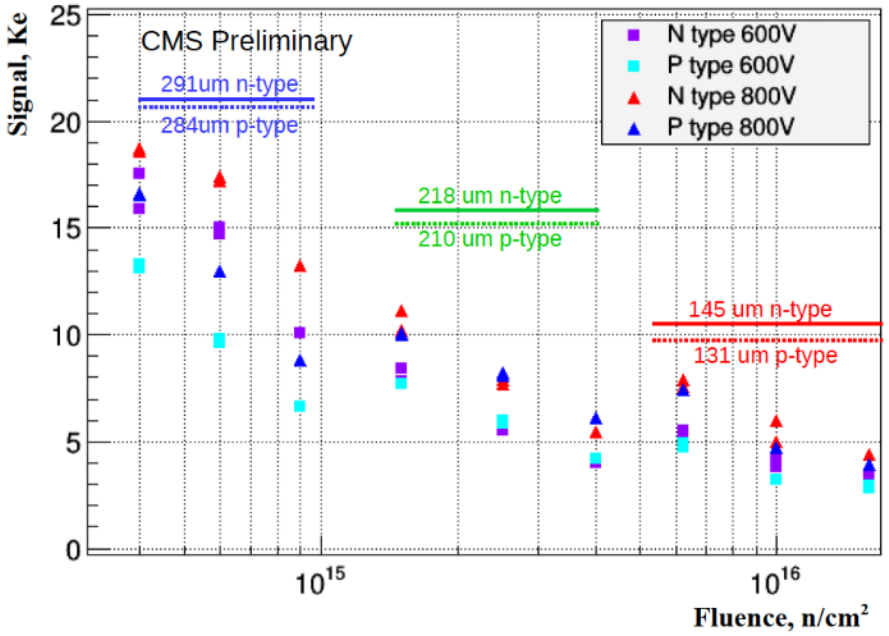


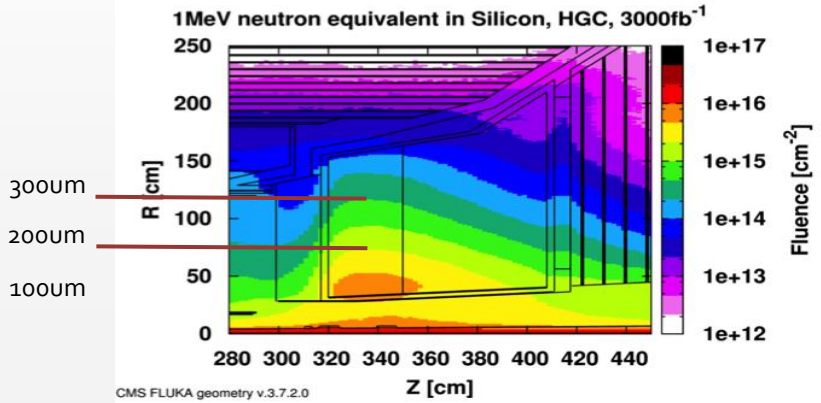
- Several issues to be studied rapidly
  - ToT accuracy. Timing performance.
  - System issues.
  - Prototypes assembled for tests in beam
  - Will be studied with SKIROC2-CMS and test vehicle
    - Backup with bi-gain and ToT above 1-2 pC or dynamic gain switching

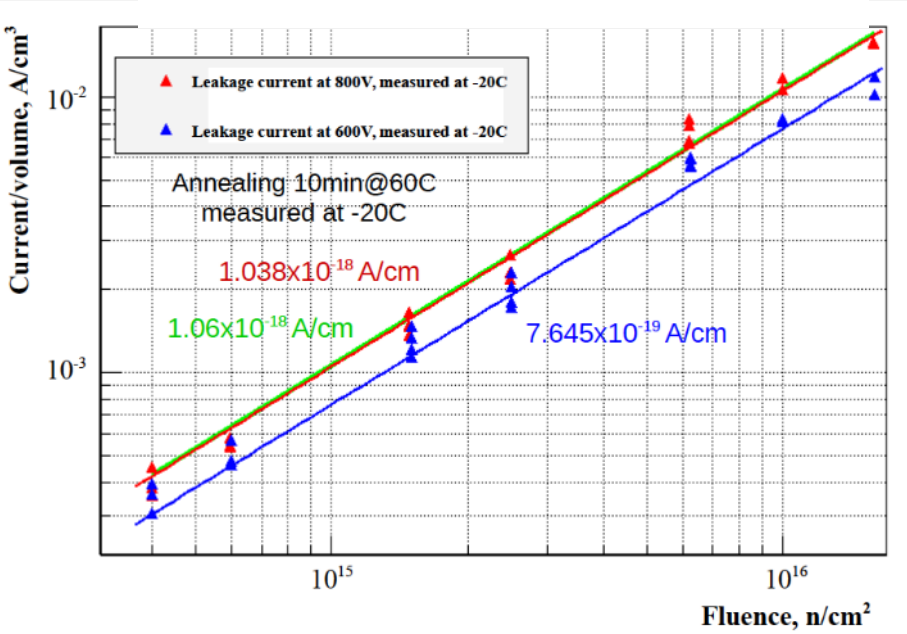
Additional slides

Basic Silicon sensor R&D

Essential results documented in TP







Slide From M. Mannelli, ACES Workshop

SKIROC2-CMS: Noise simulations

- Cd = 50pF, T=-30°C, noise after HG shaper, no leakage current

ENC	Rf=1M, Cf=1pF	Rf=20k, Cf=500fF
Positive input	0,2fC (1250 e-)	0,25fC (1560 e-)
Negative input	0,23fC (1440 e-)	0,3fC (1875 e-)

- Noise after HG shaper is dominated by input PMOS transistor

SKIROC2-CMS: Crosstalk and power consumption

CROSSTALK

Signal	Crosstalk	Crosstalk
Preamp output	0,34%	0,35%
HG shaper	0,3%	0,7%
LG shaper	0,34%	0,35%
Fast shaper	0,62%	3%(1)

(1) Neighboring channels trigger when hit channel is saturating

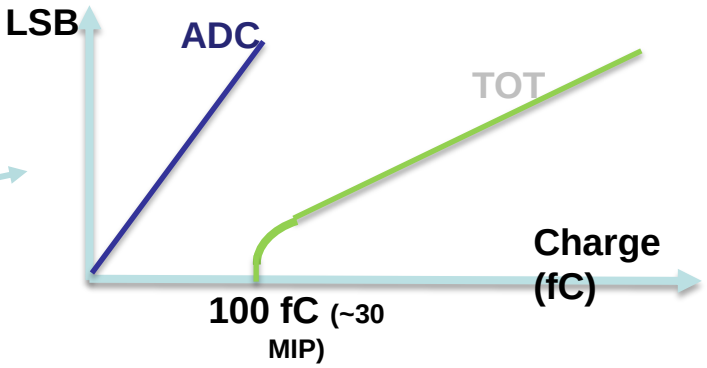
POWER CONSUMPTION

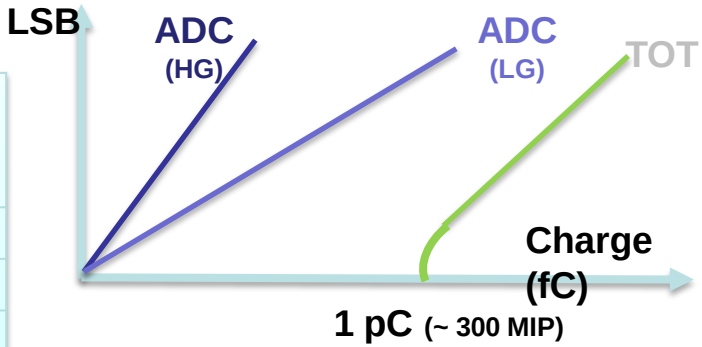
Preamplifiers (positive / negative)	5,3 mW / 5,6 mW
Slow shapers	1,94 mW
ToT	0,1 mW
ToA	2,6 mW
TDC	1,93 mW
Total analog (/channel)	12 – 13 mW

Assuming 20mW power dissipation for the digital part, we expect 850 mW for the entire chip

Trigger: 1MHz readout issues / info

- 3 possibilities for sums:
  - Analog sum: cost = 1 ADC / 4 channels
  - Full range Digital sums: cost 1 LUT / channel
    - Correct for TOT non linearity
    - Correct different slopes
  - ADC(s) range Digital sums:
    - up to 30 MIP in baseline
    - Up to 300 MIP in bi-gain (HG/LG factor of 2)





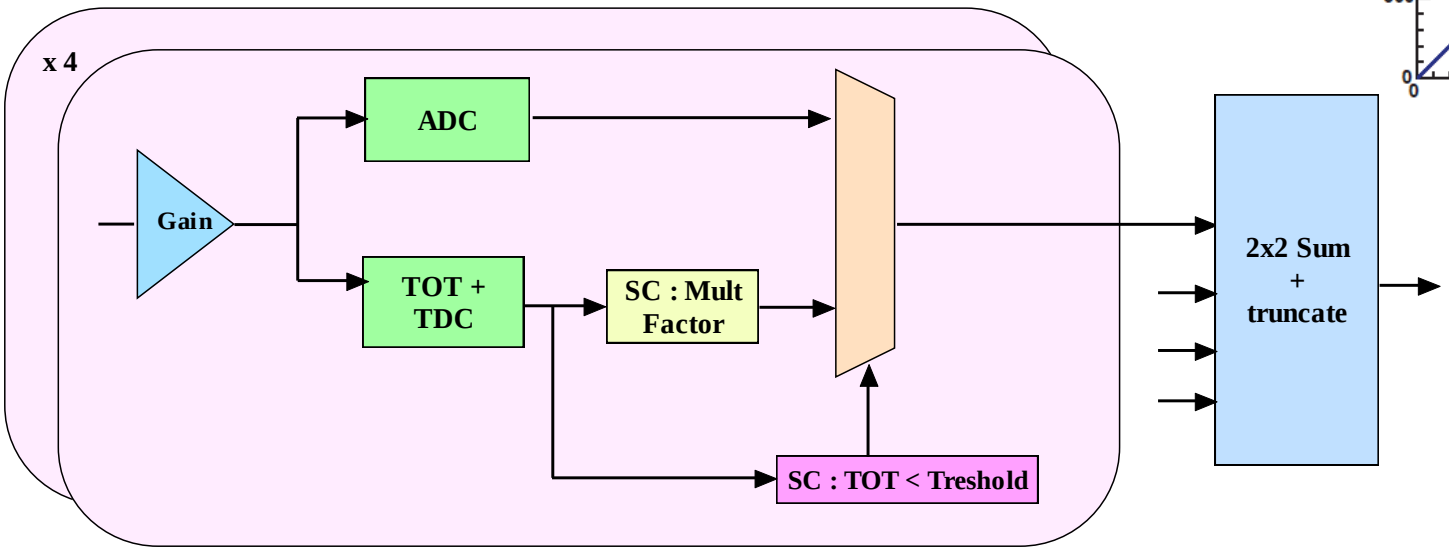
	Range	Sum precision	Extra ADC	Extra LUT power
A-sums	Full	++	16	0
Full D-sums	Full	++++	0	64
ADC D-sums (baseline)	30 MIP	+	0	0
ADC D-sums (bi-gain)	300 MIP	+++	0	0

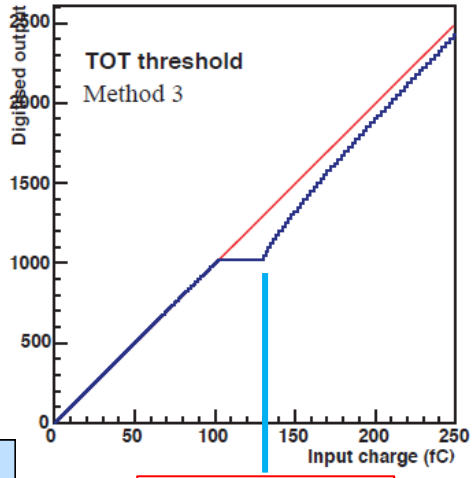
- For sums, mapping sensor cell to ASIC channel is done on PCB
  - Could have 2x2 / 4x4 sums (if adjacent channels ex:0-3 and 4-7)
  - Adding extra mapping/confirmation in ASIC may add complexity / power consumption

- Bandwidth: (dedicated slide ?) TP + DATA

Architecture for “method3”

- Block inputs:
  - Charge ➔ ADC and TOT
  - Multiplication factor (SC) ➔ needed to have the same slope between ADC / TOT (0 to 1 with step 2^{-k})
  - TOT Threshold (SC) ➔ to remove TOT data below it





Threshold

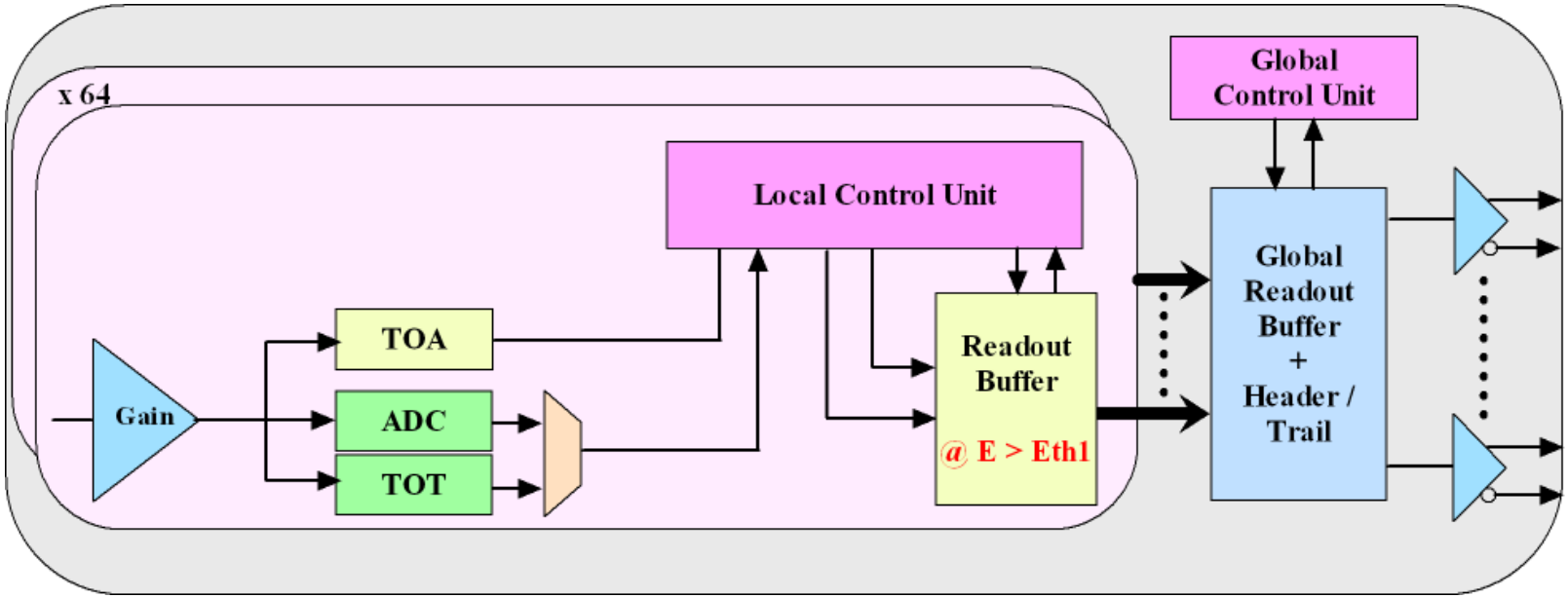
- Design and simulation:
  - VHDL block written, simulated and synthetized
  - Full process takes about **15 ns** (post synthesis)
  - Next steps: estimate power/timing vs multiplication factor precision
  - Easily adaptable to all “method” (except 2) + Baseline & Bi-Gain architecture

Mult Factor:

$$\sum_{k=0}^{n} a_k \,.\, 2^{-k}$$

Trigger: 40MHz readout architecture

- 64-channel ASIC with 0-suppress (see Philippe talk @ Engineering days):
  - 1 bit for empty cells
  - E > Ethr1, register ADC
  - E > Ethr2, register ADC + TOA



1MHz readout

- Trigger logic / mapping done outside
- Reduction of buffers inside FE
- Increase Bandwidth / chip
- Power balance should be estimated