CHESS2  Front end readout of the multi-segmented HV CMOS sensors

HERVÉ GRABAS ON BEHALF OF THE STRIP CMOS COLLABORATION.
Upgrade Strip sensor – Baseline sensor

2.5cm long strip - 75µm wide. Dual silicon sensor.
Strip detector hit occupancy

Consistent with simulation by Nick Edwards:

Sim. Marco Battaglia [high pT H → bb jets]
1% average occupancy of the detector is not an issue.

**No de-randomizer in the sensor.**

Need to be able to cope with bursts of ~20 hits in the detector.

Contrary to the Baseline Sensor, we cannot retain all the hits in the CHESS detector.

<table>
<thead>
<tr>
<th>Nb of strips in group</th>
<th>Wirebonds needed</th>
<th>Wirebonds per strip @320MHz</th>
<th>Max. number of hits @320MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>512</td>
<td>$5 + 1 + 9 = 15$</td>
<td>0.03</td>
<td>8</td>
</tr>
<tr>
<td>256</td>
<td>$(5 + 1 + 8) \times 2 = 24$</td>
<td>0.045</td>
<td>16</td>
</tr>
<tr>
<td>128</td>
<td>$(5 + 1 + 7) \times 4 = 52$</td>
<td>0.1</td>
<td>32</td>
</tr>
<tr>
<td>64</td>
<td>$(5 + 1 + 6) \times 8 = 96$</td>
<td>0.18</td>
<td>64</td>
</tr>
</tbody>
</table>

- We are going to use a 128 strips group retaining 8 hits.
## Baseline to HV-CMOS

<table>
<thead>
<tr>
<th><strong>Baseline</strong></th>
<th><strong>HV-CMOS</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Number of strip</strong></td>
<td>256 (for comparable area)</td>
</tr>
<tr>
<td><strong>Strip pitch</strong></td>
<td>75µm</td>
</tr>
<tr>
<td><strong>Strip segmentation</strong></td>
<td>None</td>
</tr>
<tr>
<td><strong>Number of sensor</strong></td>
<td>2 (stereo)</td>
</tr>
<tr>
<td><strong>Output signal</strong></td>
<td>Analog</td>
</tr>
<tr>
<td><strong>Max. nb. of hits</strong></td>
<td>256/ b. crossing</td>
</tr>
<tr>
<td><strong>Nb. of wirebonds</strong></td>
<td>1/strip</td>
</tr>
</tbody>
</table>
HV-CMOS Monolithic Active Sensors

Increase the depletion region:
- Increasing high voltage, up to 120V with AMS H35
- Increasing substrate resistivity, possible 1000ohms-cm
Strip sensor dimensions

128 Strip
5mm

630µm

40µm

32 pixels in a strip – 2cm
## Specifications - Motivations

<table>
<thead>
<tr>
<th>Specifications</th>
<th>Specs</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate resistivity</td>
<td>20Ohms to 1000Ohms</td>
<td>MIP From 1500e to 4000e</td>
</tr>
<tr>
<td>Substrate high voltage bias</td>
<td>120V</td>
<td>40% more charge vs 60V</td>
</tr>
<tr>
<td>Pixel size</td>
<td>40µm x 630µm</td>
<td>400fF det. capacitance</td>
</tr>
<tr>
<td>Number of pixel per strip</td>
<td>32</td>
<td></td>
</tr>
<tr>
<td>Number of strips</td>
<td>128</td>
<td>Factor ~2 improvement in r-phi resol.</td>
</tr>
<tr>
<td>Timing resolution</td>
<td>25ns</td>
<td></td>
</tr>
<tr>
<td>Maximum number of hits per strip</td>
<td>1 + flag</td>
<td></td>
</tr>
<tr>
<td>Maximum number of hits per 128 strips</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>Readout speed</td>
<td>320MHz</td>
<td></td>
</tr>
<tr>
<td>Number of wirebonds</td>
<td>28/128strips (data only)</td>
<td>x5 reduction</td>
</tr>
<tr>
<td>Additional constraint</td>
<td>Rad-hard design</td>
<td>Periphery: dead area 4mm - shorter strips</td>
</tr>
</tbody>
</table>
CHESS2 architecture

- Column Decoder
  - 128 x 32 pixels
  - Half Comparator, Latch & Hit encoding
  - Records Hits
  - Select 1 Hit/Strip
  - Select 8 Hits

- Strip Encoder
- Global DACs
- SACI
- Control Logic
- Global Registers
- Matrix Pointers
- LVDS TX
- LVDS output

Configure CHESS2

Doesn’t reflect actual size or placement
CHESS2 reticle layout view

18.6mm
Possible dice line 100µm

2.4mm

2 array mirrored
Shared pads

24.3mm

Test structures

1 array standalone
Independent pads
Can be diced away.
One array - dimensions
CHESS2 pixels

Injection

IFB

1.8

3.3

Load

Casc

RowENB

ColENB

RAMWrEn

1/2/4/8

2cm line – current output

Collecting Nwell – diode biased
Half comparator

- The threshold is only used locally at the periphery
- Matching is done at the periphery as well
- Mostly current is carried to the periphery, avoiding long line charging effect
Pixel geometry – 630µm x 40µm

Amplifier.
Half comparator.
RAM controlled -
- charge injection
Row/Col selection

Trim RAM
Trim DAC

6 connected NWELLs
50% diode fraction
P-contact around each NWELL
120V rules
Response curve and Gain - simulated
Signal to Noise Ratio - simulated

![Graph showing Signal to Noise Ratio (SNR) vs Charge in fC for MIP 20ohms and 600ohms.](image)
Capacitance NWELL to dynamic nets

Shield to the NWELLs has been added for all dynamic nets

Dynamic net: **half comparator output**
- Parasitic capacitance from the half-comparator output net to nwells = 1.32fF
- Dynamic signal on the half-comparator output net ~25mV
- Charge injected by the half-comparator to the subsequent pixels: 200e-

Dynamic net: **charge injection signal**
- Parasitic capacitance from the charge injection to the nwell : 82aF
- Real capacitance for the charge injection signal: 2.3fF
- SNR of the charge injection signal = 28
CHESS periphery

Comparator latching

Hit encoding

1/2 Hit Latch

Ck Hard reset

Prog. reset

HitPrev HitNext

Hard coded pixel address

5 bit hit address
1 bit hit to encoding

1 bit hit flag

Sel

Hit Flag Logic

x32

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Principle behind Hit encoding in the strip

<table>
<thead>
<tr>
<th>Hit</th>
<th>Prev</th>
<th>Encoded</th>
<th>Flag</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Logic functions:

Prev = \((\text{Prev}_{-1} \text{ OR Hit})\)

Encoded = \((\overline{\text{Hit}} \text{ NOR Prev})\)

Flag = \(\text{Flag}_{-1} \text{ OR (Hit NOR Prev)}\)

The **Encoded** signal controls sending the bits to the periphery.

Both encoding and flag raising is completed in less than 6ns.
Hit Encoding – Strip Encoding

1 hit per strip + flag in case of multiple hits. 5 + 1 bit
8 hits maximum per 128 strips. 7 bit
Overflow protection in 3b adder: 8 hits maximum
Adder value used to multiplex data on 8 buses
Hit selection – Scalable to 512 strips

Worst case speeds

- Add: 500ps
- Skip: 150ps
- Bit line settling: 800ps
- Write memory: 300ps

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Data serialization

8 x 13 1bit Parallel In Serial Out cells.

Parallel input with 25ns period (synchronized to the 40MHz external clock).

Serial Output has 3.125ns period (synchronized to the 320MHz external clock).

DATA_VALID necessary to distinguish the ‘no hit’ case.
Serializer memory contents:

- Internal Data Valid bit
- Multiple hit flag
- msb
- column address (5 bits)
- lsb
- lsb
- strip (row) address (7 bits)
- msb

Output waveforms:

- Outs<0>
- Outs<1>
- Outs<2>
- Outs<3>
- Outs<4>
- Outs<5>
- Outs<6>
- Outs<7>
- Outs<8>
- Outs<9>
- Outs<10>
- Outs<11>
- Outs<12>
- Outs<13>

Clock (320 MHz)

Col addr
Row addr

mean 0
mean 1

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Hit Encoding/Serializer Simulation – RCX
CHESS2 timing

The data is pipelined with a 4 bunch-crossing delay.
Internal buffer between each stages.
The 40MHz clock is propagated along with the data in the add & skip and to the serializer block to prevent sampling errors.
LVDS Driver

*Schematic simulated at all condition (wo,wz,ws,wp) at room temperature.*

<table>
<thead>
<tr>
<th>Specs</th>
<th>Typical</th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Differential Input Voltage (@ RLOAD =100Ω)</td>
<td>600mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Common Mode</td>
<td>1.2V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Current</td>
<td>3mA*</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Speed</td>
<td>320MHz</td>
<td>500MHz</td>
<td></td>
</tr>
<tr>
<td>Supply</td>
<td>3.3V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*Can meet standard LVDS requirements.*
SLAC ASIC Control Interface (SACI)

Serial Interface with handshake protocol

5 Signals
- 3 shared: saciClk, saciCmd, saciRsp.
- 1 dedicated select line per slave: saciSelL.
- 1 Reset Line (RstL) can be shared with the ASIC Global Reset.

- Operated between 0V and 3.3V
- Allows multiple SACI on same bus (parallel mode).
SACi – Control unit

- SACI Core
- ADDRESS Buffer
- CMD, CLK Buffer
- DATABUS Buffer
- SACI System
- Rad Hard Register
- Rad Hard Bits
- Logic
- Command Logic
- Command Decoder
- Bus to ASIC
- Internal Bus
- DataBus to Matrix
- Pixel Write
- Bits
- Row Logic
- Col Logic
- Pixel Write DataBus to Matrix
- Buffers
- Bus to ASIC
- Internal Bus

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# Global Register Map

The registry store the ASIC configuration settings needed for the DACs and the control unit.

Radiation tolerant register.

The registers are set to properly bias CHESS2 upon start-up.

<table>
<thead>
<tr>
<th>Address</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
</tr>
</thead>
<tbody>
<tr>
<td>DAC0</td>
<td>0</td>
<td>DAC2</td>
<td>0</td>
<td>DAC4</td>
<td>0</td>
<td>DAC6</td>
<td>0</td>
<td>DelEXEC</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>DAC0</td>
<td>1</td>
<td>DAC2</td>
<td>1</td>
<td>DAC4</td>
<td>1</td>
<td>DAC6</td>
<td>1</td>
<td>DelCCKreg</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>DAC0</td>
<td>2</td>
<td>DAC2</td>
<td>2</td>
<td>DAC4</td>
<td>2</td>
<td>DAC6</td>
<td>2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DAC0</td>
<td>3</td>
<td>DAC2</td>
<td>3</td>
<td>DAC4</td>
<td>3</td>
<td>DAC6</td>
<td>3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DAC0</td>
<td>4</td>
<td>DAC2</td>
<td>4</td>
<td>DAC4</td>
<td>4</td>
<td>DAC6</td>
<td>4</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DAC0</td>
<td>5</td>
<td>DAC2</td>
<td>5</td>
<td>DAC4</td>
<td>5</td>
<td>DAC6</td>
<td>5</td>
<td></td>
<td></td>
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<tr>
<td>DAC1</td>
<td>0</td>
<td>DAC3</td>
<td>0</td>
<td>DAC5</td>
<td>0</td>
<td>DAC7</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DAC1</td>
<td>1</td>
<td>DAC3</td>
<td>1</td>
<td>DAC5</td>
<td>1</td>
<td>DAC7</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DAC1</td>
<td>2</td>
<td>DAC3</td>
<td>2</td>
<td>DAC5</td>
<td>2</td>
<td>DAC7</td>
<td>2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DAC1</td>
<td>3</td>
<td>DAC3</td>
<td>3</td>
<td>DAC5</td>
<td>3</td>
<td>DAC7</td>
<td>3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DAC1</td>
<td>4</td>
<td>DAC3</td>
<td>4</td>
<td>DAC5</td>
<td>4</td>
<td>DAC7</td>
<td>4</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DAC1</td>
<td>5</td>
<td>DAC3</td>
<td>5</td>
<td>DAC5</td>
<td>5</td>
<td>DAC7</td>
<td>5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Spare bits</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

![Table Diagram](image-url)
Hit encoding
8 Hit encoding logic

8 Hits selection
Hit Memories
SACi – Registers – Current sources

SACi & Current sources
Output memory – Serializer – LVDS pads
Conclusions

CHESS2 is a full reticle demonstrator strip sensor in a High Voltage CMOS technology.
– CHESS2 uses the advantage of CMOS process to fully encode hits for all the pixels.
– The encoding is fully synchronous at 40MHz but lossy with a maximum of 8 hit/strips.
– The reticle houses 3 independent array of 128 strips each.

The advantage of the CMOS technology is to:
– Reduce the number of wire-bonds needed therefore handling costs.
– Reduce the detector capacitance
– Reduce the material budget of the detector.

In addition CHESS2 improves by a factor 2 the resolution of current baseline sensor in r-phi and z.
Acknowledgements

We want to acknowledge for the work on CHESS the contribution of all the people involved in design, test and characterization of the devices.

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BACKUP
Pixel dimensions and layout

6 connected NWELLS: 24.3µm x 80.2µm – 53.3% coverage

120V design rules

No inter-wells substrate contacts

Diode biased with external supply
HV contact in blue around pixels

No contacts added here
Pixel ground distribution
Ground mesh - detail
Ground mesh – all pixels
Ground connection strategy

Resistance in the mesh is ~20mOhm across each 630µm column -> 2.4mV drop

2.5mm – 26 connection
0.1Ohms
10mV drop @ 100mA

Ground bus added next to pads
Number of rad-hard NMOS - Pixel part

<table>
<thead>
<tr>
<th>Component</th>
<th>Total NMOS RAD_SOFT</th>
<th>Total NMOS RAD-HARD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixels</td>
<td>0</td>
<td>114688</td>
</tr>
<tr>
<td>Comparator periphery</td>
<td>0</td>
<td>67840</td>
</tr>
<tr>
<td>Latching</td>
<td>0</td>
<td>65408</td>
</tr>
<tr>
<td>Column selector</td>
<td>952</td>
<td>0</td>
</tr>
<tr>
<td>Column selector periphery</td>
<td>403</td>
<td>0</td>
</tr>
<tr>
<td>Row selector</td>
<td>1427</td>
<td>0</td>
</tr>
<tr>
<td>Bias</td>
<td>1134</td>
<td>255</td>
</tr>
<tr>
<td>Total</td>
<td>3916</td>
<td>248191</td>
</tr>
</tbody>
</table>

These numbers for 128 strips. Need to be multiplied by x3
~4mA of leakage current on the digital supply - ok
Programmability and Debug Mode

- Matrix and Hit Encoding clock sync fine tuning
  - 4 Bits (400ps Step -> Max 6ns)

- Hit Encoding pipeline timing optimization
  - The write and reset phases length of the two stages of the hit encoding can be independently programmed

- Hit Encoding Test Mode

- LVDS TX Adjustable current

- LVDS RX
  - AC Mode
  - Different input impedance (100 Ω – 300 Ω)
## Number of rad-hard NMOS Digital Back-end

<table>
<thead>
<tr>
<th></th>
<th>NMOS RAD SOFT</th>
<th>NMOS RAD HARD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control Unit</td>
<td>2954</td>
<td>2688</td>
</tr>
<tr>
<td>Hit Encoding</td>
<td>0</td>
<td>38463</td>
</tr>
<tr>
<td>Serializer + Buffer</td>
<td>0</td>
<td>2059</td>
</tr>
<tr>
<td>LVDS TX/RX</td>
<td>103</td>
<td>0</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td><strong>3057</strong></td>
<td><strong>43210</strong></td>
</tr>
</tbody>
</table>
CHESS2: Serializer

- 8 x 13 1bit PISO Cell.
- Parallel input with 25ns period (synchronized to the 40MHz external clock).
- Serial Output has 3.125ns period (synchronized to the 320MHz external clock).
Dynamic Hit Latching

Dynamic comparator output resynchronization on the 25ns clock.

25ns clock pumping: no high Z node for more than 12.5ns.
Hit Flag Logic

Simple asynchronous propagating logic to raise the Flag in case of additional hit in the strip.

Schematic has been optimized to use a minimum of NMOS as they require more space.

Not a dynamic cell: no high Z nodes.

Both encoding and flag raising is completed in less than 6ns.