Development of SOI monolithic pixel sensors

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Advanced pixels
10:50-12:30
Outlines

Introduction (features, process summary, MPW)
Current issues (radiation tolerance, crosstalk)
1. Radiation tolerance
   - Double SOI (Tr. Test and Integration-type pixel sensors)
2. Crosstalk reduction
   - Double SOI (counting-type pixel sensors)
Pixel size reduction technique (counting-type pixel sensors)
Status of 3D chips
Summary
Japan Grant-In-Aid (FY2013-FY2017)

Imaging of Elementary Particle Origin of Mass by Higgs Particle

micron Accuracy 2mm

128x128 (目標) 1.8K Operation

Far Infra Red Evolution of Stars

Harsh Environment

Precise Time Resolution

SOI

XFEL femto Second 1nm Resolution

Exploration of Primitive Black Holes

Distant X-ray Background Reduction

3D Structure of a Cell

Imaging Mass Spectrometer Rapid Analysis

Au Nano Particle $\Delta x = \sim 10$ nm

100 nm
SOI Monolithic pixel sensor

SOI=Silicon on insulator

The features of SOI monolithic pixel sensor

• No mechanical bump bonding. Fabricated with semiconductor process only
• Fully depleted (thick / thin) sensing region
  with low sense node capacitance (~10 fF@17 μm pixel) → high sensor gain
• SOI-CMOS; Analog and digital circuit can be closer → smaller pixel size
• Wide temperature range (1-570K)
• Low single event cross section
• Technology based on industry standards; cost benefit

Targets
High-Energy Physics
X-ray astronomy
Material science
Non-destructive inspection
Medical application

SOI=Silicon on insulator
# Process Summary

| Process (Lapis Semiconductor Co. Ltd.) | 0.2µm Low-Leakage Fully-Depleted (FD) SOI CMOS  
1 Poly, 5 Metal layers (MIM Capacitor and DMOS option)  
Core (I/O) voltage : 1.8 (3.3) V |
|--------------------------------------|---------------------------------------------------------------------------------------------------|
| SOI wafer (200 mm φ =8 inch)         | Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick  
Buried Oxide: 200 nm thick  
Handle wafer thickness: 725 µm → thinned up to 300/500 µm (Lapis) or ~50 µm (commercial process)  
Handle wafer type: NCZ, NFZ, PCZ, PFZ, double SOI(DSOI) |
| Backside process (2011~)              | Mechanical Grind → Chemical Etching → Back side Implant → Laser Annealing → Al plating |
KEK MPW run

- KEK organizes MPW runs once (FY2014-) or twice a year
- Mask is shared to reduce cost of a design
- Including pixel detector chip and SOI-CMOS circuit chip

MX1786 (FY14-1)

MX1850 (FY15-1)
Current issues

1. Additional pixel process
2. Double SOI (DSOI) wafer
Various Implantation Options in Sensor part and DSOI

P/n various doping density

DSOI STEM image

Top SOI: SOI-CMOS

- Shield the back gate effect
- Reduce sensor-circuit crosstalk
- Compensate the TID effect

* BOX thickness 145nm
* SOI1,2 thickness: to be asked (confidential)
Radiation tolerance study

- TEG

- Integration-type pixel sensors INTPIXh2 (chip size 6 x 6 mm)

Gamma-ray (Co-60) irradiation test by Univ. of Tsukuba

K. Hara et al., ”Initial Characteristics and Radiation Damage Compensation of Double Silicon-on-Insulator Pixel Device,”, PoS(VERTEX2014)033.
FET threshold shifts and compensation in DSOI

IV curves of an NMOS (2MGy irradiated) with Changing VDSOI2

Residual of Vth shifts of various FET types (FETs grouped into 3 in VSOI2 setting)

Transistor IdVg curve was recovered when applying negative voltage at SOI2
N-type DSOI pixel sensor (INTPIXh2)

Response to infrared laser of 1064 nm wavelength and 10 ns pulse duration.

The pixel images after 100 kGy (10 Mrad) could not obtain but recovered with VSOI2=-10V.

The average ADC count as a function of the square root of the bias voltage for sensor. Obtained similar linearity and sensitivity to pre-irradiation with VSOI2=-10 V.

S. Honda et al., TIPP2014, 2-6 June 2014, Amsterdam
Integration-type p-type DSOI sensor - INTPIX8 (FY14-1)

FY14-1 MX1786
18 x 12 mm chip
1024(H) x 640(V)
16 (x 64ch.) parallel output
16 um pixel size

Active layer (blue)
PS2(mid. SOI contact)
P- substrate
BNP(p-stop)
(floating)
N+
bnw
Soi2 for DSOI

Pixel layout 16 x 16 um
Am-241 spectrum by p-type DSOI INTPIX8

* G0,G1 ON

VDD18  VDD33
GND

LOAD  STORE
G0  G1
RST

V_RSTCDS  Vcds
CDS  READ
OUT

-50deg.C
Vdet=-200V
T_integ=0.5ms
4000 frames

* Gain correction for each pixel
Is not done

Vcds set value
=700V

Gain
47μV/e-

Readout Noise
70e-@-50deg.C

* The numbers are Preliminary

Full pixel

Gain correction
for each pixel
Is not done

X-ray spectra were obtained using the DSOI sensor

* IIN1=10μA, IIN2=7μA, IINABUF=36μA

5clusters only
(Just showed as reference)
Status of Counting-type pixel sensors

- Sensor – circuit crosstalk study
  CPIXTEG3b (KEK & IHEP)

Yunpeng Lu et al.,
“First results of a Double-SOI pixel chip for X-ray imaging”
NIM A (in press)

- Reduction of Pixel size (future plan)
Counting-type pixel sensors (cntpix,cpix…)

- Area of the 15 bit counter is large (∼30 x 50)
  → Area reduction: share nmos and pmos active area
- Counter didn’t work due to the crosstalk in a single SOI
Sheet resistance is high ~ $10^4$ Ohm/sq (depends on voltages)
SOI2 contacts should be put much
Pickup of digital switching

- Counter driven by external clock as a source
- 5mV @ shaper output for Double-SOI chip
  - 74 e⁻ referred to input charge
  - Submerged in noise floor (ENC ~ 113e⁻)
- 95mV for Single-SOI chip
  - ~3770e⁻ referred to input charge
Idea of pixel size reduction

New D Flip-Flop
Share active region and contacts of PMOS and NMOS
Area \( \sim \frac{1}{4} \)

Evaluation test will be done
FY2016 chips

\[ 12 \times 7 = 84 \text{um}^2 \]

\[ 3.3 \times 6.3 = 20.79 \text{um}^2 \]
A gold (Au) cone bump formed by nanoparticle deposition

3-um-diameter Au cone-bump connections with adhesive injection

Pixel 2014 proceedings  
M. Motoyoshi et al.
Status of 3D chips (2/2)

The 2nd prototype chip (MX1542)

Daisy-chain output

MPW12-1 (MX1542)
3DTEG KEK/LBNL/Hokkaido Univ.
(Include 10um pixel)

~1000 micro bump connection was successful
Edit DRC/LVS rule for 3D chips and submit new design (MPW FY16)
Summary and future plan

SOI pixel sensor development since 2005
Some application plans are ongoing

Current issues:
The back-gate effect is suppressed by the BPW process or double SOI
Radiation hardness can be improved with double SOI, and … (ongoing study)
Crosstalk issue can be solved utilizing double SOI

Suggestion in reduction of pixel size
3D bump connection between 2 SOI chips was successful

Future plan:
- Continue various application studies using existing SOI sensors
- Develop new SOI detectors for various applications
- Double SOI counting-type pixel sensors with a small pixel size (~50 x 50 um)
- High radiation tolerance study
- 3D integration SOI sensor development