A High Dynamic Range Pixel Readout in a Si-Ge Process

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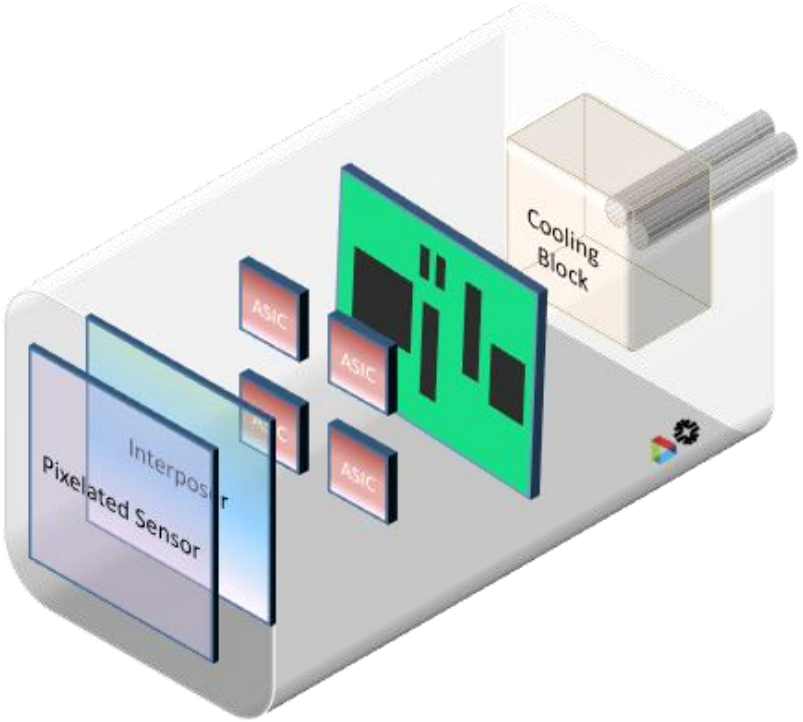
FASPAX: Fermi-Argonne Silicon Pixel Array X-ray detector

- New regime in area detectors:
  X-ray camera beyond the dynamic range of a CCD, sensitivity of a photon counting detector, and:
  - un-matched burst image rate (~13 MHz),
  - large, fully active (seamless) area (15x15 cm^2),
  - small pixel size (100x100 μm^2) for 2.2M pixels

- Enabler of science for studies of irreversible processes, time-resolved or high flux applications and high speed imaging (DCS)

- Approach uses 3D integrated technology to provide seamless, wafer-scale detector; interposer adapts sensor pixel to ASIC pitch; ASICs in SiGe process, bump-bonded to interposer; 500 μm thick Si X-ray detector

- New front-end concept: single - 10^5 photon per image capability in small pixel footprint



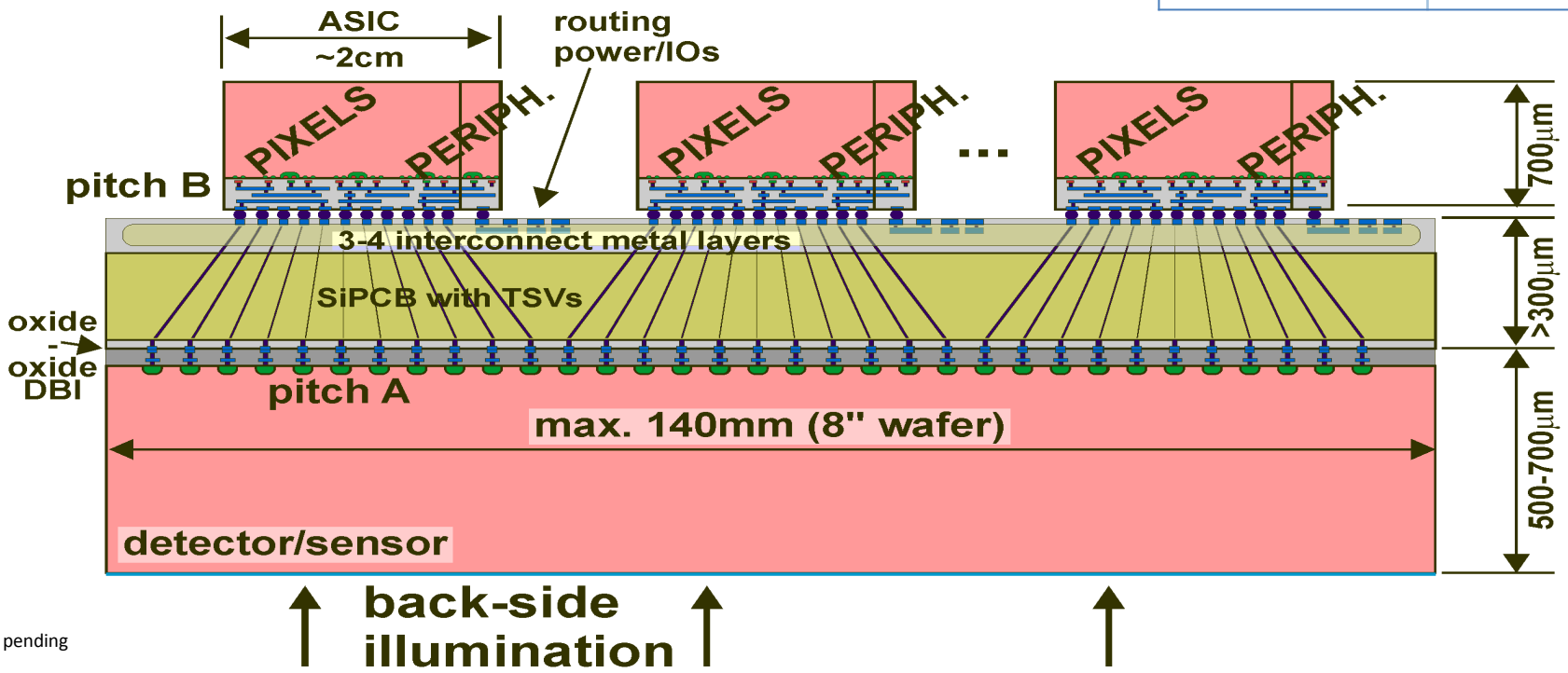
Expanded view of X-ray camera

The proposed camera has a fast frame rate, five orders of magnitude dynamic range and small pixel size on a seamless fully active wafer scale detector. It exceeds the capability of any existing X-ray detector and enables a rich science program

Back-Illuminated X-Ray Detector

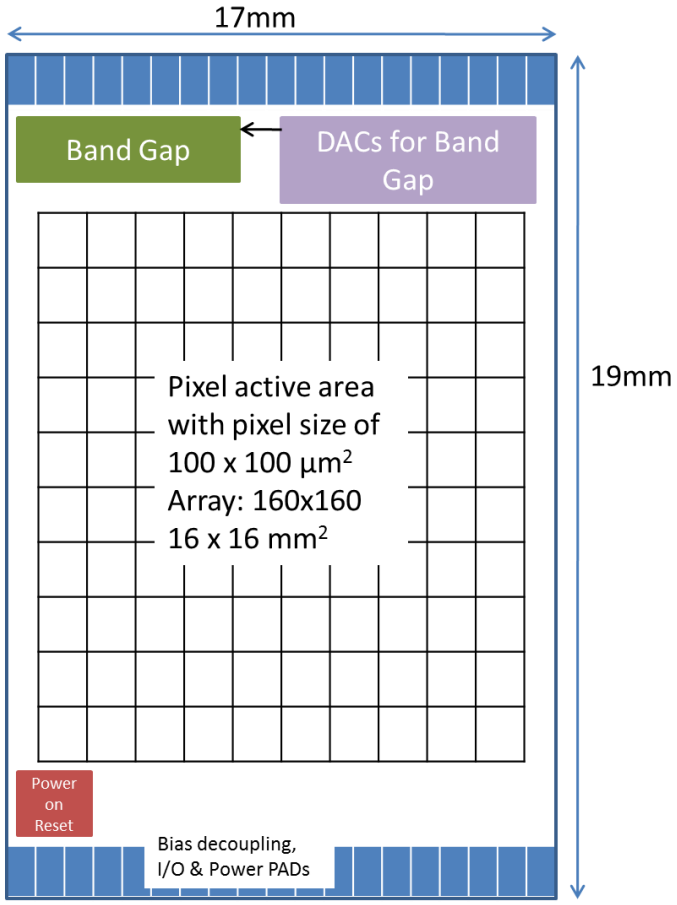
- Versatile, fast integrating area detector:
  - MHz burst frame rates will record high-resolution movies of microsecond phenomena
  - Flexible dynamic range: on per pixel basis, gain for integrated signal – from single photon to 10^5 photon/pixel

Parameter	Value
Pixel size	100x100 μm²
Buffer depth	24 – 256
Range	1 – 10^5 γ's
Detector area	~15x15 cm²
Frame Rate	13 MHz
Well depth	1fC – 100 pC
Si Thickness	500-700 μm

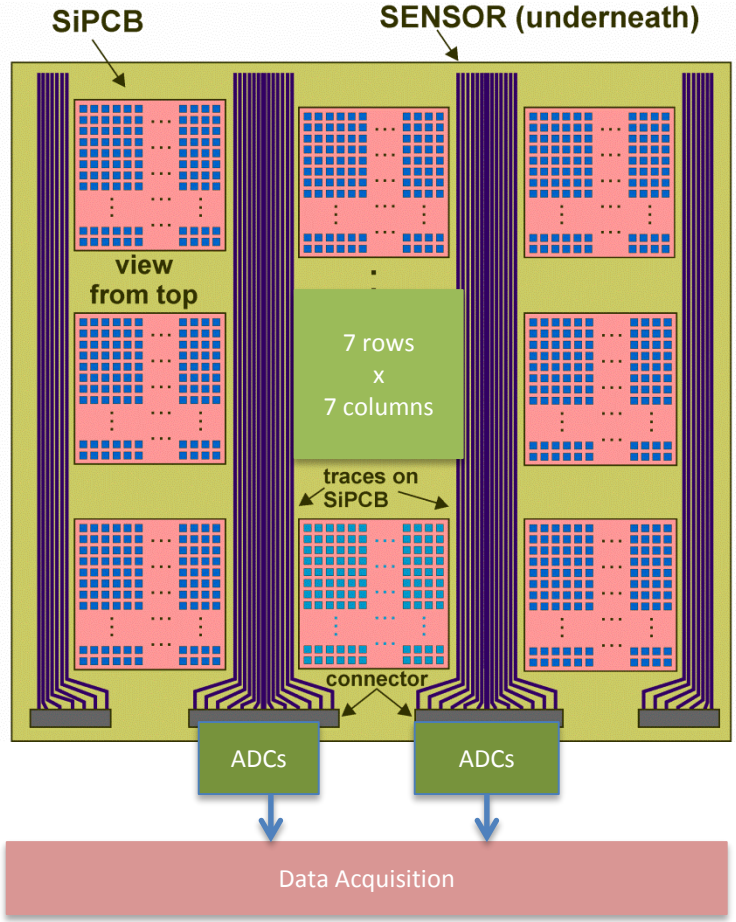


Patent pending

Final Goal:
ASIC and Si/ Glass PCB Floorplan



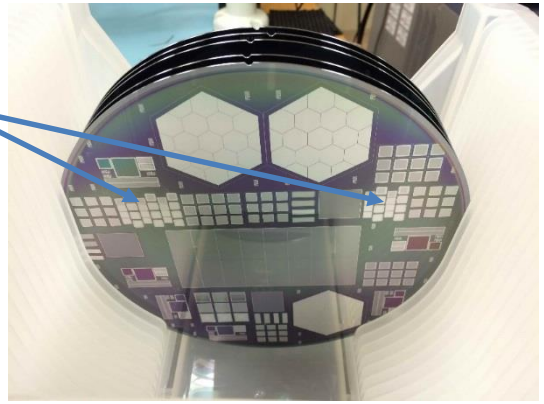
As an example, with a detector pitch A of 125µm x 125µm, and a pixel array of 160 x 160, the total area is 20mm x 20mm. This area needs to be tapered to 100µm x 100µm with a total active area of 16mm x 16mm and an ASIC size of 17mm x 19mm. (Reticule size is approximately 18mm x 20mm)



E.g. The vertical and horizontal space between ASICs would be 1 mm and 3 mm, respectively. The horizontal space would be used for routing power and analog signals from the ASIC to the connector
Wafer Size approx. ~ 14cm x 14cm; no. of ASICs on wafer 7x7 array (49)

Sensor R&D

First prototype n-in-p devices (on shared wafer), suffered guard ring breakdown at ~130V. Revised designs currently being fabricated.



- Investigating three types of devices:
  - N-in-p silicon
  - N-in-n silicon
  - CdTe (from Acrorad)
- Plasma effects are a possibility at the limits of FASPAX dynamic range, so silicon devices are being optimized to tolerate a bias of 1 kV.
  - Fabricating series of prototype devices guided by Silvaco simulation.

General Parameters of the prototype sensor	
Charge species	electrons
Operating bias	1 kV
Pixel pitch	100 μm x 100 μm (125 μm x 125 μm)
Size of prototype devices	32 x 32 pixels
Thickness	500 μm - 700 μm

FASPAX project effort includes:

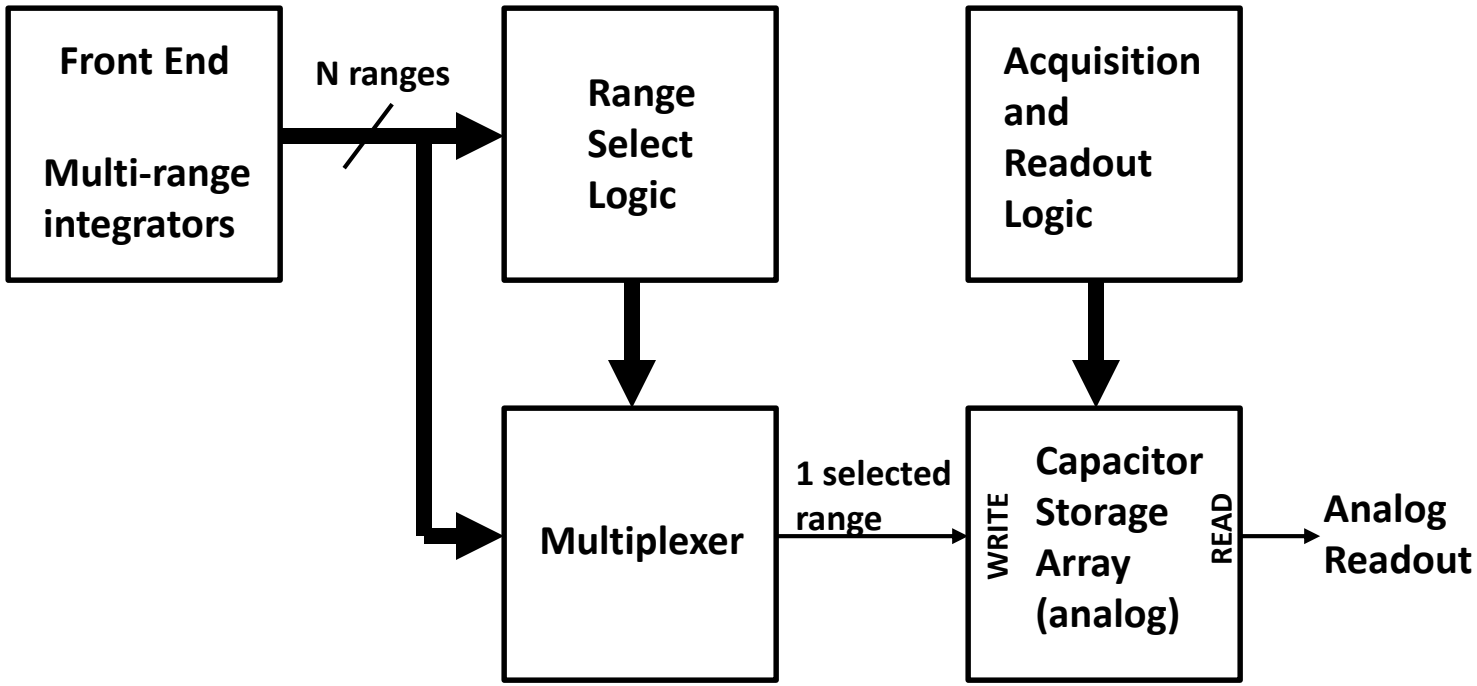
- Small sensor
- ASIC
- Interposer assembly
- Data acquisition system

This talk addresses the ASIC design effort 

Design requirements for the FASPAX pixel

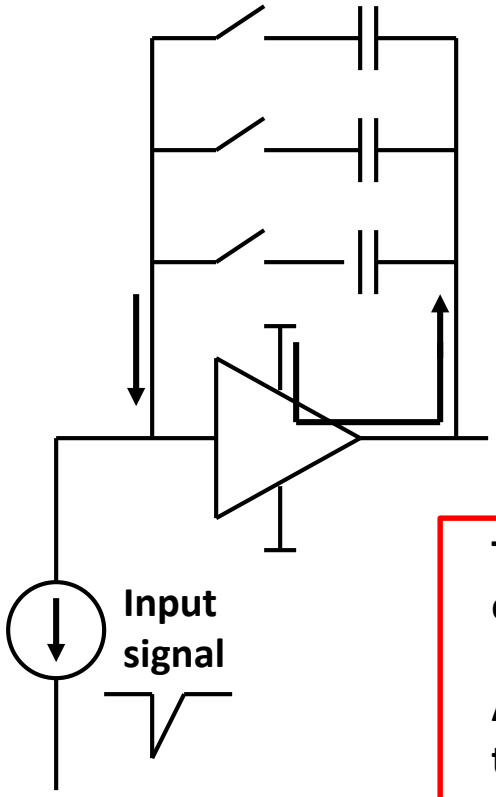
- Single photon sensitivity (resolve signal of ~ 2000 e, 0.3 fC)
- Dynamic range of at least 10^5 (signals of ~ 0.3 fC to 50 pC (max)
- Pixel area 100u X 100u
- 13.3 MHz signal burst rate (75 ns)
- “Low” input impedance to absorb fast input signals
- Storage of at least 48 samples for subsequent analog readout
- Readout of all pixels on a chip in < 10 ms
- “Low” power dissipation
- Robust design that is insensitive to bussing parasitics, power supply values, biasing variations, common mode noise, etc.

Solution: multiple-range charge integrating pixel



One of the biggest challenges: integrating 50 pC in a 100u X 100u pixel

An existing technique –
adaptive gain active integrator:



The problem: integrating 50 pC requires a total feedback capacitance of 50 - 100 pF. In a 100u X 100u pixel…*no!*

Also required would be a large and fast current transient from the supply and amp to actively source 50 pC (~5-10 mA peak)…*no!*

Requires a new approach!

A new approach for pixels: use a version of the "QIE" (Charge Integrator and Encoder) technique. QIE chips have been successfully employed in HEP experiments for years.

- **Split the input signal into multiple scaled ranges with an NPN current splitter (NPN split ratios are constant over a wide range! – not so with MOS)**
- **Incorporate the current splitter into a feedback amplifier to provide low input impedance and good bandwidth**
- **Shunt away ("dump") large signal currents from the more sensitive ranges**
- **Feed the current splitter outputs to passive integrators of small size**
- **Voltage buffer the integrators to drive an analog storage cap array**
- **Range decision logic to pick one relevant range per integration to store**

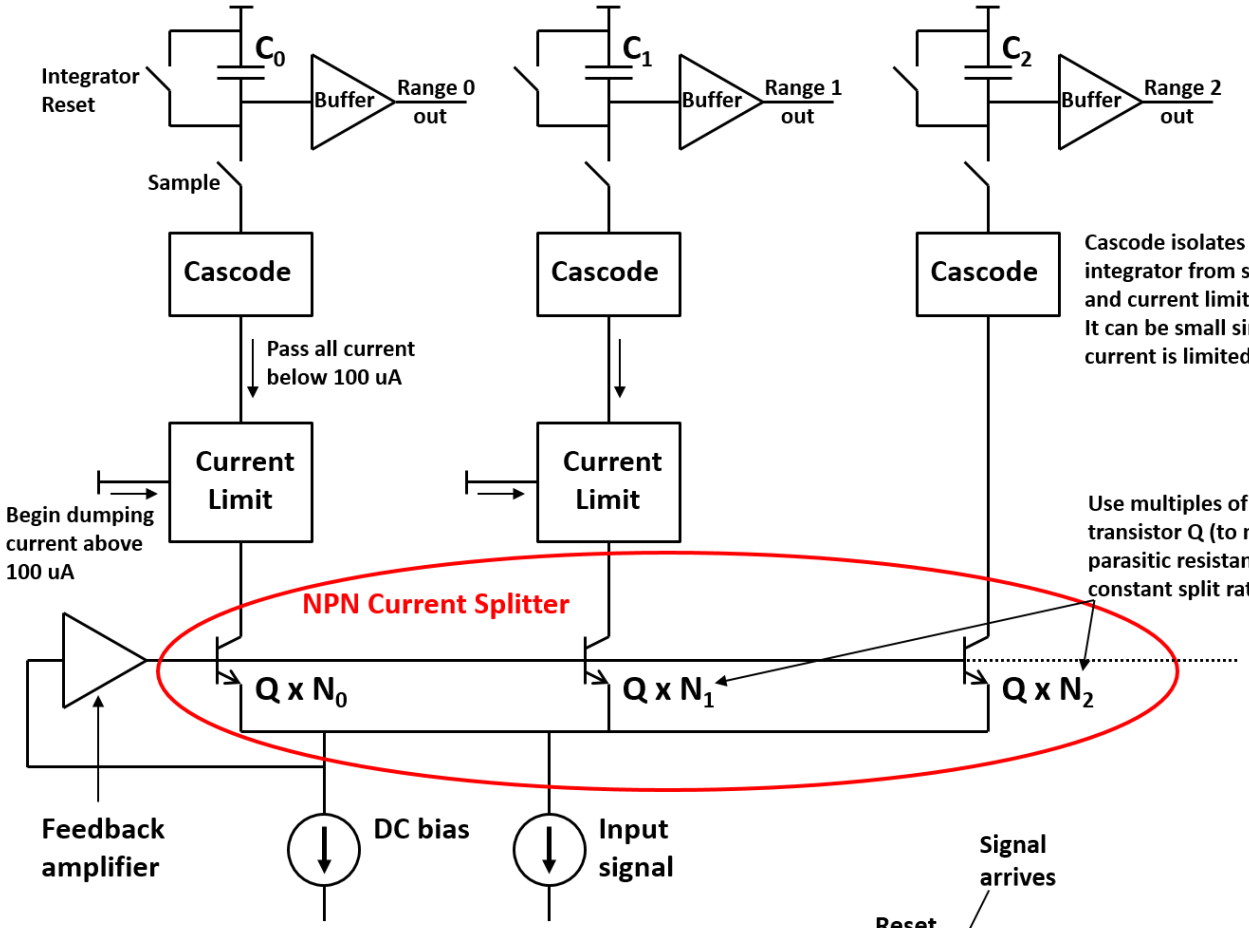
Advantages of this approach:

- **No big capacitors are required!**
- **Active sourcing of an image charge is not required (the signal itself does the work)**
- **Simplicity, fairly easily implemented in a small area pixel**
- **No "adaptive gain" switching is necessary during the integration period – all ranges integrate different fractions of the signal, and the desired range is chosen after integration is complete**

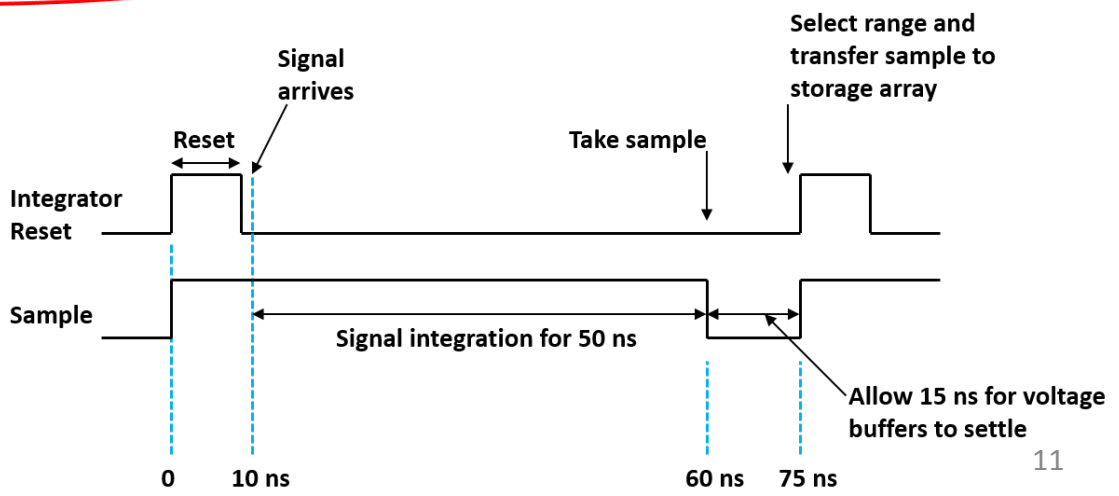
A challenge with this approach:

- **DC bias current is required for the splitter, which is integrated with the signal. This adds common mode levels to the signals, and adds shot noise! Minimize bias current while maintaining speed.**

Generalized approach for front end design (N ranges, 3 are shown here)



The overall range scaling depends on the splitter NPN ratios and the integrating capacitor ratios



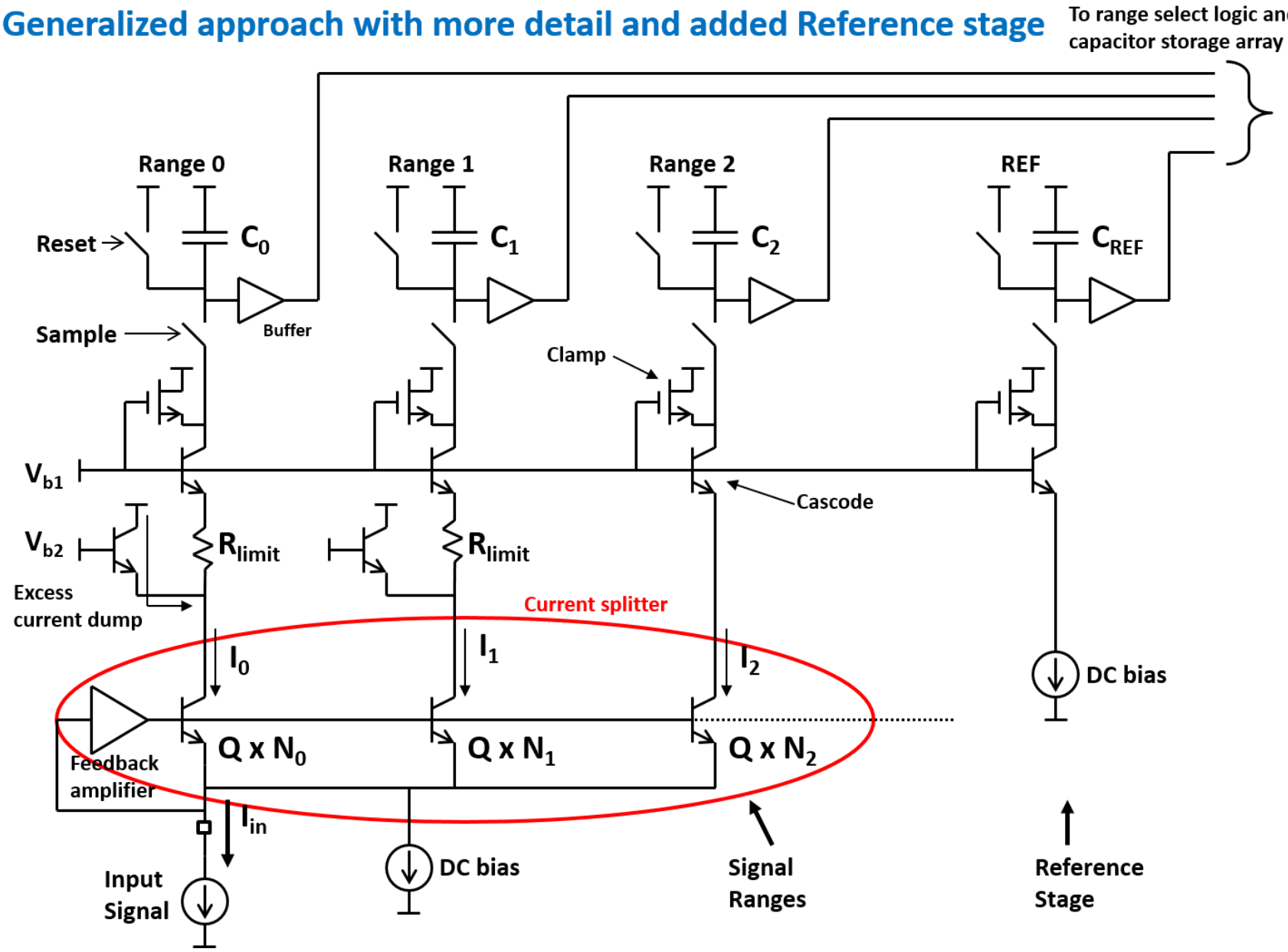
Vulnerabilities of this configuration:

- **DC bias current adds to the signal ("common mode" offset)**
- **Common mode is sensitive to integration time jitter, supply voltage, temperature, etc.**

The solution employed by QIE chips: add a "Reference" stage

- **Add a Reference integrator that is "identical" to the most sensitive range integrator**
- **Integrates just the bias current (no signal)**
- **Forms a pseudo-differential system**
- **Store and read out the Reference stage along with the signal readout**
- **Pseudo-differential readout tends to cancel out common mode-effects**
- **Very successful technique in QIE chips**
  - **Extremely stable pedestal**
  - **Insensitive to process variations, supply voltage, integration time….**
- **Price to pay:**
  - **Increase in noise (both Signal and Reference stages contribute)**
  - **Increase in real estate (area)**

Generalized approach with more detail and added Reference stage



Some problems with the generalized approach so far:

If the integrating capacitor values and bias currents differ range-to-range, then the integrator voltage space is different for each range.
Also, the benefit of the pseudo-differential configuration in cancelling common-mode effects is limited to only the most sensitive range!

The FASPAX design approach:

Make all integrating capacitors equal and small, and insure equal bias currents in all ranges

This also helps keep the cap layout area small!

↓

All range scaling must therefore be done with splitter NPN ratios

↓

Minimize the number of ranges. 3 ranges with scale factors of x32 needed to cover the whole dynamic range

↓

But all scaling done in the input splitter requires too many NPNs! Incorporate a 2nd splitter in the cascode of the 3rd stage.

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Add bias currents where needed so that each integrator sees the same DC current

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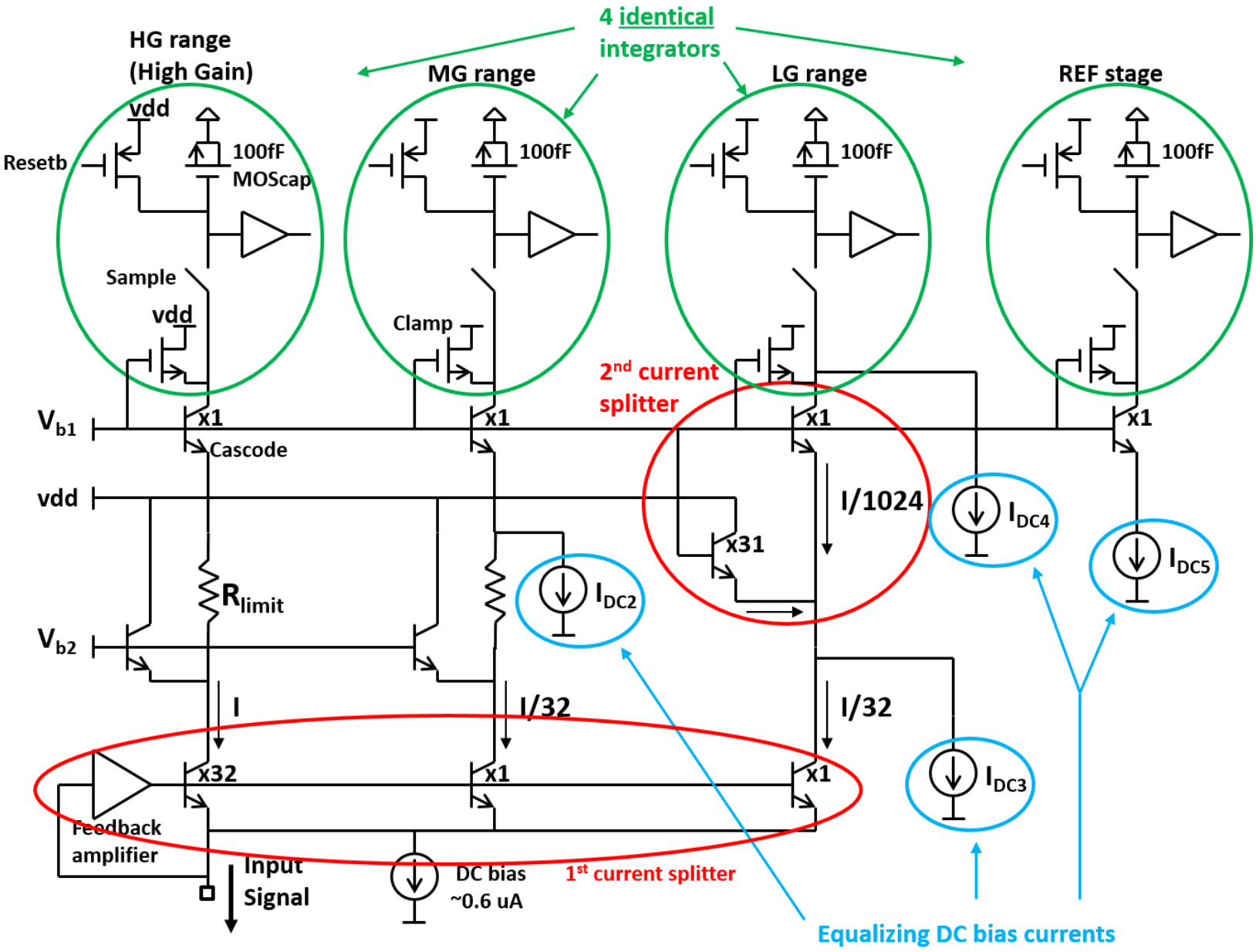
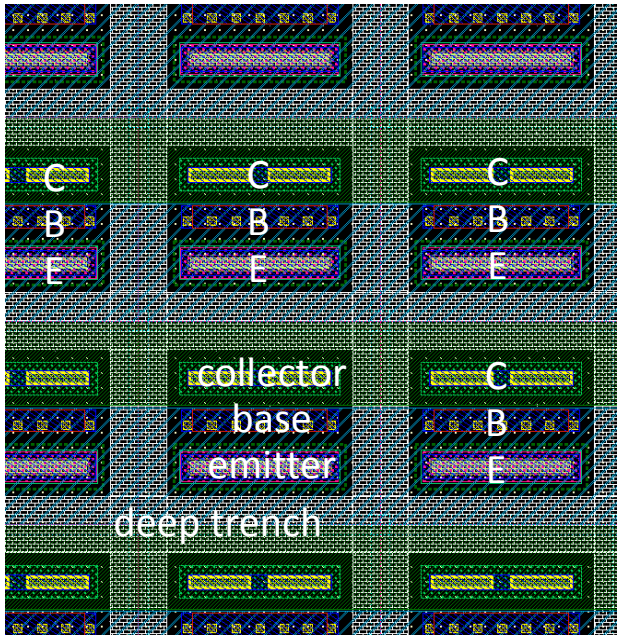
The Reference stage now cancels common mode effects on all ranges!

Specific FASPAX implementation

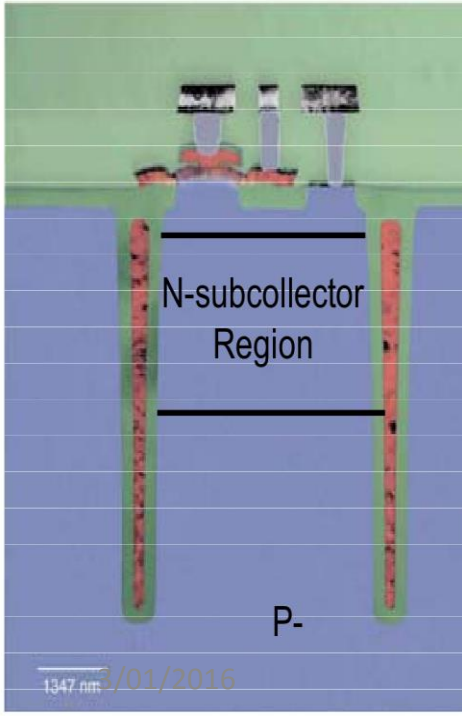


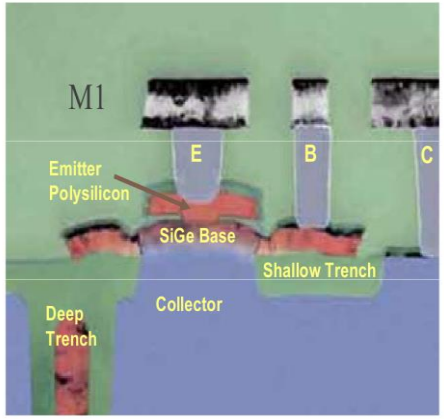
Process chosen: 130nm SiGe BiCMOS8HP

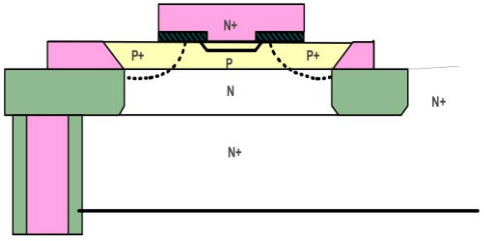
- Offers high-performance SiGe hetero-junction bipolar npn (self-aligned emitter) at moderate cost
- Small feature size, fast, low power CMOS.
- Single and dual gate MOS
- 8 metal layers, thick redistribution top layers
- High-density capacitors
- Good substrate isolation



Layout of adjacent BJTs sharing the lateral deep trench







- Deep (6um) trench isolation all around the collector → low sidewall capacitance and increased substrate isolation
- Not possible to share collectors, but **<u>sharing of the trench between adjacent BJTs is allowed – area efficient!</u>**
- Fixed emitter width (W=0.12µm)
- Peak f_T=200GHz β_{MAX}=600

MIM caps are available in this process, but…. even with relatively small values they still take a fair amount of room AND disrupt the upper levels of metal routing. AVOID MIM CAPS! Use MOS caps instead.

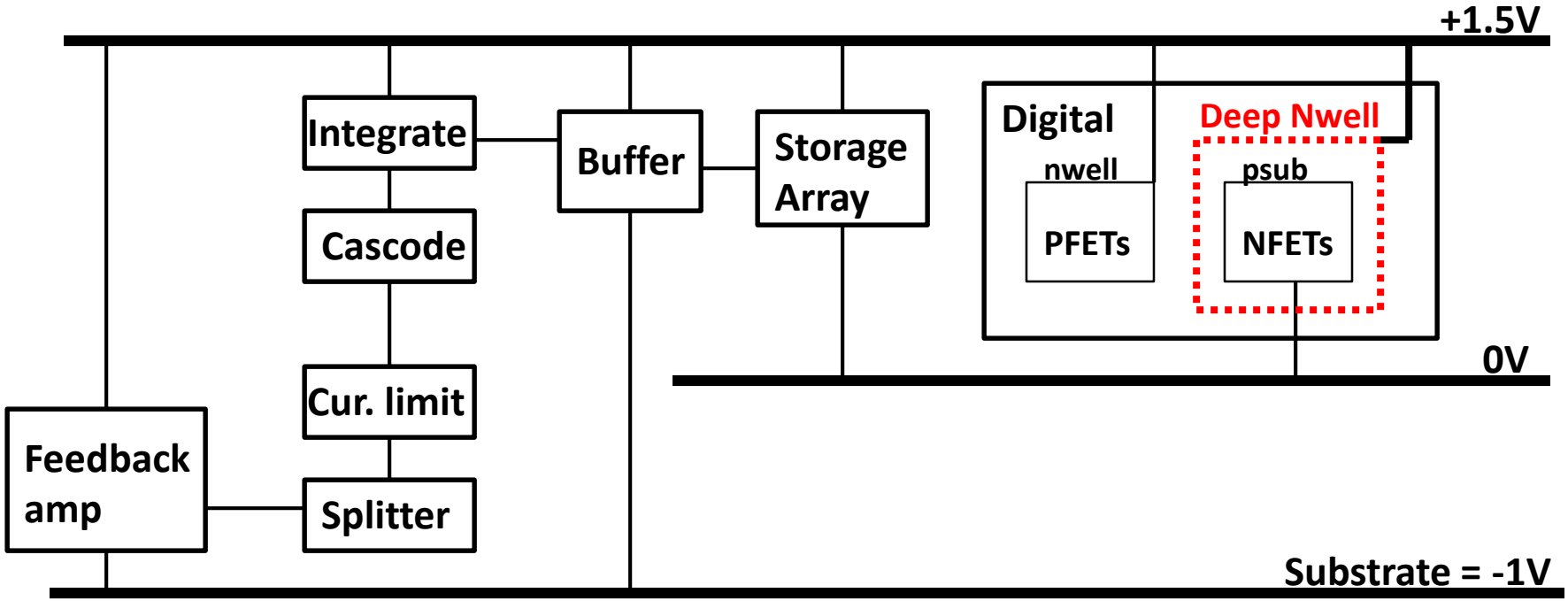
1.5V process – the FASPAX chip digital logic should operate between 0 and 1.5V.
However, 1.5V is not enough headroom to stack the splitter, current limiter, cascode, and integrator!

How to get enough analog headroom?

Component ratings
NFET, PFET: 1.5V max. across any 2 terminals (including substrate)
DGNFET, DGPFET: 2.5V max. across any 2 terminals (including substrate)
NPN: Vce < 1.5V, Collector-substrate < 20V
Deep Nwell available!

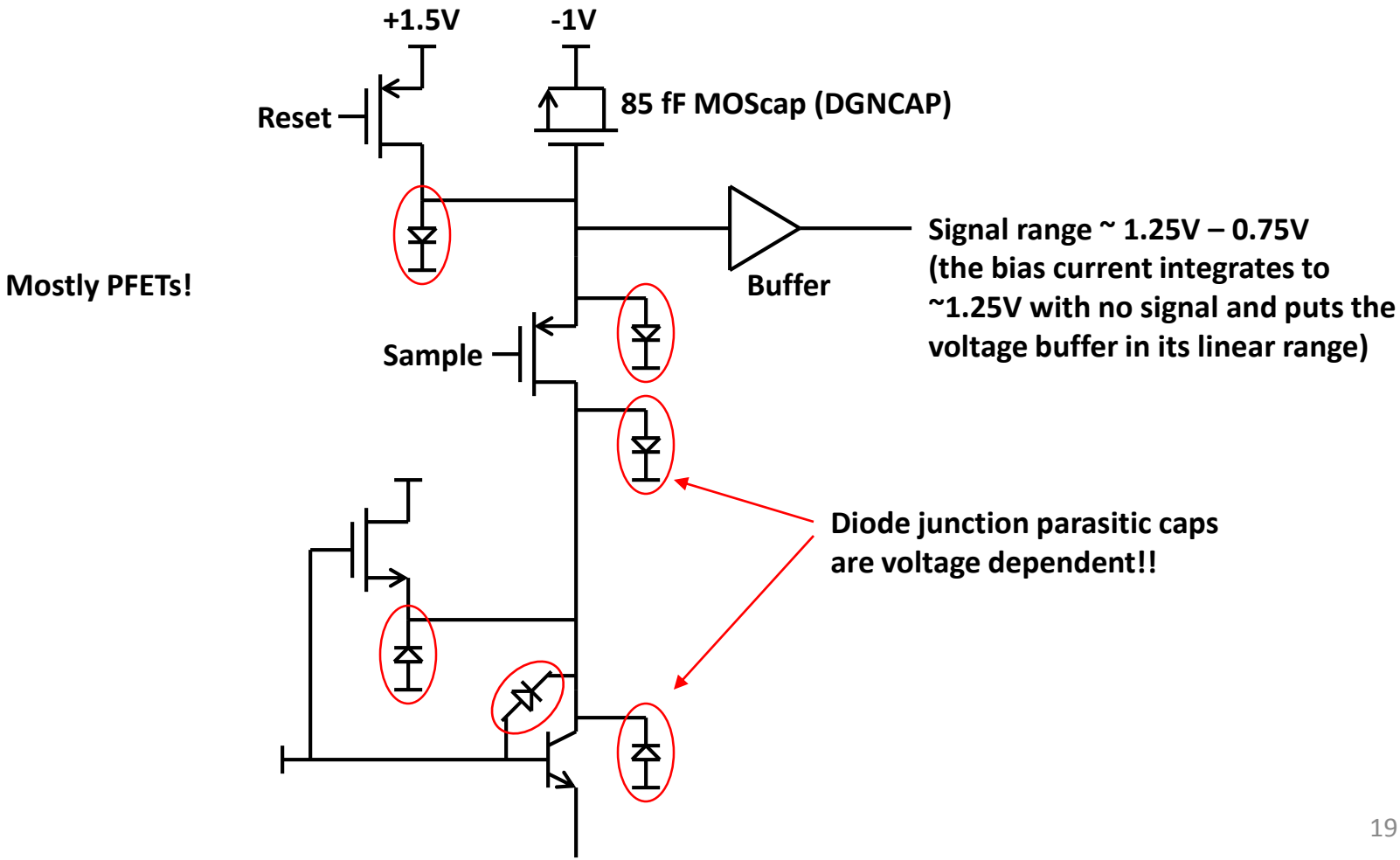
Strategy:

- 2 supply voltages, +1.5V and -1V.
- Digital section: use NFETs and PFETs, all NFETs in one Deep Nwell (digital psub = 0V)
- No Deep Nwells in analog (too much area required)
- NFETs and PFETs can be used in analog only if the voltage between any two terminals (including the substrate) is always < 1.5V. All NMOS FETs sit in the -1V substrate!
- If any analog two-terminal voltage can ever be > 1.5V, use DGNFET or DGPFET. *Try to minimize the number of NMOS FETs in the analog section*! (Can use 1.5V PFETs since they are in an Nwell, as long as maximum voltage limits are respected)
- Use enclosed layout for all DGNFETs (minimize leakage with radiation)
- No problem with NPNs, just limit Vce if necessary



Passive Integrator

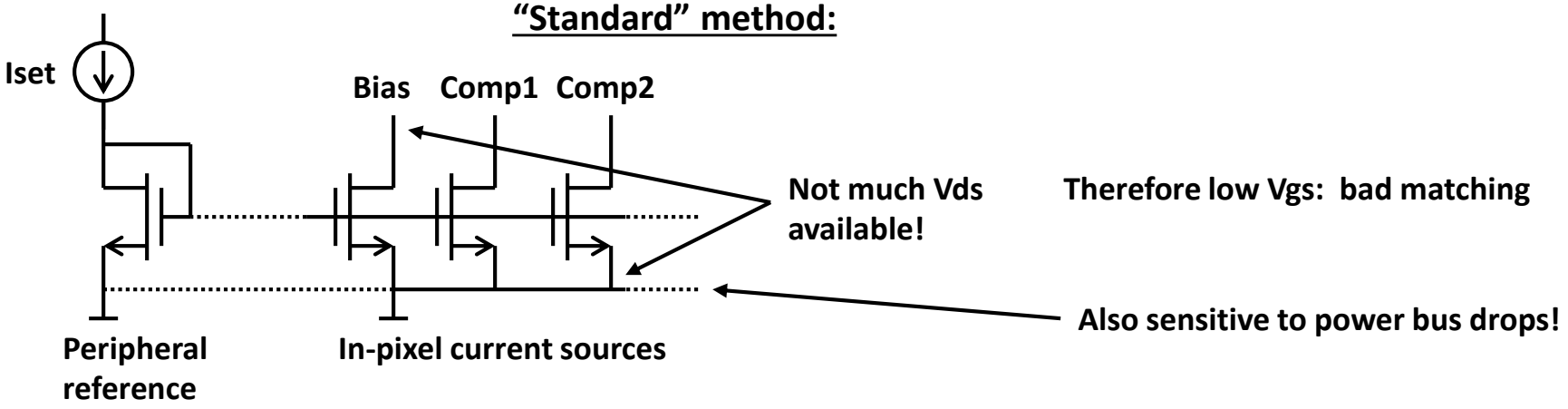
Integrator cap: Cint ~ 100 fF
Use DGNCAP MOS cap. Needs > 1.5V bias to be linear: reset to 2.5V!
Several non-linear parasitic diode caps contribute to Cint (15 - 20 fF total parasitic)
With careful attention and balancing, Cint is very stable with voltage (tests show to 0.1%)!



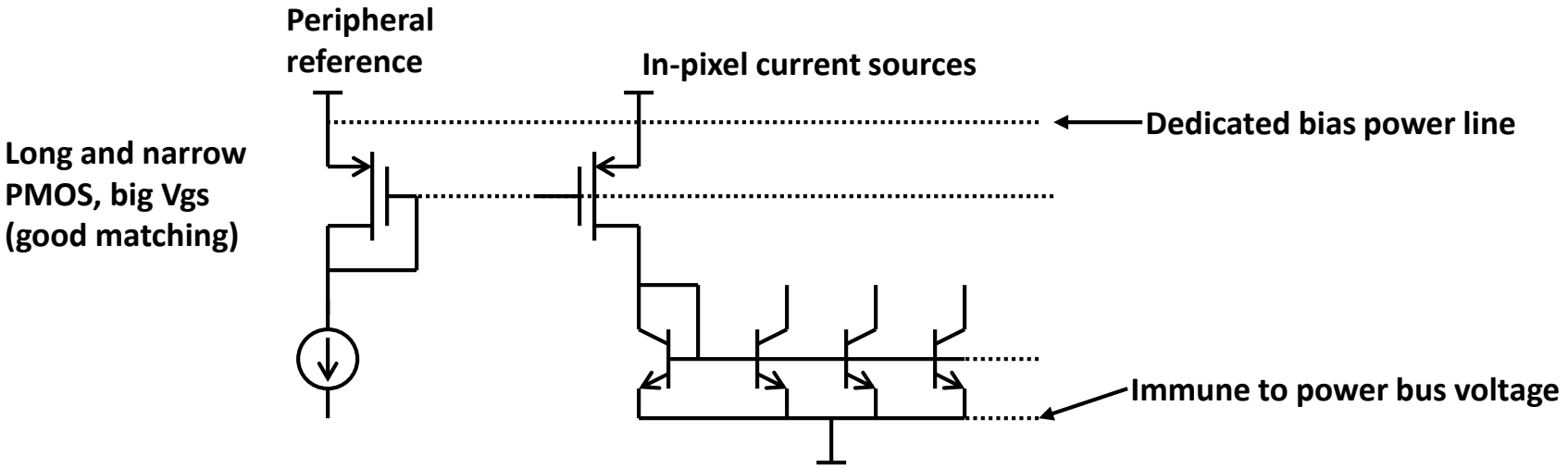
How to form the bias and compensating current sources?

Keep in mind the goal of minimum sensitivity to power supply variation and bussing IR drops!!

"Standard" method:



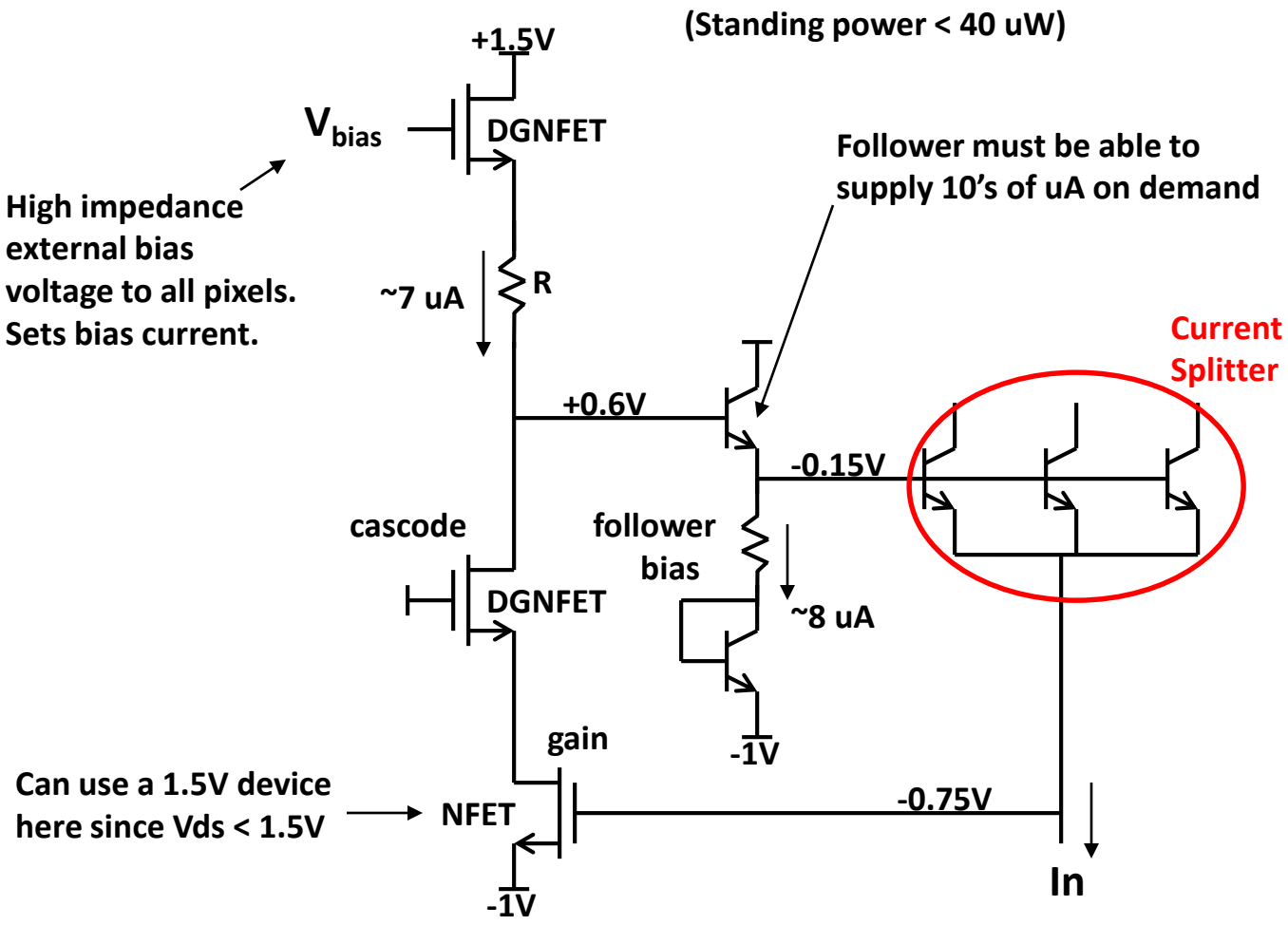
Better approach:



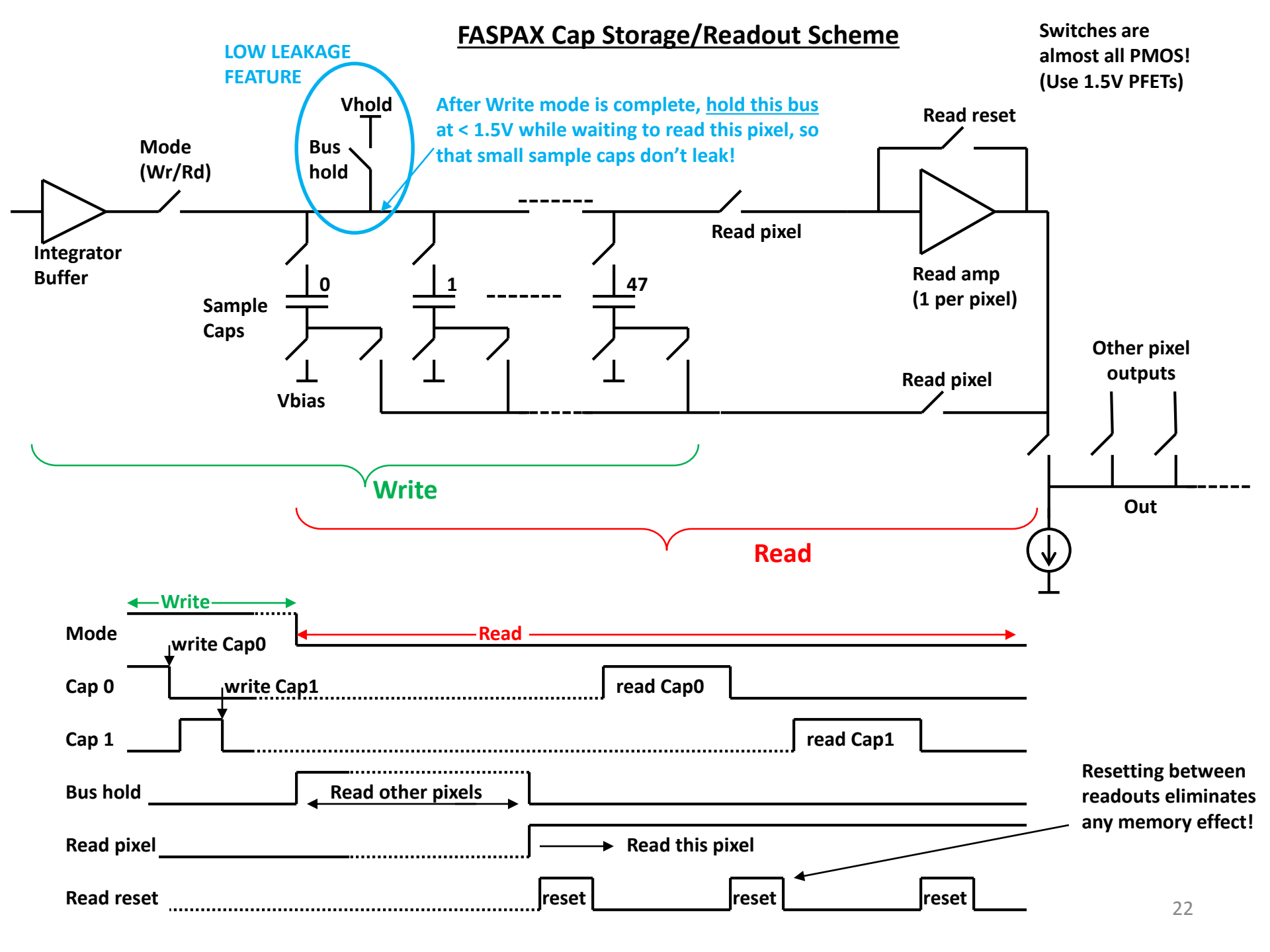
Feedback amplifier

Again, keep in mind the goal of minimum sensitivity to power supply variation and bussing IR drops!!

Design a self-biasing configuration that needs no classical transistor current sources:

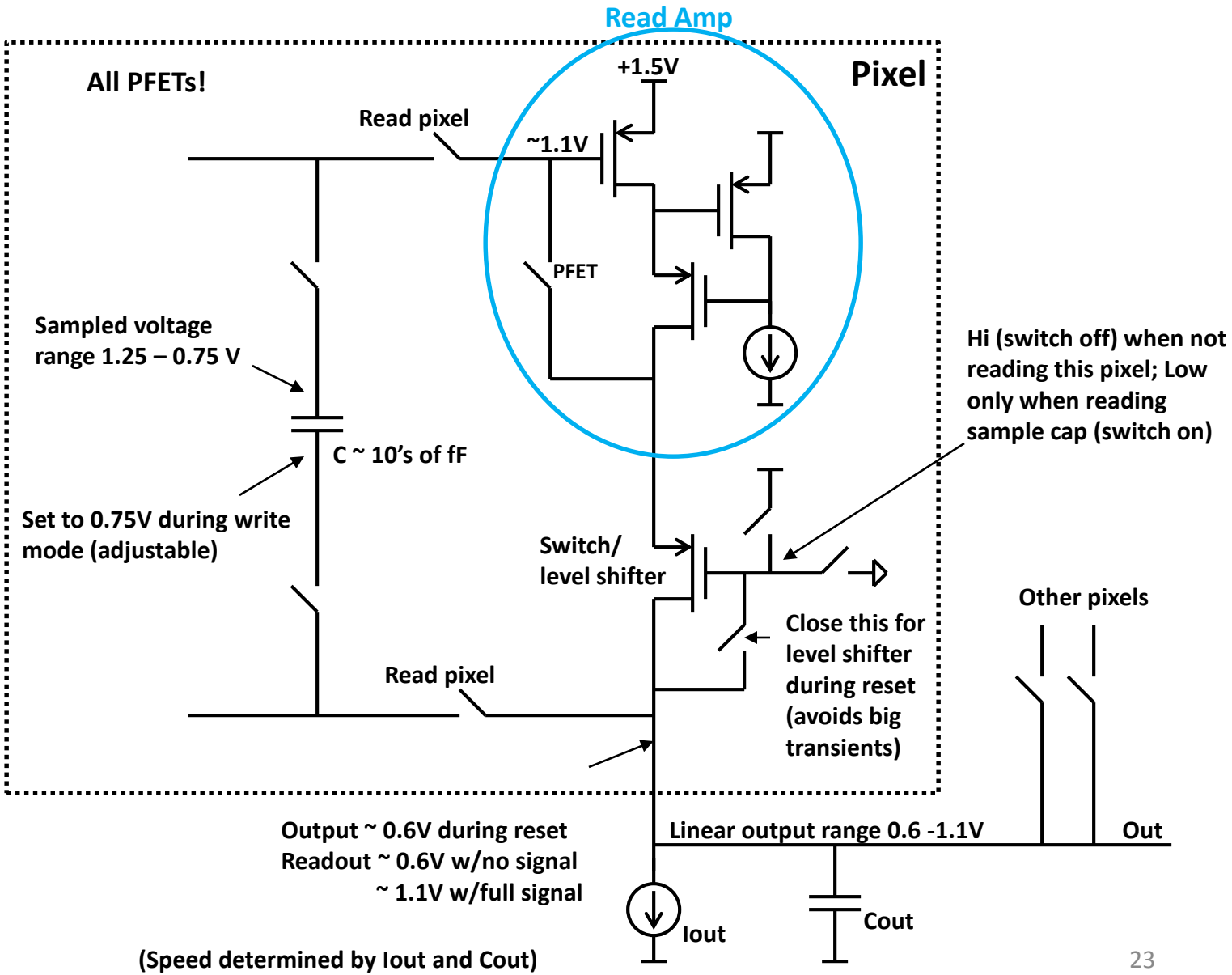


FASPAX Cap Storage/Readout Scheme

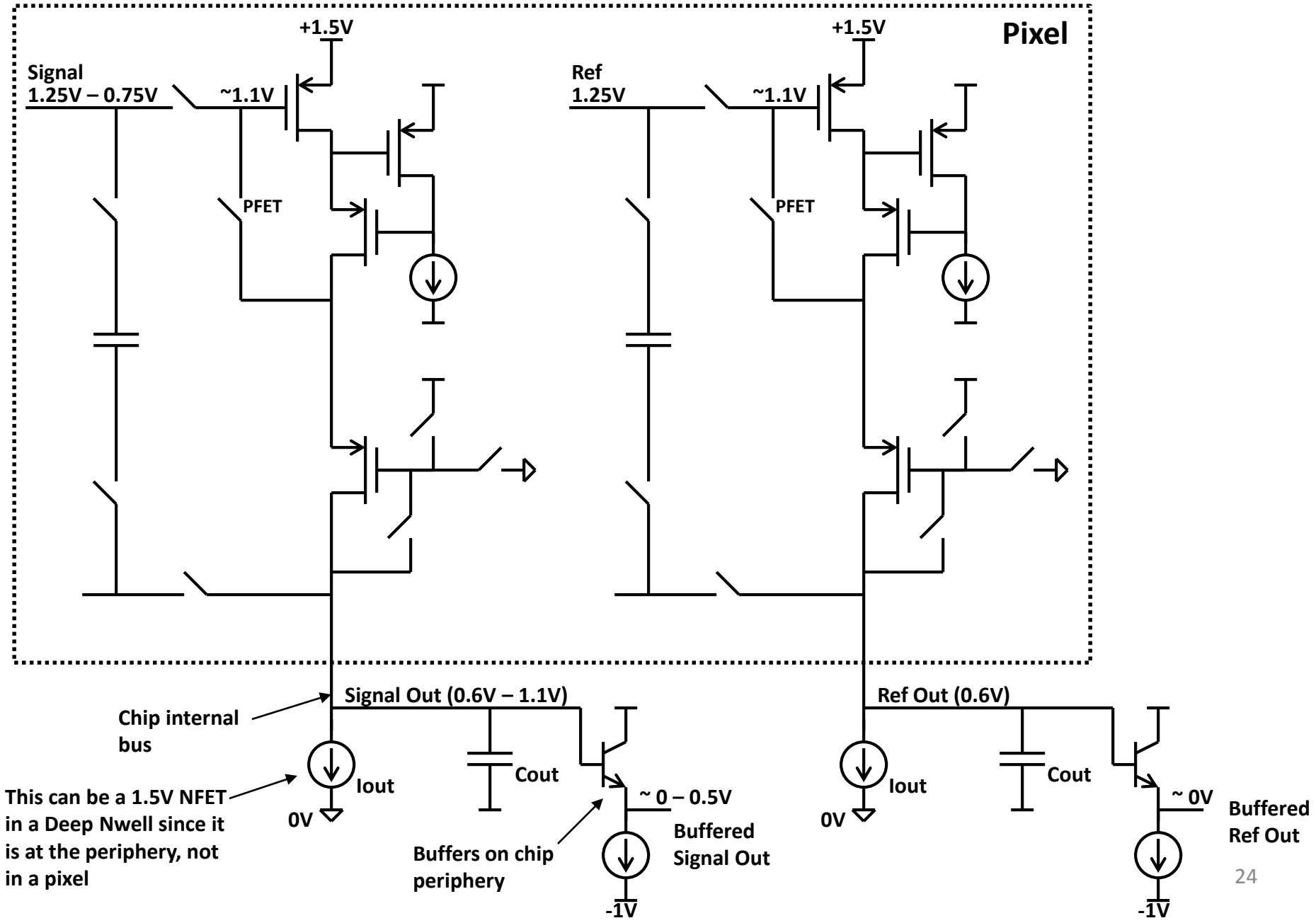


"Common Source" Readout technique (developed at Fermilab for other projects)

Inverting readout with gain = 1.0. Simple and very linear in a 0.5V range!



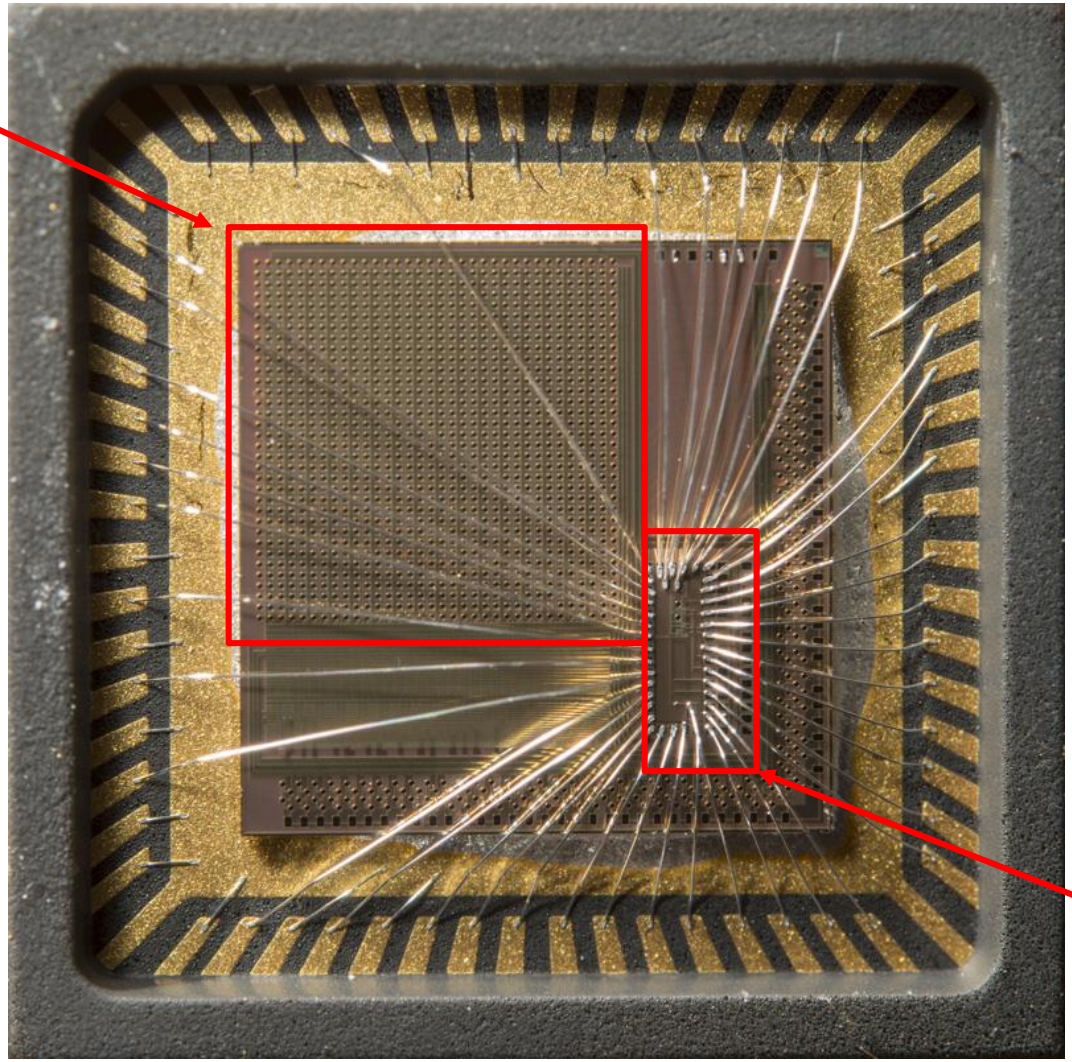
Pseudo-differential implementation of the readout, with output buffers:



The first prototype chip

Pixel array

(not tested yet)

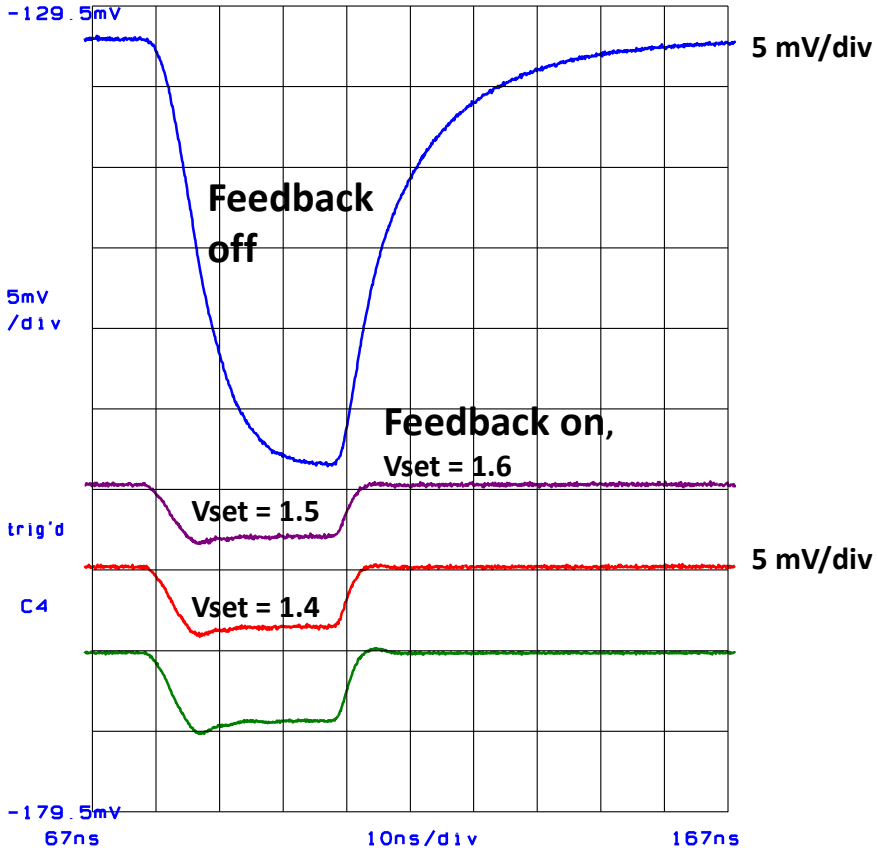


2 separate test circuits (Front End, Readout)

(tested)

A few test results:

Current splitter input voltage for 1 uA square pulse (Cin ~ 70 fF)



Effective transfer gain on Range 0: 8.8 mV/fC (close to expected)

Integrator range: with Vdd = +1.50V, the integrator is linear to 0.1% between 1.43V and 0.70V.
(Could easily reduce integration cap value and maintain linearity)

Range scaling: **Range 0 – 1 ratio is measured at x36 (on one chip, expected is x32)**
Range 1 – 2 ratio is measured at x1011 (expected is x1024)

Integrator Buffer Settling Time: < 10 ns

Cap Storage Array: works as expected, very linear

Storage cap droop:

Vhold	Droop for 4 ms hold time	
1.38V	136 mV	
1.35V	50 mV	
1.30V	8.5 mV	
1.25V	0.3 mV	
1.20V	~0	The bus hold strategy is very effective!

Some thoughts on noise

		Ibias	Sig. noise (e)	Sig. + Ref. noise (e)	
Front End	Shot noise (50 ns integration, calc. for C=100fF)	0.5 uA	395e	559e	Measured noise agrees closely with calculated
		0.2 uA	250e	354e	
		0.1 uA	177e	250e	
	Cint = 100fF KTC noise: (calculated)		113e	(159e for Sig. + Ref.)	
					Charge noise matters ↑
	Voltage buffer noise: (100 MHz BW, measured)		315 uV (224e @ 8.8 mV/fC)	445 uV (316e)	Voltage noise matters ↓
Read out	Sample cap KTC noise: (calculated for C=30 fF)		330 uV (234e @ 8.8 mV/fC)	467 uV (331e) ←	Voltage noise here would be reduced with bigger Csamp
	KTC + gm noise on Read Amp input		? ←		This noise will depend on the ratio: (Total Cin)/Csample
	Total Read Amp noise (measured)		612 uV (435e @8.8 mV/fC)	865 uV (615e) ←	Measured with a small pipeline test circuit, will be worse in a final chip.

Noise is too high!

Strategies for noise reduction:

Front End: Reduce Ibias as much as possible (challenge to maintain desired frequency response, needs design mods)
Reduce Cint to raise transfer gain (reduction in input referred noise from voltage buffer and readout)

Readout: Increase the value of Csample (double it to 60 fF?)
Reduce Read Amp Cin as much as possible (minimize Cin/Csample ratio!)

Summary

- **A first prototype chip has been fabricated.**
- **The 2 test circuits (Front End and Readout) have been tested with good results, showing that the proposed method for a small area, high dynamic range pixel works.**
- **The prototype pixel array still remains to be tested.**
- **The noise is higher than desired for single-photon resolution – this must be addressed**
- **A second small-scale prototype of test circuits that incorporate strategies to lower the noise will be designed and fabricated. Range select logic still needs to be designed, and will probably be included on this submission.**
- **Lessons learned from testing the pixel array will be factored into a future full-size array submission.**