Front end electronics for silicon strip detectors in submicron technologies

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Outline

- Silicon strip detectors for the High Luminosity LHC upgrade
- Requirements and constraints
- Basic architectures of the input stages
- Examples of the channel architecture for ATLAS and CMS
- Summary

Silicon strip trackers for LHC high luminosity upgrade

Silicon strip sensors are baseline solution for the inner tracking detectors at HL LHC(*) for 30cm<r<1m

- ATLAS: strips 2.5 and 5cm/70um pitch, (ABCStar chip in GF 130nm)
- CMS: strips 5cm/90um pitch (CBC in GF 130nm), 2.5cm/100um pitch (SSA chip in TSMC 65nm) combined with 1.44mm strips (MPA chip in TSMC 65)
- LHCB: strips 5 and 10cm/pitch 95 or 190um (SALT chip in TSMC 130nm)

(*) experiments operating with high luminosity and in highly radiation environment (not ALICE)

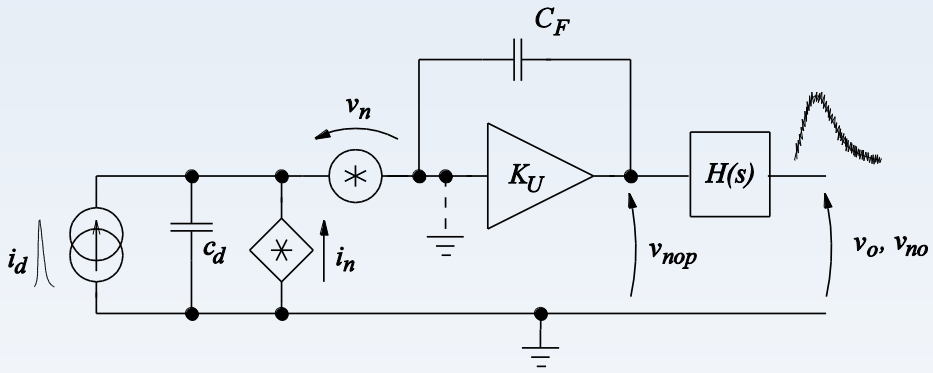
Silicon strip trackers for LHC high luminosity upgrade (2)

- Radiation environment: doses in the range of 100MRad and 10^{15}N/cm^2 → CMOS deep submicron (now 130 or 65 nm)
- High luminosity = high granularity →
  - lower sensor capacitances (usually a few pF)
  - power/area constant (~10mW/cm^2) → reduced power/channel
- Lower signals (thinner sensors, severe radiation damage) → maximum ENC below 800 to 1000 e-

→ impact on the optimization of the input stage

Reception of signal from sensors

- Charge Sensitive Amplifiers & CR-RC shaper (Tp < 25ns)
- Main contributions from electronics to ENC (ideal case, SE stage): input transistor and feedback



SERIES

$$ENC^2 = \left(F_V \, \overline{v_{ne}} \, c_d / \sqrt{\tau}\right)^2 + \left(F_i \, \overline{i_{ne}} \, \sqrt{\tau}\right)^2$$

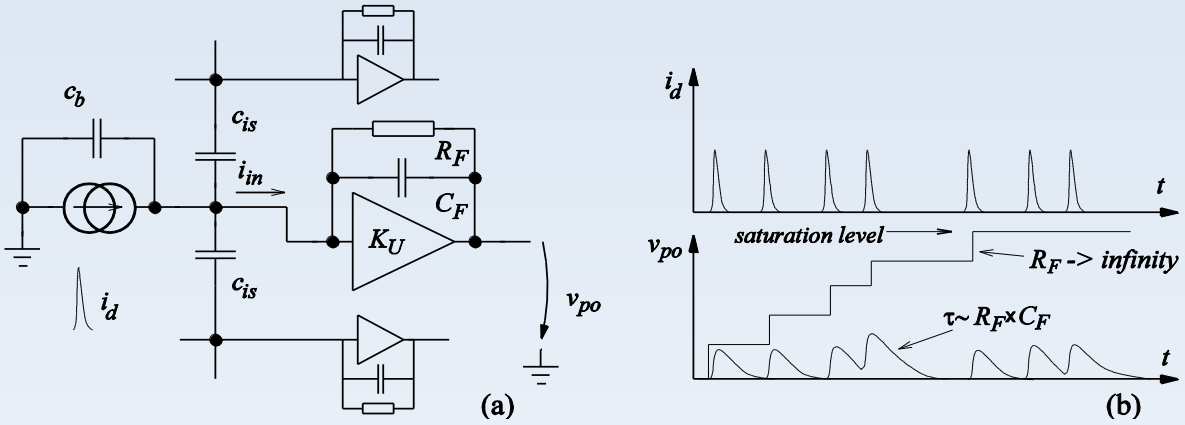
where

$$\overline{v_n} = \sqrt{\frac{4\,k\,T\,\gamma\,n}{g_m}}$$

Higher granularity of the sensor helps for noise/power optimisation (series noise dominant)

τ – peaking time c_d – detector capacitance
F_V, F_i – filter coefficients for CR-RC^n filter

Reception of signal from sensors (2)



Strip detector: mesh of the parasitic capacitances → basic task for the input stage: effective charge collection and crosstalk minimization (low input impedance of the preamplifier)

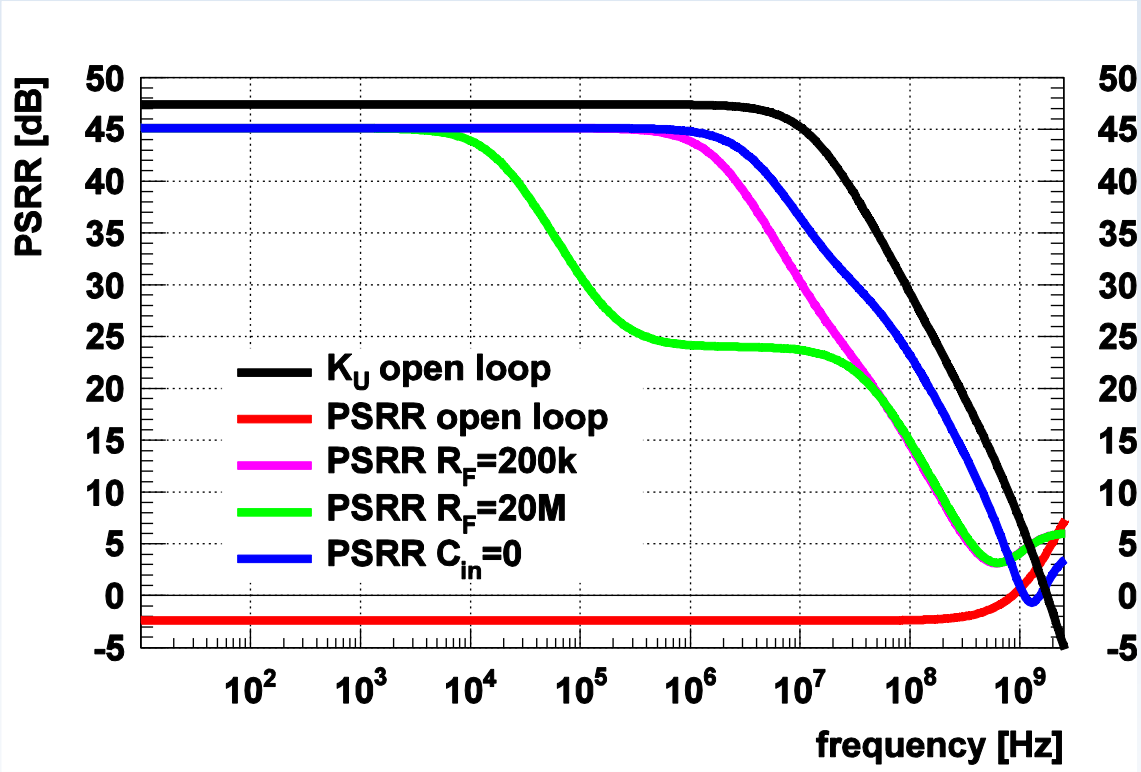
CSA input impedance: feedback impedance divided by open loop gain →

- trade off between input impedance and close loop gain
- transimpedance amplifier preferable

For electronics at ATLAS and CMS we require GBP above 1GHz and open loop gain 70-80dB (for detector capacitances of the order of 3-8pF the crosstalk signals below 5%)

Optimisation of the input stage → driving the open loop gain and GBP preserving the power budget (single ended input stage preferable)

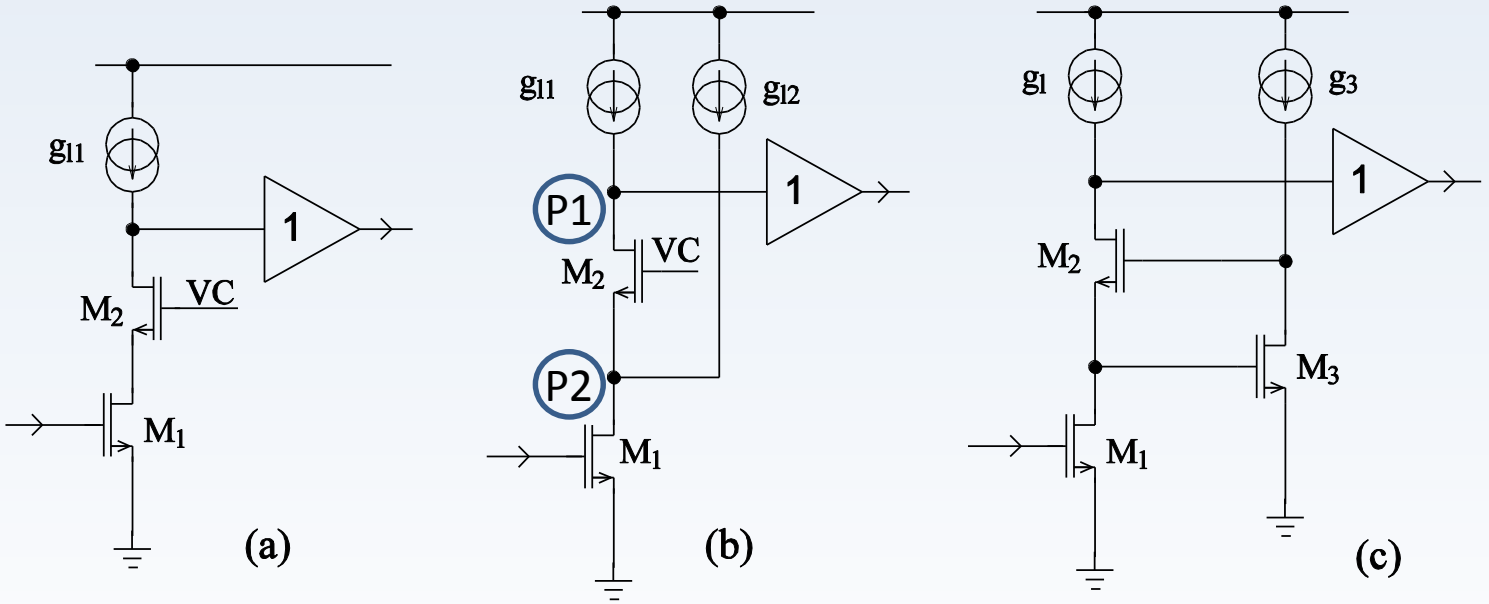
PSRR: another motivation to increase GBP and open loop gain



Open loop gain and PSRR characteristics on the example of TDCPix preamp (fast (Tp=5ns) pixel, GF 130nm) working in charge and transimpedance mode

High gain input stages for CSA

- **Requirements: High radiation** → CMOS devices only, 130 and 65nm processes.
  Low power → single stage, high bandwidth and high open loop gain (50-80dB) amplifier → telescopic cascode.
- Dominant noise source for fast shaping: series noise of the input transistor (thermal) → NMOS transistor preferable
- Unity gain buffer to avoid loading effect from the feedback circuit



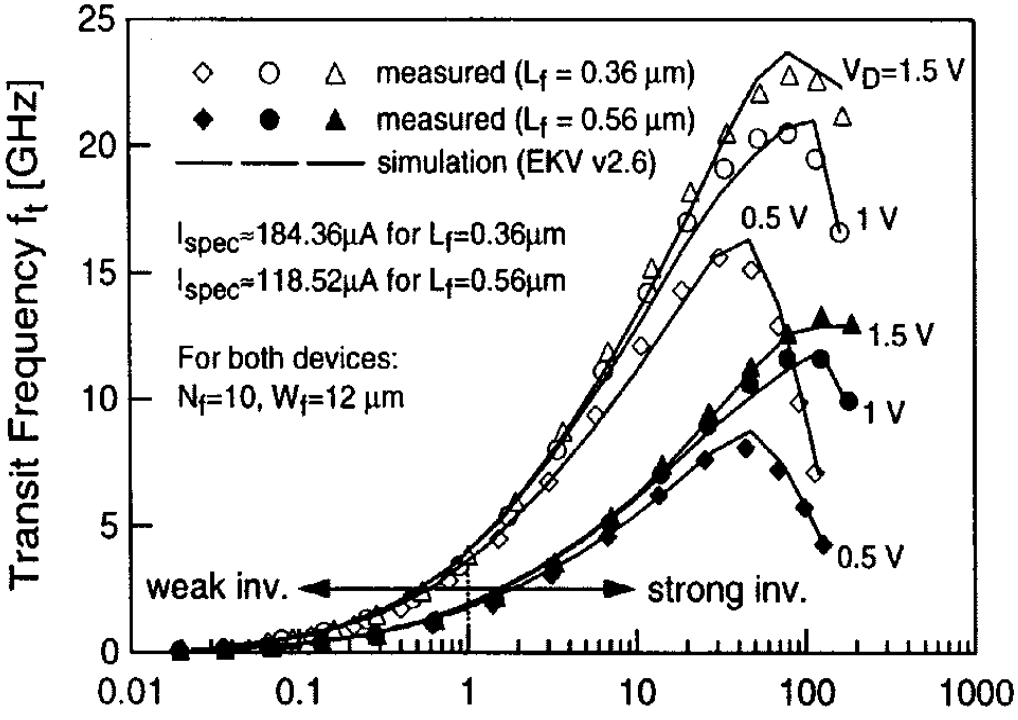
(a) Telescopic cascode, (b) telescopic cascode with GBP improvement (shifting P1, limit by P2), (c) regulated telescopic cascode

High gain and GBP: technology limitation

IBM CMOS	250nm RF (IBM)	130nm RF (GF)	65 nm LP (TSMC)
t_{OX}	5nm	2.2nm	2.6nm
K_p@Ispec NMOS	330 uA/V^2	720 uA/V^2	320 uA/V^2
Vdd	2.5V	1.2V (1.5V)	1.2V
g_m/g_{ds} moderate inv. (example for input transistor)	70 (l=500nm)	30 (l=300nm)	18 (l=140nm)*
Peak ft	35 GHz	94 GHz	240 GHz

(*) g_m/g_{ds} ~constant for the same transistor length

Limitations for GBP: consequence of the operating point



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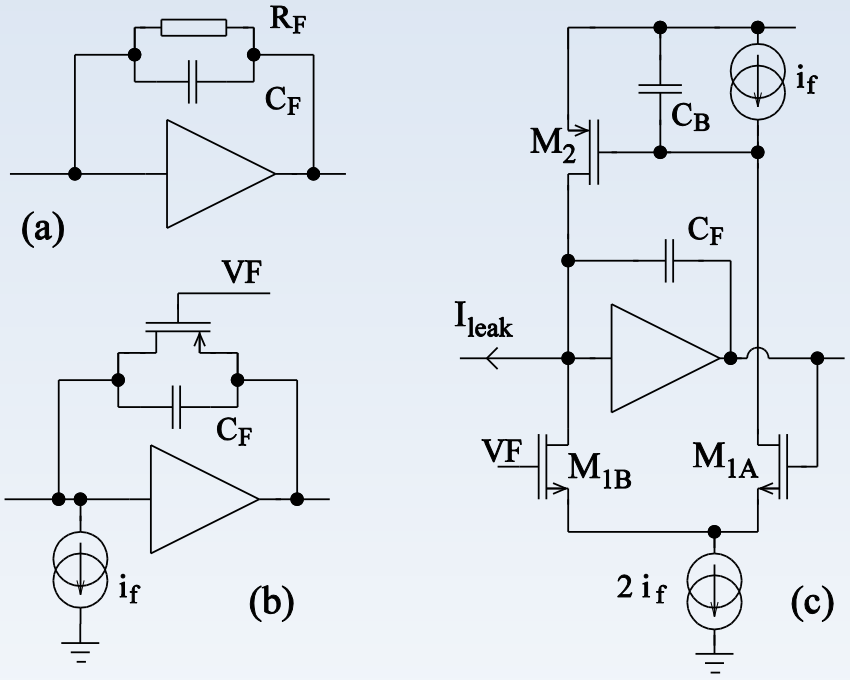
Transit frequency ft as a function of inversion order for 250nm CMOS technology

Transit frequency is degraded with device dimensions and depends strongly on the bias (inversion region); in front end electronics we are far away from the maximum ft

Limitations for GBP: layout constraints

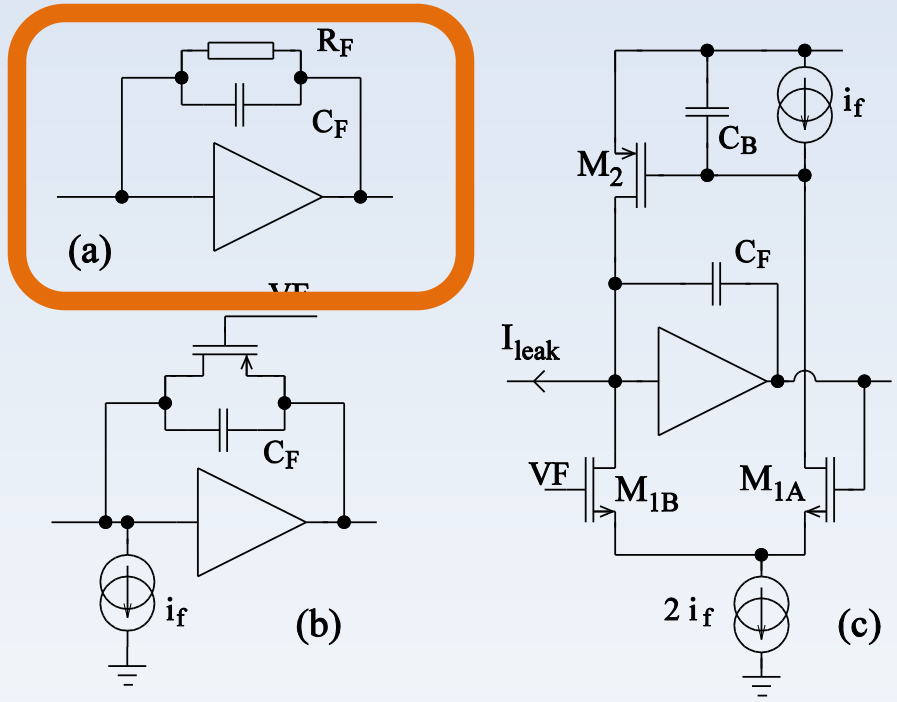
Multichannel (128-256) ASIC: front end electronics layouted in narrow pitches (22um for ABCStar) – not optimal for preserving GBP (differences between schematics and layout for GBP up to 30%)

Input stages: feedback circuits in ATLAS and CMS front end amplifiers



- Main tasks:
  - Integration of charge on the feedback capacitor C_F (defines signal gain)
  - Baseline restoration (resistor or active circuit):
    - discharge of the C_F (high data rates → short time constant)
    - leakage current compensation (in case of DC coupled sensors)

Input stages: feedback circuits in ATLAS and CMS front end amplifiers



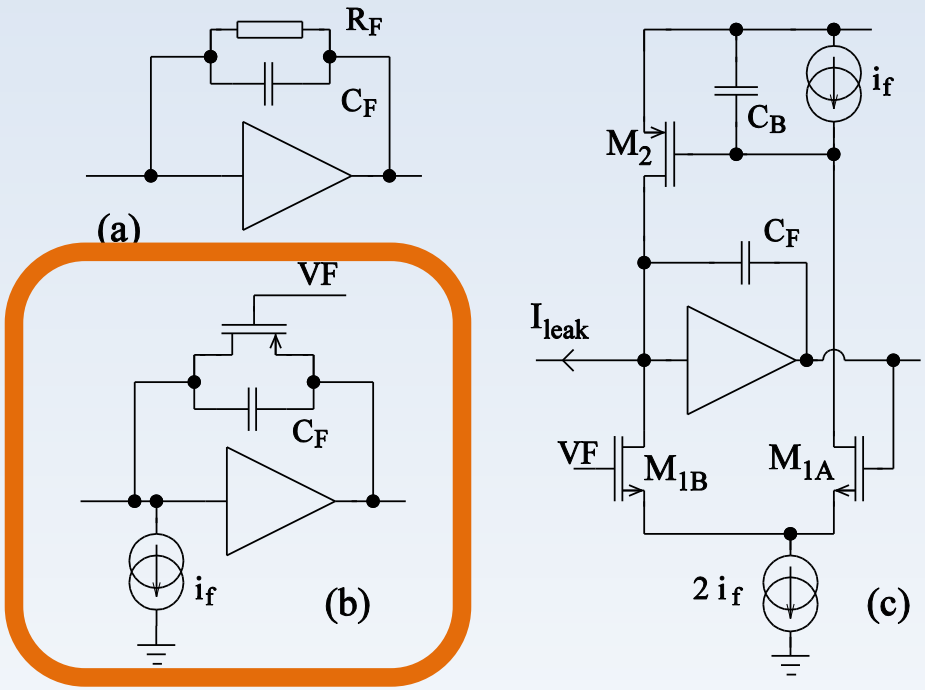
(a) Resistive feedback

Discharge with $\tau \sim R_F C_F$, ENC: parallel noise contribution $\sim 1/R_F$

Disadvantage: no control of DC at preamp output

Advantage: simple and robust, tolerance to low level of leakage (DC change but no extra noise contribution), leakage compensation can be added

Input stages: feedback circuits in ATLAS and CMS front end amplifiers



(b) Active feedback with MOS in saturation

Discharge with $\tau \sim C_F/g_m$, ENC: parallel noise contribution $\sim g_m$ of feedback transistor (and from i_f)

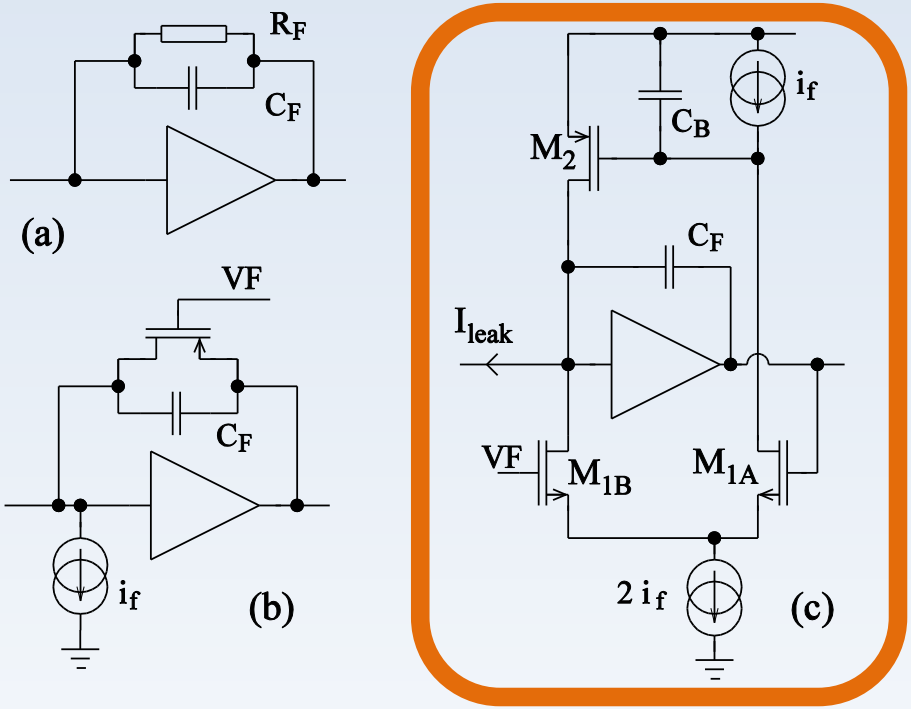
Disadvantage:

- no leakage compensation – AC coupled sensors
- Signal compression for negative charges (n-on-p sensors)

Advantage: easy control of DC at the preamp output (with V_F), fast response for signal overdrive (quadratic compression)

Used in ABC250 and ABC130 prototypes.

Input stages: feedback circuits in ATLAS and CMS front end amplifiers



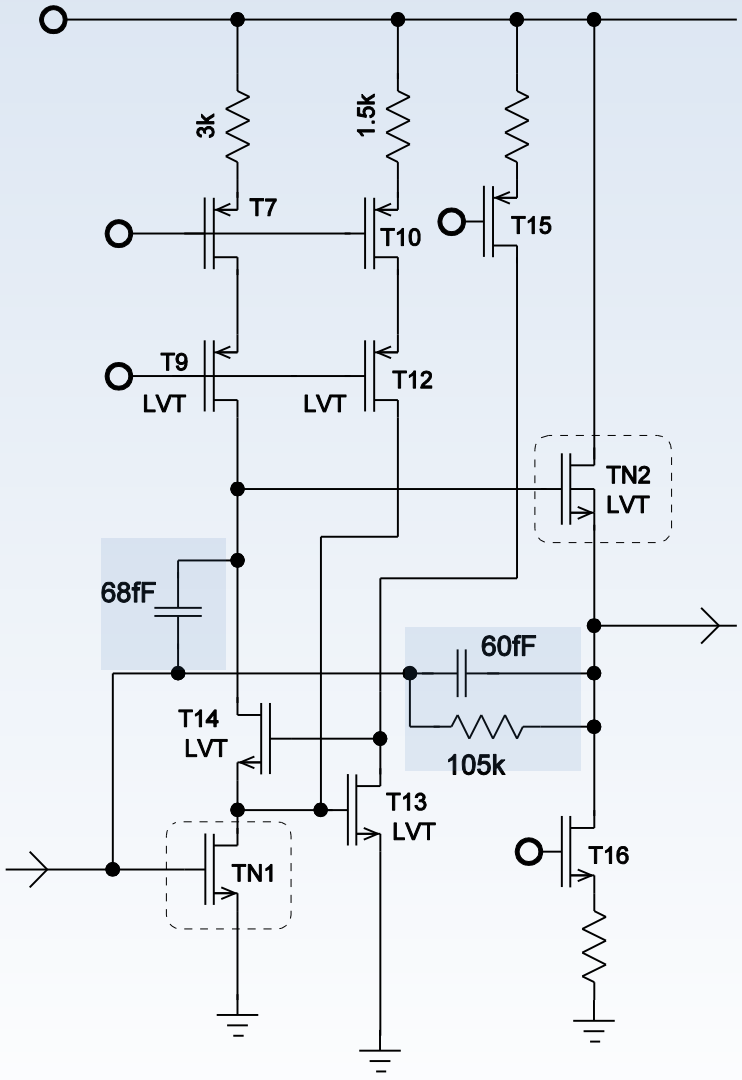
(c) Krummenacher feedback

Discharge with $\tau \sim 2C_F/g_{m1}$, ENC: main parallel noise contribution $\sim g_m$ of transistor M_2 (still some contribution from M_{1B})

Disadvantage: extra low freq. zero, 2x higher parallel noise when compare to simple AFP

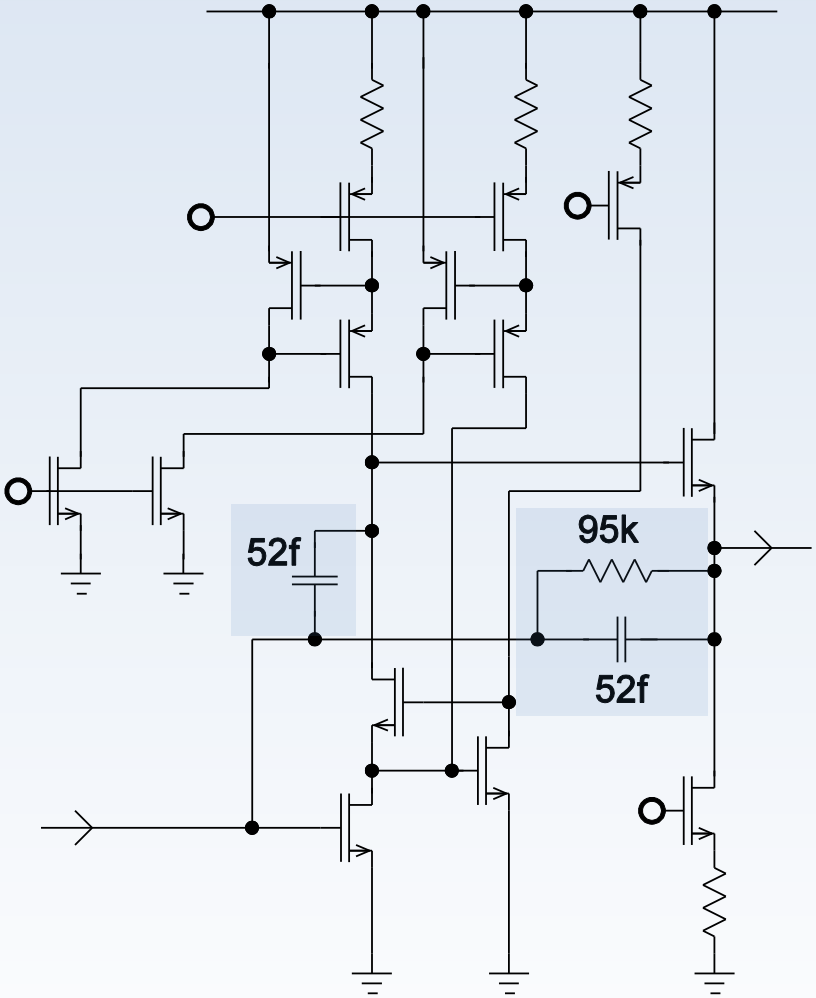
Advantage: leakage compensation, small silicon area for high feedback impedance implementation (important for pixel circuit), DC at the output controlled with V_F, no signal compression

ATLAS strip tracker – ABCStar amplifier



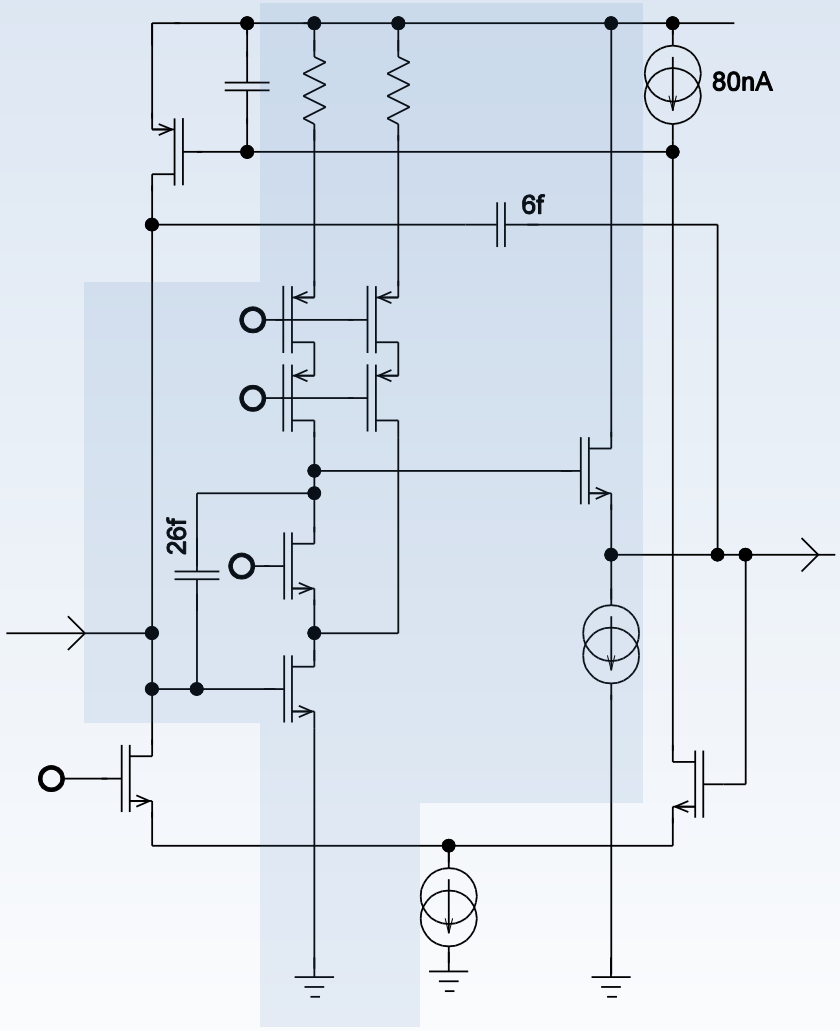
- Application: ATLAS silicon strips (2.5cm and 5cm), Cin: 3-8pF
- GF130nm process
- Regulated cascode with NMOS input transistor biased with 140uA
- Open loop gain: 78dB (standard cascode load)
- GBP boosting (GBP~1.5GHz)
- Miller compensation with poles splitting
- Resistive feedback
- Strong (120mV) degeneration of active loads (noise minimization), minimum Vdd 1.1V (max=1.6V)

CMS short strips (PS) – SSA



- Application: CMS short strips (2.5cm), Cin~5pF
- TSMC 65nm process
- Regulated cascode with NMOS input transistor biased with 130uA
- Open loop gain: 80dB (fully regulated cascodes)
- GBP boosting (GBP~2GHz)
- Miller compensation with poles splitting
- Resistive feedback
- Light (60mV) degeneration of active loads (noise minimization), minimum Vdd 1.15V (max 1.26V → tight for power distribution system)
- Mixture of regular, HVT, LVT and native transistors (to optimize the operating point)

CMS ultra short strips (PS) – MPA

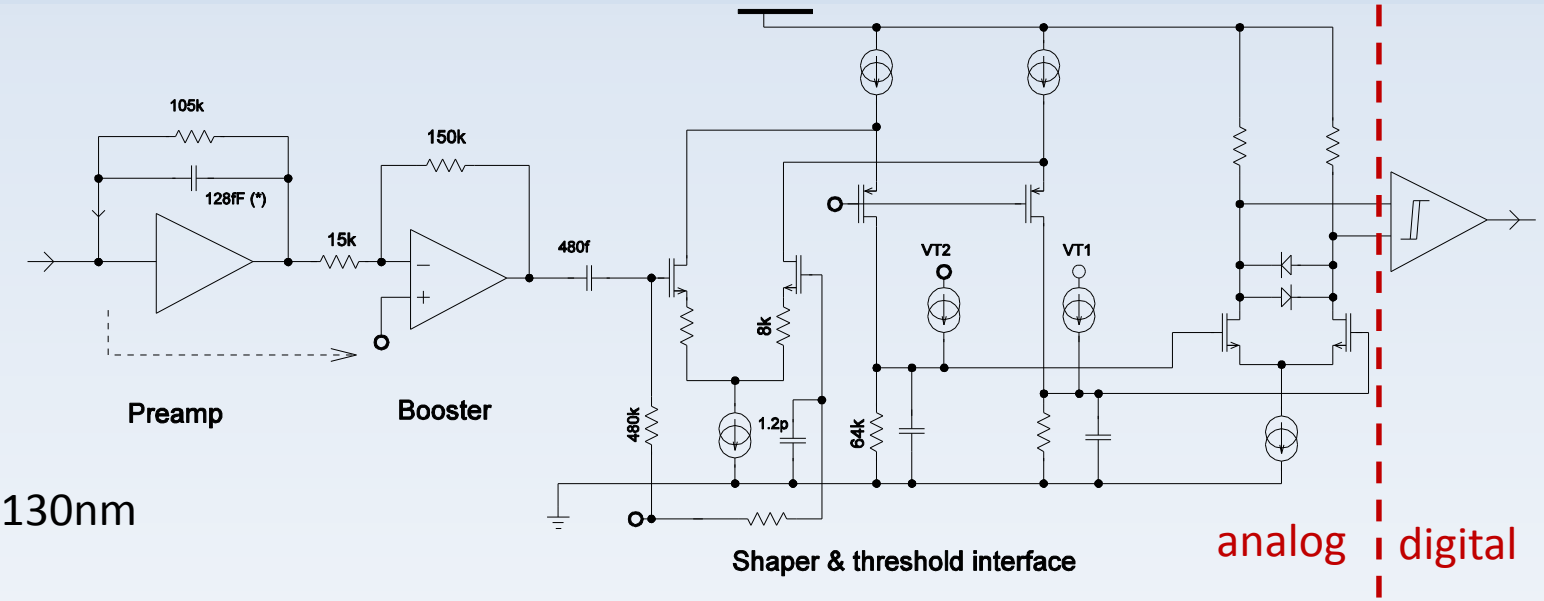


- Application: CMS ultra short strips (1.44mm), Cin<0.5pF
- TSMC 65nm process
- Telescopic cascode with NMOS input transistor biased with 12uA
- Open loop gain: 54dB
- GBP boosting (2GHz)
- Miller compensation with poles splitting
- Krummenacher feedback
- Light (60mV) degeneration of active loads (noise minimization), minimum Vdd 1.1V

Front End channel: examples

- ATLAS and CMS strip trackers: binary architecture (low power, simple and robust) → to limit so called "common mode" effects we need:
  - Reasonable PSRR
  - Good separation between analog and digital domains in terms of:
    - substrate isolation (triple well, BFMOAT, NT_N)
    - architecture (single ended to differential conversion (at least between analog and digital part of discriminator))
  - Reasonable gain in the front of the discriminator (50-100mV/fC) → in most cases we need booster amplifier (for few pF input capacitance the preamp feedback capacitor is around 100fF → preamp gain <10mV/fC)
- Maximum one AC coupling (difficult to DC couple 3 gain stages) after preamp or after booster (it limit the mismatch propagation and improves PSRR at low and medium frequencies)
- Low pass filter in the last gain stage (shaper) to improve the PSRR. The final shape is similar to CR-RC^2 because of bandwidth limitations in all gain stages.

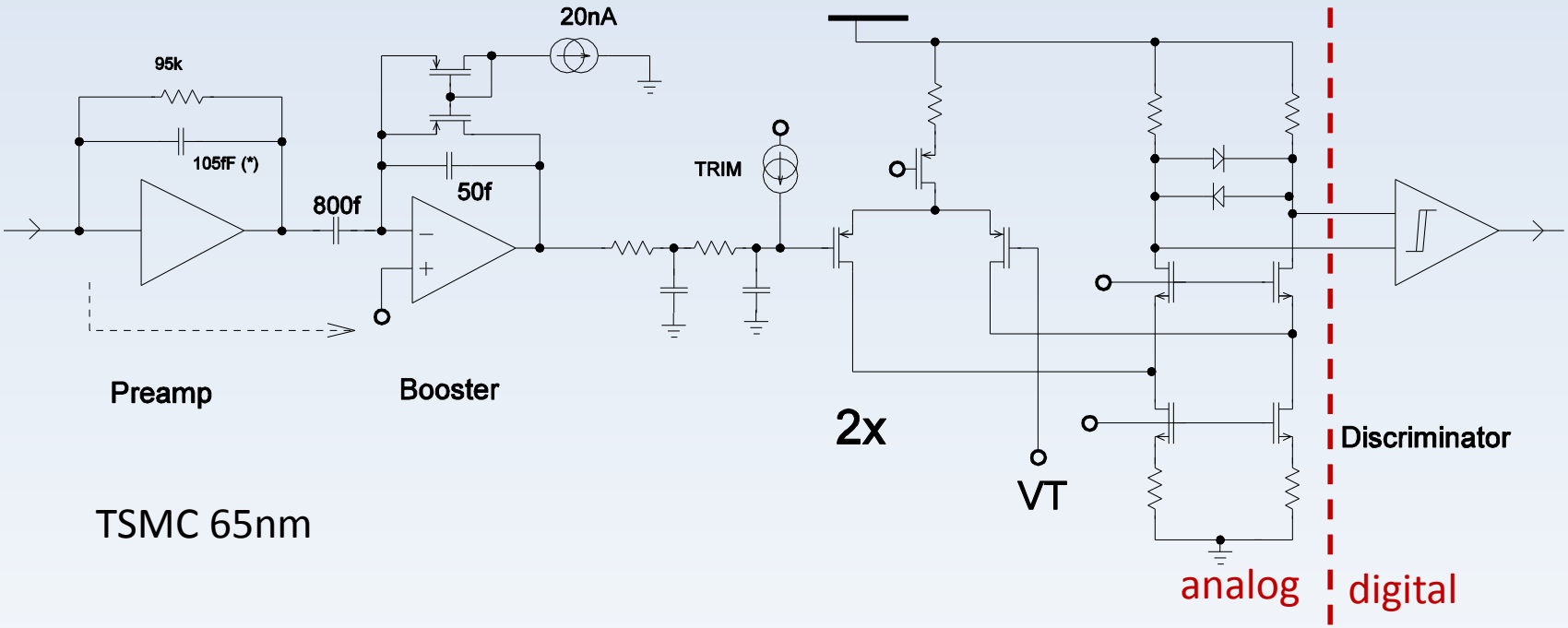
ABCStar channel



GF 130nm

- Preamp with resistive feedback (105k) and 115fF equivalent capacitor
- 10V/V booster amplifier
- AC coupled single ended to differential shaper/threshold interface (folded cascode with resistive load and degeneration)
- Differential thresholds current sources (VT1&VT2: global DAC and TRIM DAC) → architecture has impact on gain matching but allows for optimisation of the dynamic range for 1.2V supply
- Shaping 22ns, ENC@5pF 600e-, gain 95mV/fC
- Power **consumption** ~320uW

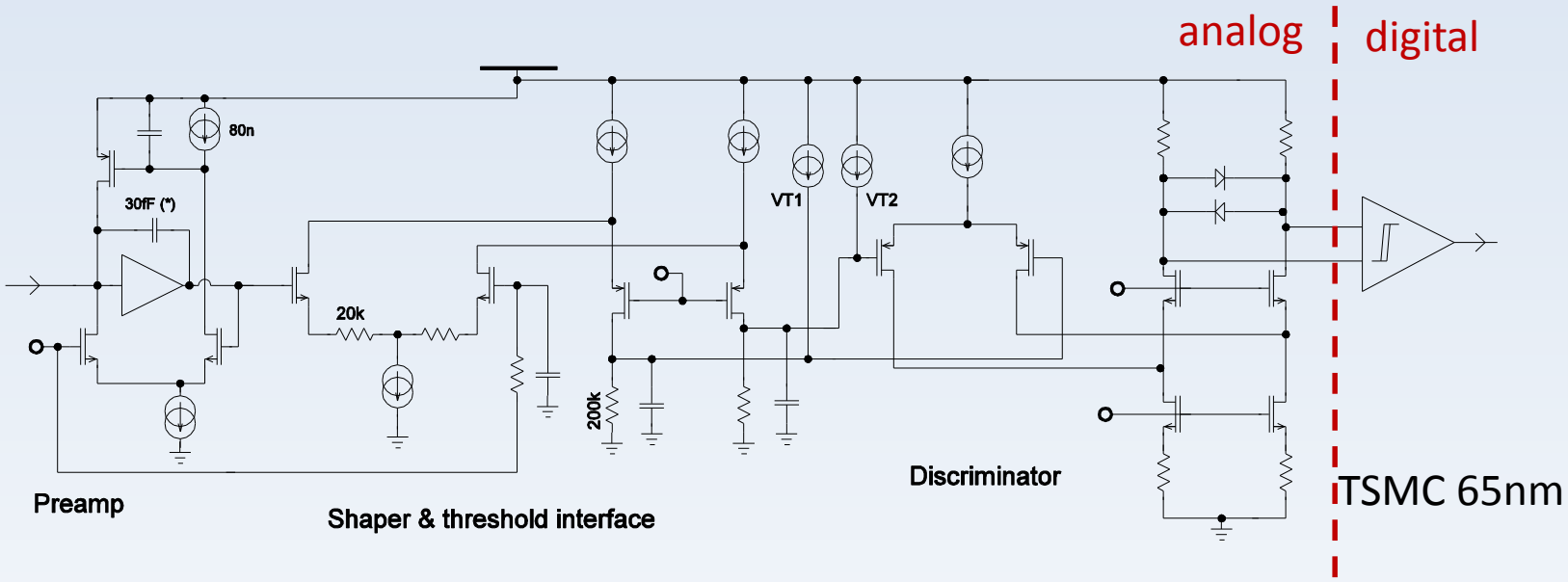
CMS short strips (PS) – SSA



TSMC 65nm

- Preamp with resistive feedback
- Booster: capacitive feedback (~15V/V) with active feedback for overshoot compression (PMOS in linear region with overshot compression); architecture optimized for double pulse resolution (<50ns), (same principle as in CBC chip for CMS long strips)
- Passive RC filter
- Shaping 17ns, ENC~700e- at C_{in}=5pF, gain 50mV/fC (to allow for higher linearity; over MIP signal detection)
- 2x 3 stage discriminator, (1st stage; folded cascode with resistive load); differential coupling between analog and digital domains
- Overall power: 300uW

CMS ultra short strips (PS) – MPA

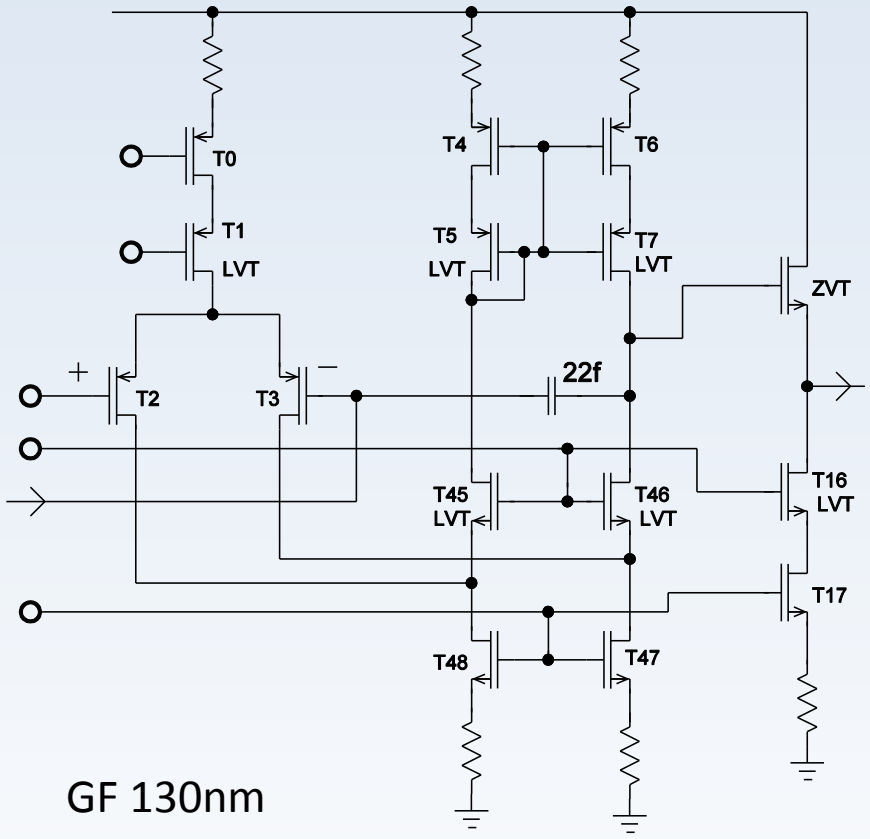


- Higher gain in the preamp (Cin<0.5pF) → no need for booster
- Second stage DC coupled: folded cascode with resistive load and degeneration (NMOS input possible because of DC output stabilization) → still one low freq. zero in transfer function from Krummenacher
- 3 stage discriminator
- Power per channel ~35uW
- Peaking time 24ns, ENC with detectors <200e-, gain 85-90mV/fC

Booster amplifiers: requirements

- For 20ns peaking time shaper and 10V/V gain:
  - open loop gain above 40dB
  - GBP above 250MHz

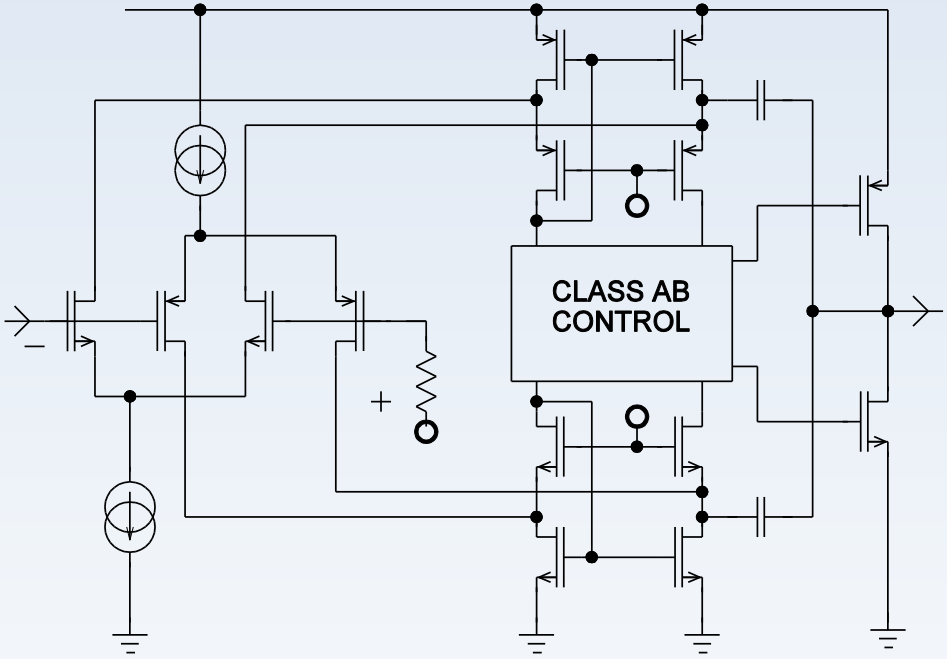
Booster (ABCStar)



GF 130nm

- Folded cascode with PMOS input (to match DC from preamp) with zero VT NMOS
- open loop gain 48dB/280MHz GBP
- Consumption: 50uA

Booster (SSA)



TSMC 65nm

- Classical RtR amplifier with class AB output stage
- open loop gain 60dB/400MHz GBP
- Consumption: 35uA

Summary

- Presented selection of circuit is limited to the new designs for upgraded ATLAS and CMS
- Clear tendency to use telescopic cascodes (standard or regulated) with NMOS input device
- Binary architecture in all designs