FE65-P2: Prototype Pixel Readout Chip in 65nm for HL-LHC Upgrades

Tomasz Hemperek, Dario Gnani, Abderrezak Mekkaoui, Rebecca Carney, Mauricio Garcia-Sciveres, Hans Krueger, Timon Heim, Mark Standke, Carlo Gottardo, Veronica Wallangen, Lashkar Kashif

hemperek@uni-bonn.de
## Moore's law in HEP

Moore's Law is a observation made by Gordon Moore in 1965 which states that the number of transistors on an integrated circuit doubles approximately every two years, or equivalently, the cost of computers shrinks by about half every couple of years. The graph below shows the number of transistors on a chip from 1970 to 2010.

### Table: HEP Technology Standards

<table>
<thead>
<tr>
<th>Name</th>
<th>D-OMEGA Ion</th>
<th>LHC1</th>
<th>FE-I3</th>
<th>FE-I4</th>
<th>RD53A</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Technology Node</strong></td>
<td>3 µm</td>
<td>1µ</td>
<td>0.25 µm</td>
<td>0.13 µm</td>
<td>65 nm</td>
</tr>
<tr>
<td><strong>Chip size</strong></td>
<td>8.3x6.6 mm²</td>
<td>8x6.35 mm²</td>
<td>10.8x7.6 mm²</td>
<td>18.2x19 mm²</td>
<td>20x20 mm²</td>
</tr>
<tr>
<td><strong>Pixel size</strong></td>
<td>75x500 µm²</td>
<td>50x500 µm²</td>
<td>50x400 µm²</td>
<td>50x250 µm²</td>
<td>50x50 µm²</td>
</tr>
<tr>
<td><strong>Pixel array</strong></td>
<td>16x63</td>
<td>16x127</td>
<td>18x160</td>
<td>80x336</td>
<td>400x400</td>
</tr>
<tr>
<td><strong>Transistor count</strong></td>
<td>???</td>
<td>800k</td>
<td>3.5M</td>
<td>80M</td>
<td>~1G</td>
</tr>
</tbody>
</table>

hemperek@uni-bonn.de

FEE2016 - Krakow - 31.05.2016
Phase 2 upgrade of ATLAS and CMS

- 100MHz/cm²
- 400MHz/cm²
- 2GHz/cm²
# Specification for RD53A

## Parameter | Value
--- | ---
Pixel size | 50x50 or 25x100 µm²
Analog power | 4 µA/pixel -> 160/cm² (<100 fF)
Digital power | < 4 µA/pixel -> 160 mA/cm²
Analog Threshold | 600 e-
Timing Resolution | 25 ns
Hit Rate | >2 Ghits/cm²
Trigger Rate | 1 MHz
Trigger Latency | 12.5 µs
Output Data Rate | 5 Gbit/s
Powering schema | serial
Size | 400x400 pixels (2x2 cm²)
Radiation tolerance | > 500MRad

[https://cds.cern.ch/record/2113263](https://cds.cern.ch/record/2113263)
Specifications:
• TSMC 65 nm design
• 64x64 pixel matrix with 50x50 µm bump pattern
• Designed as “analog islands in digital sea”

Goals:
• Exercise and test design flow in TSMC 65 nm
• Test prototype version of analog pixel front end
• Demonstrate low threshold operation with chosen isolation and power distribution
• Use for sensor testing
• Test radiation hardness
Analog Design
Based on the new geometry $C_{det}$ of 100fF maximum is assumed.

- Leakage current compensation a la FEI4 (not shown), 10nA nominal
- 5b (4b + sign) tuning DAC
- Few different variants are considered
- Globally settable feedback cap (2bit). CF0/CF1 become CF0'/CF1' in some variants
- Target total analog current is <5uA/pixel
• Simple straight cascade configuration
• Could operate at very low currents
• Only 2 Bias lines
• All devices are isolated from substrate
• A mix of transistor flavours

• Threshold adjusted by unbalancing differential output
50um Analog pixel

- A FE surrounded by digital
- Shielding and isolation necessary
- Optimized for binary operation
- Analog info provided by TOT
- Several variants and hooks to optimize for different scenarios
- Some large chip considerations have been taken into account
- Power lines are such that DV~5mV for a column of 336 rows @ 5uA/pixel
A 2X2 Pixels (quad) – “analog islands”

Digital “donut” Blanket DeepNwell

Digital section

Analog section
Digital Design
Evolution of Front End array organization

**Traditional Design**
- Make 1 pixel
- Step and Repeat identical copies
- Custom made digital

**More Recently**
- Make few-pixel region
- Step and Repeat identical copies
- Synthesized digital

**New Approach**
- Synthesized digital “core” containing a large number of analog pixels (256 in FE65P2)
Recalling Region Logic and Double Column in FE-I4

Region Logic

- analog
- digital

- hit processing
- ToT counter
- ToT memory
- latency counter
- trigger/readout

Double Column

- Token
- Bus

End of Chip Logic
Buffering efficiency

- very simple simulation assuming:
  - random distribution of hits (worst case)
  - 50x50um pixels
  - FE-I4 like architecture (2x2 pixels)

<table>
<thead>
<tr>
<th>trigger latency [us]</th>
<th>hit rate [GHz/cm²]</th>
<th>memory locations</th>
<th>inefficiency [%]</th>
<th>avr. mem occupancy</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>2</td>
<td>7</td>
<td>0.2</td>
<td>1.4</td>
</tr>
<tr>
<td>10</td>
<td>3</td>
<td>7</td>
<td>2.3</td>
<td>1.9</td>
</tr>
<tr>
<td>10</td>
<td>3</td>
<td>8</td>
<td>0.9</td>
<td>1.9</td>
</tr>
<tr>
<td>20</td>
<td>2</td>
<td>7</td>
<td>6.4</td>
<td>2.3</td>
</tr>
<tr>
<td>20</td>
<td>2</td>
<td>9</td>
<td>1.1</td>
<td>2.4</td>
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FE65-P2 Overview

- 4 pixels per region
- 7 Latency memories (stores up to 7 hit arrival times for the region) allows to reach 10µs latency with 50kHz/pixel hit rate with <1% loss
- 4-bit ToT (Time over Threshold) counting per pixel
- Code adapted from FE-I4
- Note 7 latency buffers compared to 5 in FE-I4, but 1/5 the area!
• OpenAccess mixed signal (modified flow CERN)
• Hierarchical
• We use Cliosoft SoS and git

Timing: ETS/AAE: ECSM, - PrimeTime: CCS
Multi column flow:

- Synthesize region
  - Equivalence
- Synthesize multi column (region fixed)
  - Equivalence
- Place & Route (floorplan, place, cts, route, opt)
  - Equivalence
- Export abstract, .lib files, qrc extraction
  - Check timing with primetime and export delay files for simulation

Flat 64x4 pixel core/column!
(every pixel is potentially different)
Timing: ok
Density: 85%
Power: 1.4mA (5.5uA/pixel)
Data Flow

Global signals:
- bunch crossing clock
- 2x 9bit LatnecyId (distance of latency)
- 2x 4bit TriggerId/TriggerRequestId
- trigger
- Readout based on single token for full chip
- Support for 16 consecutive triggers
- Output data format similar FE-I4 24 bit words:
  - Column, Row, 2xToT
Assembly in hierarchical flow

- Synthesize core (multi column fixed)
  - Equivalence
- Place & Route (multi column and analog/DACs/power as macro)
  - Equivalence + timing
- Assembly flat design (no hierarchy)
  - Timing (also with prime time)
- Simulation with flat delay annotated design

- Pads are added at the end (we have to have some custom pad ring for now)
Exactly the same python code can be used for testing physical chip. Same firmware for FPGA (ready to use by USBpix/GPAC).
Testing
Readout System

Multi I/O board
- General Purpose Adapter Card (GPAC), programmable power, DACs, level shifters
- Chip on the DUT (Device Under Test) board
- Python-based software/firmware framework (Basil -> https://github.com/SiLab-Bonn/basil)
- Test software and firmware: https://github.com/SiLab-Bonn/fe65_p2

Yarr:
- Based on commercial PCIe card (SPEC) with custom adapter board for FE65-P2
- Onboard voltage and current source
- Programmable injection pulser
- C++ based YARR software used to run scans https://github.com/yarr/yarr/tree/fe65_p2
• Seeing very small amount of failing pixels
• Tested multiple (10) chips by now, all show similar performance

• Data output tested up to 160MHz, issues with level shifting more than 160MHz down to 1.2V CMOS
Missed digital injection (100 inj. x 4096pix, readout@160Mbit/s)

- Designed for 40MHz @ 1.2V
- Wide range of operation

Level shifter failing

BX clock (MHz)

C. Gottardo
Threshold scan (untuned)

all s-curves

trigger delay

Injection [arb.]
Threshold and Noise (untuned)

Threshold Distribution

- mean = 640e-
- rms = 222e-

Noise Distribution

- mean = 33.4e-
Tuning the Threshold Using Noise Hits
(no charge injection)

Procedure:
- Set pixel TDACs to minimum and global threshold
- DAC very low, such that the threshold is below the noise level
- Increase the TDAC of each pixel until its noise occupancy drops below a certain threshold
- Tuning stops when the minimum global threshold is reached or more than 4 pixels reach the maximum TDAC setting
- After tuning the global threshold DAC is raised to be able to measure the threshold better
Noise Tuning – Threshold (64x8 pixels)

Without sensor!

**Untuned**

- mean = 645e-
- rms = 204e-

**Tuned**

- mean = 219e-
- rms = 30e-

vff = 24.7uA@1.2V
Noise Hit Rate:
• Measuring noise hit rate via hitOr
• Enabling a group of pixels with similar threshold
• Steadily decreasing global threshold DAC and measure hit frequency
• Repeat measurement with digital clock on and off
• If the isolation of the analog front end from the digital region is not good enough expecting noise hit rate to increase earlier
• Can not see difference in noise hit rate with clock on or off
• Need to repeat this with a properly tuned chip and masked hot pixels!
Conclusion

- **FE65-P2 works!** Tested multiple chips and all show good performance
- Characterisation started and first measurements of ENC are close to simulation
- Preliminary tunings successful
- Chip shows stable performance in temperature range from 0°C to 40°C
- First measurements indicate analog isolation strategy is successful, but need to be checked more in-depth
- Many more unirradiated, bare this test results available - all look good.
- Chips have been irradiated with protons to 150, 350, and 500 Mrad and preliminary results look good, but tests in progress.
- Very first miniature module with planar n on p sensor was wire bonded on 27/May! - results coming soon.
Thank you