Pixels for ALICE tracker upgrade

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on behalf of the ALICE collaboration
Objectives

Improve impact parameter resolution by a factor of 3 (5) in $r-\phi$ ($z$) at $p_T = 500$ MeV/c

- Get closer to IP (radius of first layer):
  
  
  $39 \text{ mm} \rightarrow 23 \text{ mm}$

- Reduce pixel size:
  
  $50 \, \mu \text{m} \times 425 \, \mu \text{m} \rightarrow O(30 \, \mu \text{m} \times 30 \, \mu \text{m})$

- Reduce $x/X_0$/layer:
  
  $\sim 1.14\% \rightarrow \sim 0.3\%$ (inner layers)

Better tracking efficiency and $p_T$ resolution at low $p_T$

- Finer granularity:
  
  from 6 to 7 layers and all layers with pixels

Fast readout

- Readout Pb-Pb interactions at 100 kHz
- Readout pp interactions at $>200$ kHz
  
  (current ITS limited at 1 kHz)

Design for fast removal and insertion

- Maintenance during yearly shutdown

Installation of the new ITS during LHC Long Shutdown 2 (2019 - 2020)
New ALICE ITS layout

~24000 CMOS Pixel Sensors
10 m² sensitive area
12.5 Gpixels

Coverage
23 mm < r < 400 mm, |η| < 1.22
Layers z-lengths: 27 - 150 cm
## ITS Chip General Requirements

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Inner Barrel</th>
<th>Outer Barrel</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip size (mm x mm)</td>
<td>15 x 30</td>
<td></td>
</tr>
<tr>
<td>Chip thickness (μm)</td>
<td>50</td>
<td>100</td>
</tr>
<tr>
<td>Spatial resolution (μm)</td>
<td>5</td>
<td>10 (5)</td>
</tr>
<tr>
<td>Detection efficiency</td>
<td>&gt; 99%</td>
<td></td>
</tr>
<tr>
<td>Fake hit rate</td>
<td>&lt; $10^{-5}$ evt$^{-1}$ pixel$^{-1}$ (ALPIDE $&lt;&lt; 10^{-5}$)</td>
<td></td>
</tr>
<tr>
<td>Integration time (μs)</td>
<td>&lt; 30</td>
<td>&lt; 10</td>
</tr>
<tr>
<td>Power density (mW/cm$^2$)</td>
<td>&lt; 300 (~35)</td>
<td>&lt; 100 (~20)</td>
</tr>
<tr>
<td>TID radiation hardness (krad) (**):</td>
<td>2700</td>
<td>100</td>
</tr>
<tr>
<td>NIEL radiation hardness (1 MeV n$_{eq}$/cm$^2$) (**):</td>
<td>$1.7 \times 10^{13}$</td>
<td>$1.7 \times 10^{12}$</td>
</tr>
<tr>
<td>Readout rate, Pb-Pb interactions (kHz)</td>
<td></td>
<td>100</td>
</tr>
<tr>
<td>Hit Density, Pb-Pb interactions (cm$^{-2}$)</td>
<td>18.6</td>
<td>2.8</td>
</tr>
</tbody>
</table>

(*) In color: ALPIDE performance figure where better than requirements
(**) 10x radiation load integrated over approved program (~ 6 years of operation)
Technology

- TowerJazz 180 nm CMOS imaging process
- Gate oxide 3 nm thick, good for TID tolerance
- High-resistivity (> 1kΩ cm) p-type epitaxial layer (18 µm to 30 µm) on p-type substrate
- Deep PWELL shielding NWELL allowing in-pixel PMOS: circuits beyond rolling shutter

Substrate reverse bias to increase depletion volume around the collection electrode

- Better tolerance to non-ionizing radiation
- Lower input capacitance $C_{in}$
- Smaller cluster => more charge $Q$ in the central pixel

High $Q/C_{in}$ allows for a lower power circuit for a given S/N (Signal over Noise) for a given bandwidth

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No free running clock over matrix. No activity if there are no hits
=> power and system noise reduction

In pixel:
Amplification
 Discrimination
3 hit storage registers (MEB)

In matrix:
Zero suppression readout based on priority encoding:
sequential readout of hit pixels address
In pixel hit discrimination and storage

- Analog front-end continuously active, acts as an analogue delay line (~2 µs peaking time)
- Global threshold for discrimination => binary pulse OUT_D
- Digital in-pixel circuitry with three hit storage registers (multi event buffer)
- Global shutter (STROBE) latches the discriminated hits in next available register
Sensor configuration and reset

- Sensor NWELL collection electrode
  - Octagonal shape with 2 μm diameter
  - Spacing between NWELL and PWELL: 3 μm (spacing vs circuit area trade-off)
- Reset mechanism
  - Diode reset: p+ in NWELL, Reset current depends on the sensor leakage and signal amplitude
  - PMOS reset:
    - Reset current limited by IRESET (> leakage) → control on the reset circuit conductance
    - Additional capacitance on node PIX_IN

ALPIDE implements diode reset

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Front-end operation principle

- Signal charge creates negative voltage step $\Delta V_{\text{PIX}_\text{IN}}$ at the input (PIX_IN)
- M1 with current source from VDDA acts as a follower and forces source to follow gate.
- This causes transfer of charge $Q_{\text{source}} = C_{\text{source}} \cdot \Delta V_{\text{PIX}_\text{IN}}$ from $C_{\text{source}}$ to $C_{\text{OUT}_A}$

- Ideally:

  $$\Delta V_{\text{OUT}_A} \approx \frac{Q_{\text{source}}}{C_{\text{OUT}_A}} = \frac{C_{\text{source}} \cdot \Delta V_{\text{PIX}_\text{IN}}}{C_{\text{OUT}_A}} = \frac{C_{\text{source}}}{C_{\text{OUT}_A}} \Delta V_{\text{PIX}_\text{IN}} = \frac{C_{\text{source}}}{C_{\text{OUT}_A}} \frac{Q_{\text{IN}}}{C_{\text{IN}}}

- Voltage gain is obtained if:

  $$C_{\text{source}} \gg C_{\text{OUT}_A}$$
In practice need feedback (to curfeed)

- curfeed net: To set M3 gate voltage level to allow IBIAS+ITHR current
- ITHR, VCASN: To define the OUT_A baseline voltage level below where I_{M8} = IDB
- ITHR defines the return to baseline of OUT_A after hit

Active low output (OUT_D): M8 current (defined by OUT_A) > IDB

The front-end works in weak inversion to reduce power consumption

- IBIAS = 20 nA, ITHR = 0.5 nA → ~40 nW (1.8 V supply voltage)

Front-end circuit - 1

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Front-end circuit - 2

- Combined capacitance to reduce layout area
  - $C_{\text{source}}$ and $C_{\text{curfeed}} \rightarrow Cs$

- Charge threshold parameters
  - OUT_A baseline value: ITHR, VCASN
  - Threshold of second stage: IDB

- Clipping transistor M6
  - Large input pulse compression
  - VCLIP to tune the clipping point
Device sizing optimized to improve charge threshold and pulse duration uniformity

First stage input PMOS (M1): trade-off on input capacitance vs RTS noise
- option (a): $W = 0.22 \, \mu m$, $L = 0.18 \, \mu m$ (minimum size)
- option (b): $W = 0.92 \, \mu m$, $L = 0.18 \, \mu m$ (~ 4 times minimum width)

Second stage input NMOS (M8): trade-off on $C_{OUT_A}$ and uniformity

Simulation: limited accuracy of transistor capacitance values in weak inversion
In trigger mode the front-end is used as analogue memory:
- hit information kept up to STROBE arrival

- The signal is latched only when both STROBE and OUT_D are active at the same time.
  - STROBE window can be defined to latch all charges above threshold:
    - STROBE delay has to be larger than the trigger latency (1.6 µs)
    - Pulse timing rms variations have to be taken into account (error bars at 5 sigma)

```
<table>
<thead>
<tr>
<th>Q_{in}</th>
<th>t1 [µs]</th>
<th>t2 [µs]</th>
</tr>
</thead>
<tbody>
<tr>
<td>50 e^-</td>
<td>2.9 ± 0.20</td>
<td>3.9 ± 0.52</td>
</tr>
<tr>
<td>100 e^-</td>
<td>1.5 ± 0.16</td>
<td>5.9 ± 0.24</td>
</tr>
<tr>
<td>150 e^-</td>
<td>0.9 ± 0.03</td>
<td>5.7 ± 0.09</td>
</tr>
<tr>
<td>5 ke^-</td>
<td>0.5 ± 0.01</td>
<td>2.6 ± 0.07</td>
</tr>
</tbody>
</table>
```
Pixel matrix layout

Pixel layout

Collection diode
- 2 µm nwell width
- nwell-pwell spacing 3 µm

Electrode

Pixel Logic:
- 3 pixel state registers
- 2 Configuration bits:
  - Pixel pulsing
  - Pixel masking

Front end

Pixel matrix

• 2 µm nwell width
• nwell-pwell spacing 3 µm

Priority encoder

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ALPIDE chip

Matrix sensitive area (512 x 1024 pixels)  
Analog DACs  
Digital Periphery  
Soldering pads

Regular Pads + Custom Blocks: LVDS, MLVDS, CMOS I/O, Bandgap, monitoring ADC

Sensitive area (4.12 cm²) power density 6.2 mW/cm²
Chip power density < 35 mW/cm² (20 mW/cm² with readout from parallel port)
Full scale prototype characterization

- Since end 2011, 4 MPWs and 5 engineering runs.
- Small scale prototypes for sensor optimization
- Full scale ALPIDE prototypes (1024 x 512 pixels)
  - pALPIDE-3 (back from foundry in October 2015)

8 sectors with different sensor design and front-end options
128 columns/sector
512 rows/column
width 3.74 mm/sector

55Fe Radioactive source
Threshold and noise distribution

- Results from test charge injection (nominal setting, substrate bias = 0 V)
- Error function (S-Curve) fit:
  - Charge threshold: \((67 \pm 14)\) e-
  - Noise: \((4.1 \pm 1.2)\) e-
Test beam: input transistor size vs RTS noise

First stage input PMOS (M1):
- pALPIDE-3a): $W = 0.22 \, \mu m$, $L = 0.18 \, \mu m$ (minimum size)
- pALPIDE-3b): $W = 0.92 \, \mu m$, $L = 0.18 \, \mu m$ (~ 4 times minimum width)

Same noise level from test charge injection but different fake hit rate => RTS noise

Larger input transistor size reduces significantly RTS noise
Larger reverse bias and spacing increases detection efficiency (larger depletion volume)
Resolution of 5 µm achieved
Cluster size: between 2 and 3 pixels
Test beam: TID effect

Efficiency & Fake-hit Rate vs. ITHR, $V = -3V$

Performance up to specifications, ionizing radiation 312 krad
Performance up to specifications, non ionizing radiation $1.7 \times 10^{13}$ 1 MeV $n_{eq}/cm^2$
Conclusions

ALPIDE chip is the CMOS Pixel Sensor that will equip the new ALICE ITS
15 mm × 30 mm, 512 × 1024 pixels, 29 µm x 27 µm pitch

Sensor design optimized for Q/C_in:
  - diode reset, 3 µm collection NWELL to PWELL spacing
Possibility to apply reverse bias:
  - further capacitance reduction and non-ionizing radiation tolerance increase

Ultra-low power front-end (40 nW/pixel, 2 µs peaking time).
In pixel discrimination and zero suppressed read-out
  - Sensitive area (4.12 cm²) power density 6.2 mW/cm² (full chip < 35 mW/cm²)

Full scale prototype performance up to specifications in test beams with large operation margin

ALPIDE final design submitted in May 2016
Description of injection capacitance and layout

Pulsing capacitor (0.23 fF) cross section

Metal3
0.64μm
0.64μm

Metal4
1.28μm
1.54μm
FRONT END OPTIMIZATION: parasitic components

- Parasitic components impact threshold, to mitigate use cascode to reduce Miller effect
  - Variation of parasitic capacitance amplified by miller effect
- Effect of $C_{P1}$ mismatch variation on $Q_{thr}$ reduced by factor 4
  (rms from transistor: $1.7 \text{e}^{-} < $ without cascode: $2.2\text{e}^{-}$)

< Sensitivity of the Charge threshold on $C_{P1}$ >

- Extracted $C_{P1}$ value: $0.38 \text{fF} \rightarrow 25\%$ variation: $0.1 \text{fF}$
- Without cascode [M9]:
  \[
  \frac{d Q_{thr}}{d C_{P1}} = \frac{2.2 \text{e}^{-}}{0.1 \text{fF}}
  \]
- With cascode [M9]:
  \[
  \frac{d Q_{thr}}{d C_{P1}} = \frac{0.6 \text{e}^{-}}{0.1 \text{fF}}
  \]
From Monte Carlo simulation optimize device sizing according to influence on charge threshold

\[ A_{tot} = \sum_{i=0}^{9} A_i \quad \rightarrow \text{Total area fixed} \]

\[ \text{rms} = \frac{\text{rms0}}{\sqrt{\text{AREA}}} \quad \rightarrow \text{rms0 depends on circuit} \]

\[ \text{rms}_{tot} = \sqrt{\sum_{i=0}^{9} \left( \frac{\text{rms0}_i}{A_i} \right)^2} \quad \rightarrow \text{Weighted sum of squares} \]

\[ A_{R E A} \quad \rightarrow \text{Large area required} \]

\[ \text{Area distribution is important} \]

<table>
<thead>
<tr>
<th>Device</th>
<th>W/L [\mu m/\mu m]</th>
<th>Area [\mu m^2]</th>
<th>rms [e]</th>
</tr>
</thead>
<tbody>
<tr>
<td>M0</td>
<td>1.8/8.5</td>
<td>15.3</td>
<td>0.69</td>
</tr>
<tr>
<td>M1</td>
<td>0.92/0.18</td>
<td>0.16</td>
<td>0.14</td>
</tr>
<tr>
<td>M2</td>
<td>0.22/0.18</td>
<td>0.04</td>
<td>0.14</td>
</tr>
<tr>
<td>M3</td>
<td>0.5/5</td>
<td>2.5</td>
<td>0.14</td>
</tr>
<tr>
<td>M4</td>
<td>2/8.4</td>
<td>16.8</td>
<td>1.13</td>
</tr>
<tr>
<td>M5</td>
<td>0.5/10</td>
<td>5</td>
<td>0.41</td>
</tr>
<tr>
<td>M6</td>
<td>0.5/3</td>
<td>1.5</td>
<td>0.14</td>
</tr>
<tr>
<td>M7</td>
<td>0.42/7</td>
<td>2.94</td>
<td>0.2</td>
</tr>
<tr>
<td>M8</td>
<td>0.22/4</td>
<td>0.88</td>
<td>0.62</td>
</tr>
<tr>
<td>M9</td>
<td>0.42/0.2</td>
<td>0.08</td>
<td>0.14</td>
</tr>
<tr>
<td>Cs</td>
<td>Cap. : 344 fF</td>
<td>43.09</td>
<td>0.14</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Version</th>
<th>Q_{thr} [e-]</th>
<th>rms [e-]</th>
<th>Q_{thr} [e-]</th>
<th>rms [e-]</th>
</tr>
</thead>
<tbody>
<tr>
<td>pALPIDE-3</td>
<td>78</td>
<td>1.7</td>
<td>92</td>
<td>2.0</td>
</tr>
</tbody>
</table>
**FRONT END: Pulse duration uniformity**

Important as front end is used as analog memory

\[
\frac{dv_{OUT_A}}{dt} = \frac{I_{Discharge}}{C_{OUT_A}} = I_{THR} + I_{M6}
\]

**OUT_A**
- Wide M4 to reduce \(I_{THR}\) variation
- Long M6 (clipping transistor) to reduce the clipping point variation
- Cascode transistor\([M9]\) to reduce \(C_{OUT_A}\) variation (Miller Effect)

**OUT_D**
- Wide M7 to reduce \(I_{DB}\) variation

\[
\frac{dv_{OUT_D}}{dt} = \frac{I_{DB}}{C_{OUT_D}}
\]
2 Configuration bits:
- Pixel pulsing
- Pixel masking

Signals buffered from the periphery

Front-end binary output
- PIX_OUT_B
- STROBE_B<2:0>
- FLUSH_B<2:0>
- MEMSEL_B<2:0>
- PIX_RESET

Input from priority encoder

3 Pixel State registers

Charge injection pulse

Output to priority encoder
### 8 different sectors for pALPIDE-3

<table>
<thead>
<tr>
<th>Sector</th>
<th>M3, M5, M6, M8</th>
<th>VCASN2 (M9)</th>
<th>Clipping M6 gate</th>
<th>M1 bulk</th>
<th>Reset</th>
<th>Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>optimized size</td>
<td>Yes</td>
<td>diode conn.</td>
<td>AVDD</td>
<td>Diode</td>
<td>2 µm</td>
</tr>
<tr>
<td>1</td>
<td>optimized size</td>
<td>No</td>
<td>diode conn.</td>
<td>AVDD</td>
<td>Diode</td>
<td>2 µm</td>
</tr>
<tr>
<td>2</td>
<td>as in pALPIDE-1/2</td>
<td>No</td>
<td>diode conn.</td>
<td>AVDD</td>
<td>Diode</td>
<td>2 µm</td>
</tr>
<tr>
<td>3</td>
<td>optimized size</td>
<td>Yes</td>
<td>VCLIP</td>
<td>AVDD</td>
<td>Diode</td>
<td>2 µm</td>
</tr>
<tr>
<td>4</td>
<td>optimized size</td>
<td>Yes</td>
<td>VCLIP</td>
<td>Source</td>
<td>Diode</td>
<td>2 µm</td>
</tr>
<tr>
<td>5</td>
<td>optimized size</td>
<td>Yes</td>
<td>VCLIP</td>
<td>Source</td>
<td>Diode</td>
<td>3 µm</td>
</tr>
<tr>
<td>6</td>
<td>as in pALPIDE-1/2</td>
<td>No</td>
<td>diode conn.</td>
<td>AVDD</td>
<td>PMOS</td>
<td>2 µm</td>
</tr>
<tr>
<td>7</td>
<td>optimized size</td>
<td>Yes</td>
<td>VCLIP</td>
<td>AVDD</td>
<td>PMOS</td>
<td>2 µm</td>
</tr>
</tbody>
</table>
Pulse shape

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Default parameters for $V_{bb}=0$, sector 5, pixel 5/5

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Threshold and Noise vs ITHR

Threshold & RMS vs $I_{THR}$

Noise & RMS vs $I_{THR}$
RTS noise, pALPIDE-2

- $W_{\text{min}}$ Input transistor (Sector 0) vs. $\sim 4 \times W_{\text{min}}$ Input transistor (Sector 1)
  - Detection efficiency > 99% (specification) for both Sectors
  - Low threshold setting: Comparable noise level (Gaussian noise)
  - Nominal threshold setting:
    - Sector 1 has lower fake hit rate (lower RTS noise)

<table>
<thead>
<tr>
<th>Sec.</th>
<th>$W_{\text{M1}}$ [µm]</th>
<th>$Q_{\text{THR}}$ [e$^-$]</th>
<th>$\sigma Q_{\text{THR}}$ [e$^-$]</th>
<th>ENC [e$^-$]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0.22</td>
<td>169</td>
<td>13</td>
<td>1.8</td>
</tr>
<tr>
<td>1</td>
<td>0.92</td>
<td>150</td>
<td>9</td>
<td>1.7</td>
</tr>
</tbody>
</table>

< Hit map – random triggers >

< Fake hit rate vs ITHR >

Nominal threshold setting $I_{\text{THR}} = 500$ pA