Ultra fast single photon counting chip

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Outline

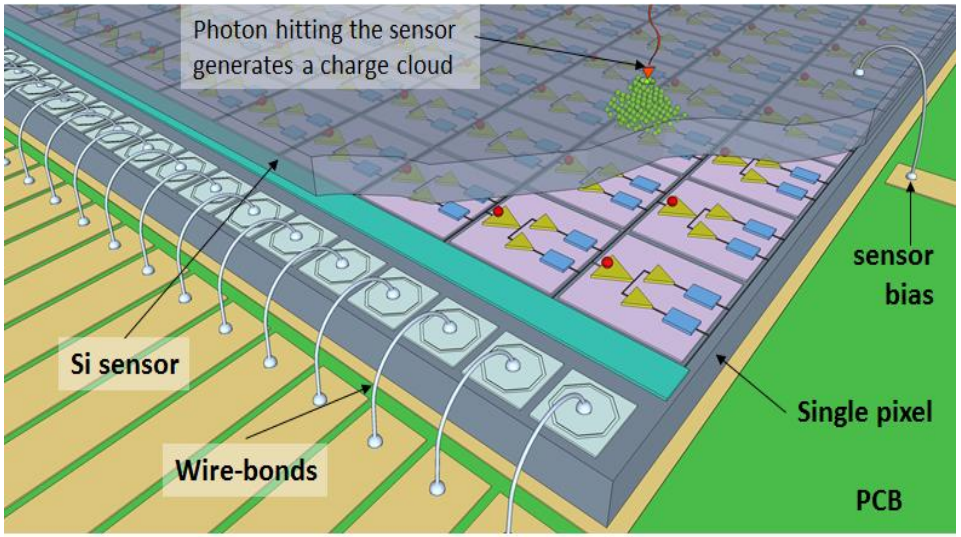
1. Motivation
   - application
   - functionality requirements

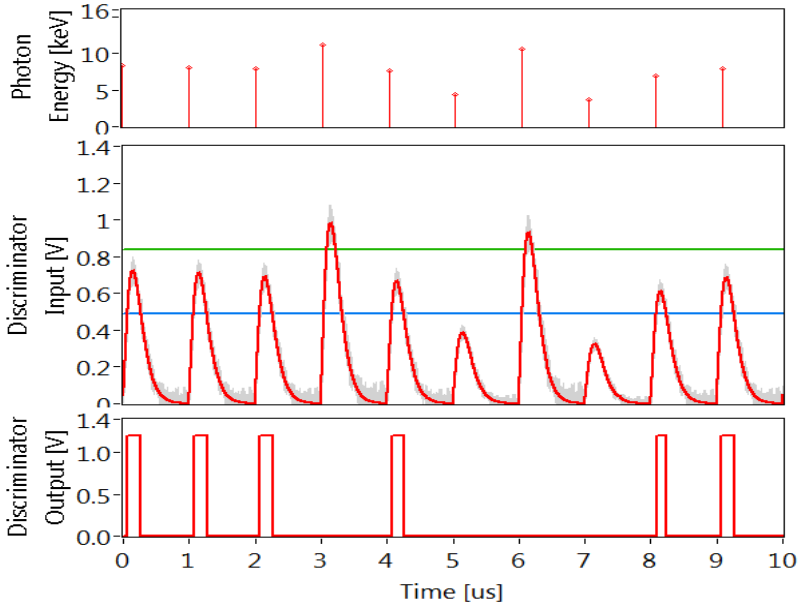
2. Readout chip architecture:
   - pixel architecture
   - operation modes

3. Measured parameters
   - offset spread
   - gain and noise
   - high count rate performance
   - continous readout and frame rate

4. Conclusions

Hybrid pixel detector for X-ray imaging





Functionality:
- single photon counting with energy window,
- input pulse: holes and electrons
- continuous readout

Critical parameters:
- pixel size 75x75 μm^2,
- good matching (offset and gain)
- high count rate per pixel & high frame rate per chip
- low noise

Readout chip architecture

UFXC32k – Ultra Fast X-ray Chip with 32k channels

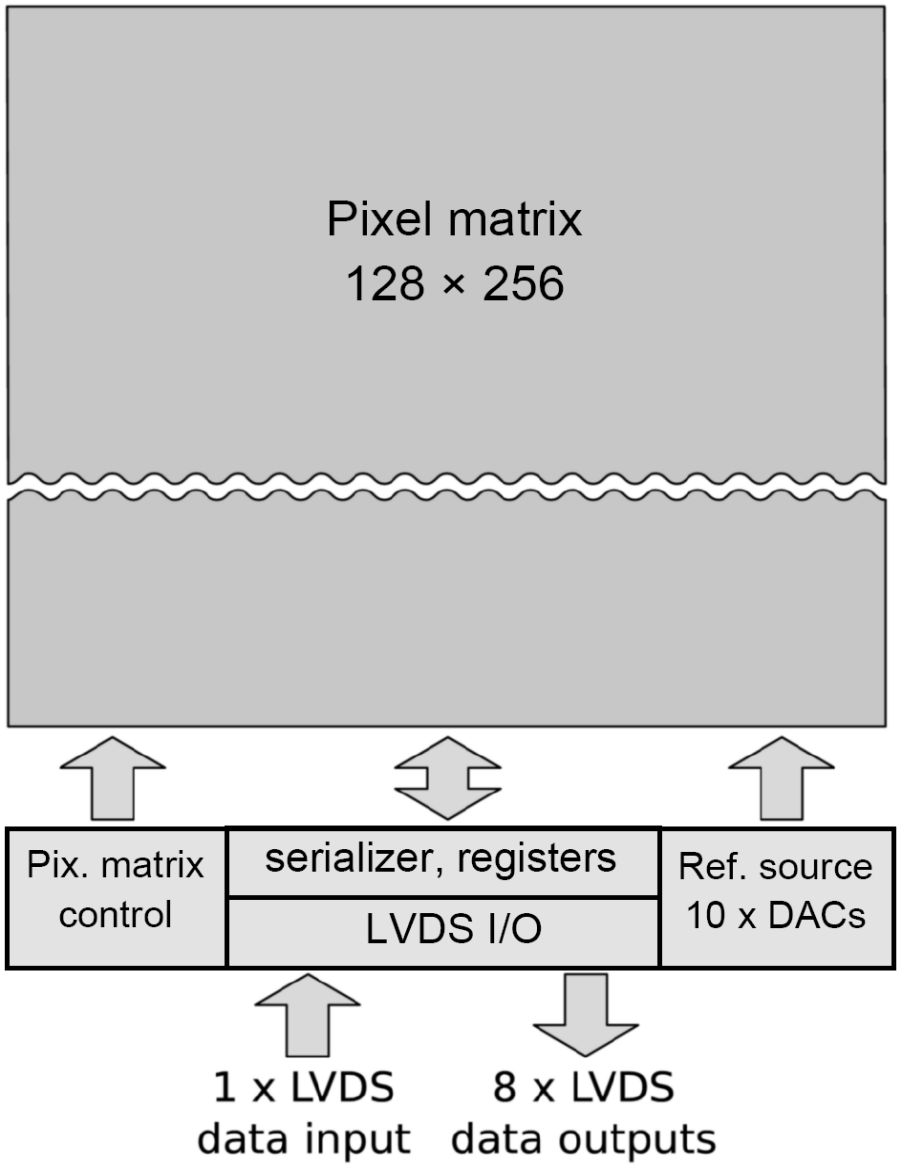
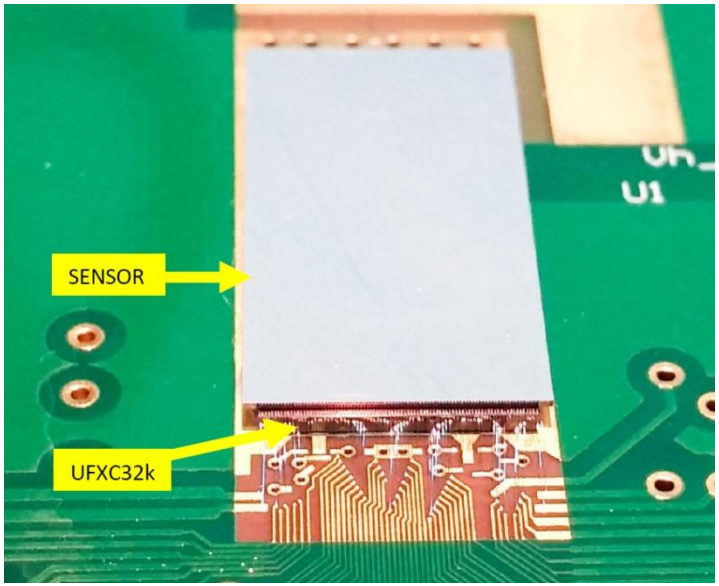


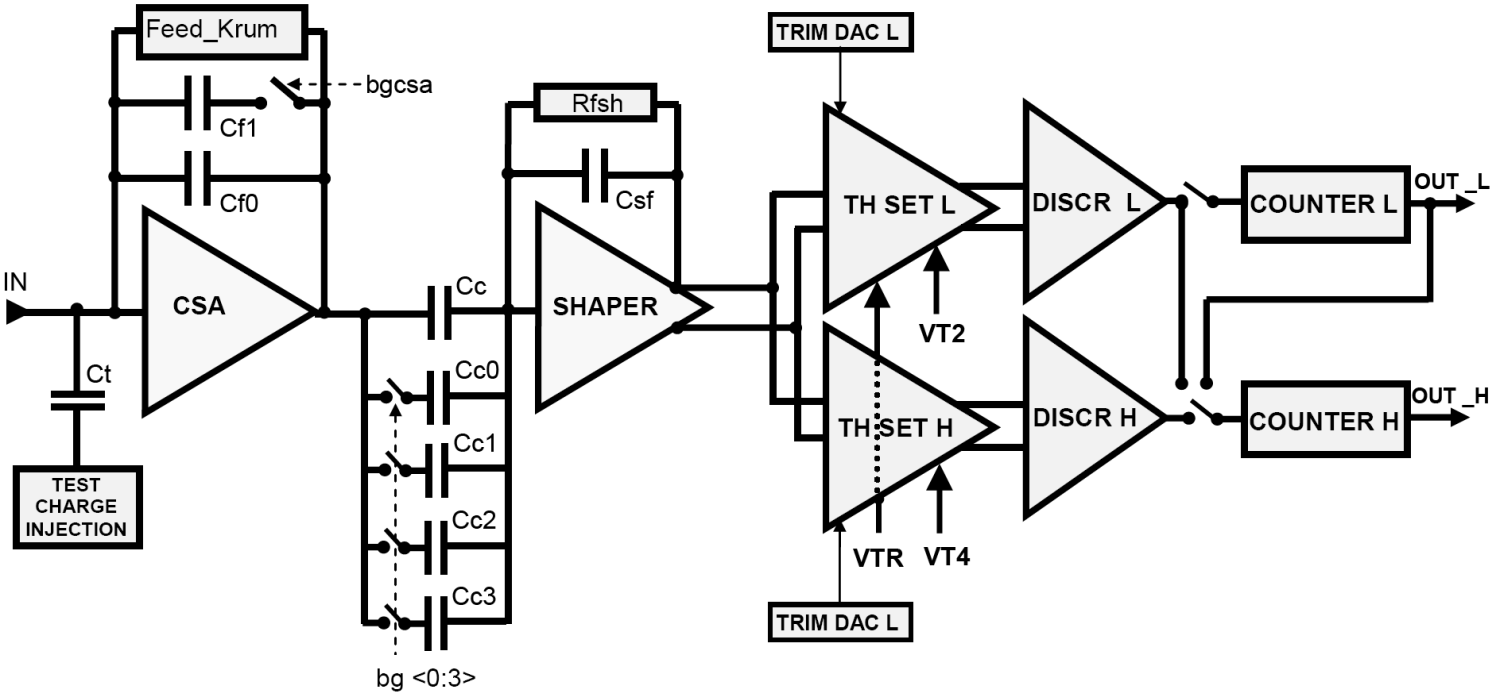
Photo of UFXC32k
with bump-bonded sensor



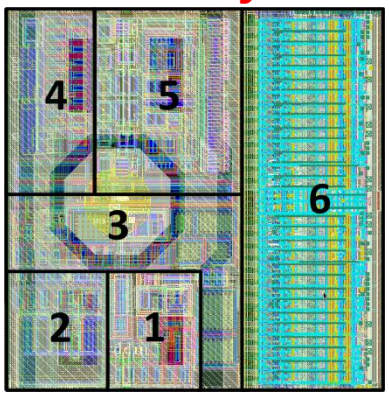
32768 pixels (75x75 μm^2)
CMOS 130 nm (~50M transistors)
chip size 9.63 × 20.15 mm^2

Single pixel architecture

Layout area: 75 × 75 μm²



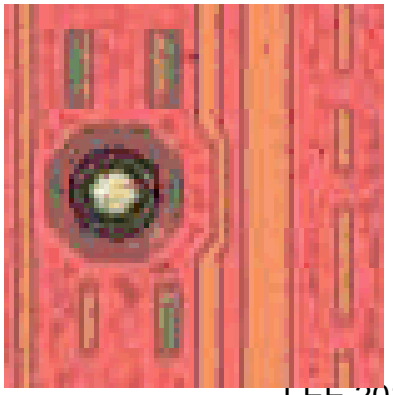
Pixel layout



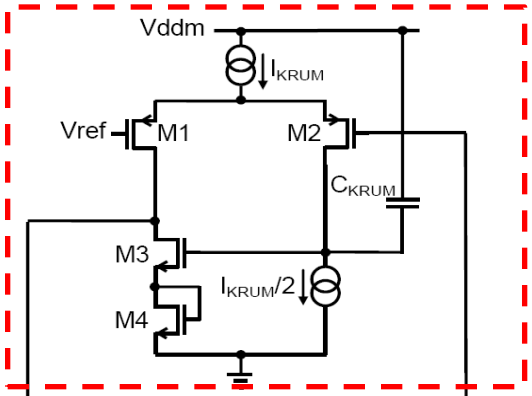
1. CSA
2. Feed_Krum
3. SHAPER
4. Refences – bias currents
5. TH_SET, TRIM_DAC
6. Counters and registers

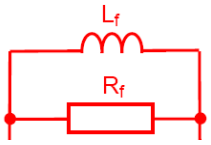
Bonding pad ϕ = 13 μm

Pixel photo



CSA & SHAPER

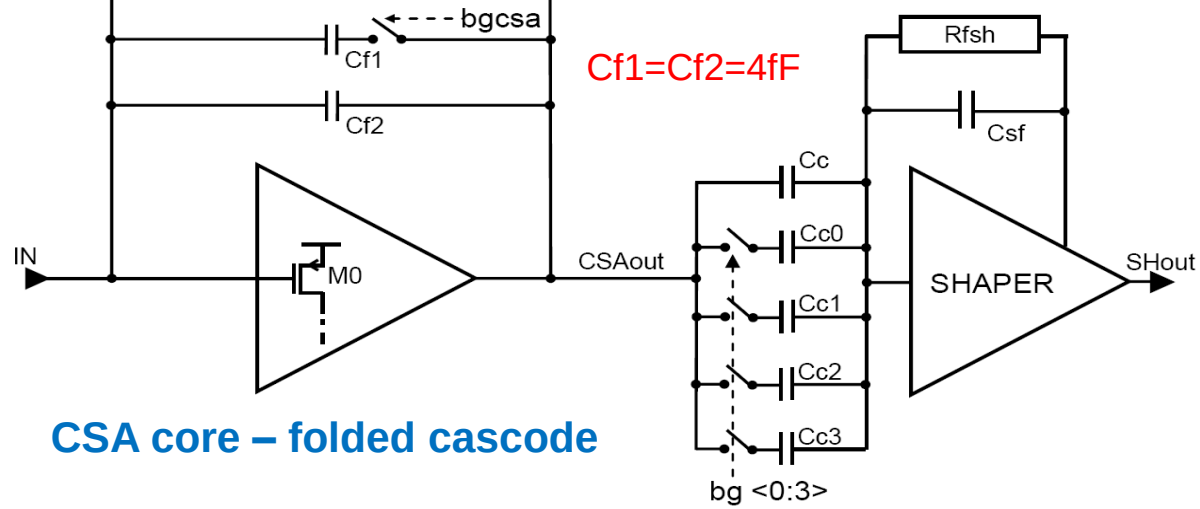




I_{KRUM}=10 nA /36nA

Rf =12.8 MΩ /3.6MΩ

Lf = 146 H /14 H

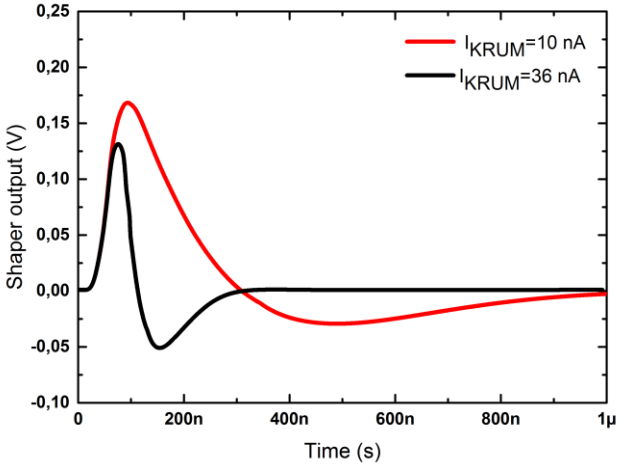


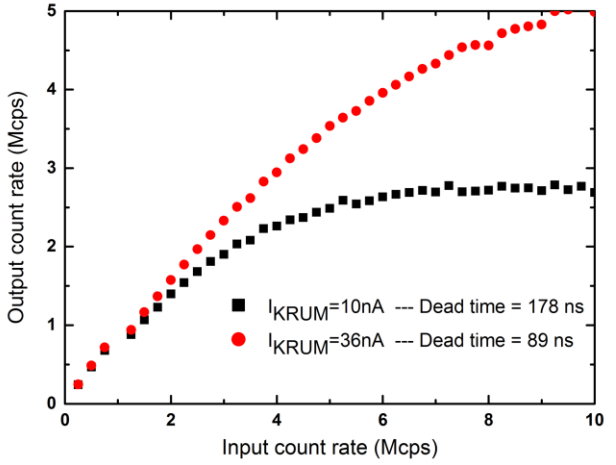
CSA core – folded cascode

Input transistor
PMOS W/L=20μm/0.15μm
IDS= 1.5 μA – 5.2 μA
(EKV model → if =0.1)

Gain tuning at shaper input
(Cc+Ccx)/Csf

Post-layout simulation



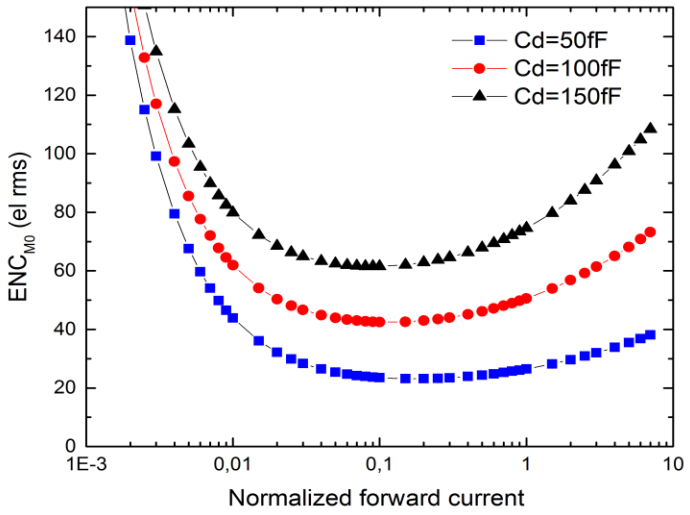


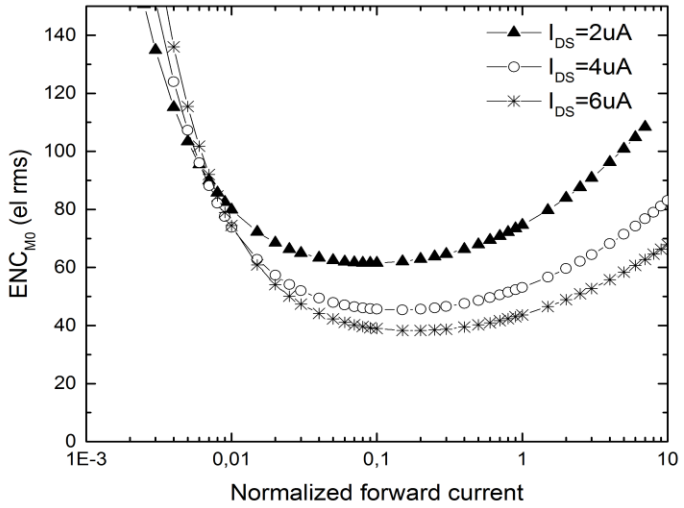
Input transistor selection

(EKV model was used)

$$\mathrm{ENC}_{\mathrm{M0}}^2 \approx \frac{F_v}{t_p}\left(C_d + C_f + C_g\right)^2 4kT\frac{\gamma}{g_m}$$

$$i_f = \frac{I_{DS}}{2n\mu\, C_{ox}(W/L)\varphi_T^2}$$



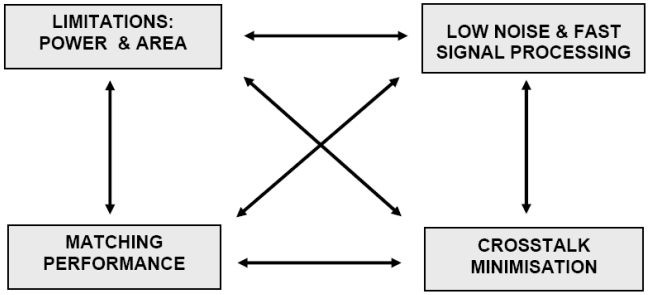


We assume L =150 nm, n = 1.3, F_v=0.92, t_p = 40 ns.

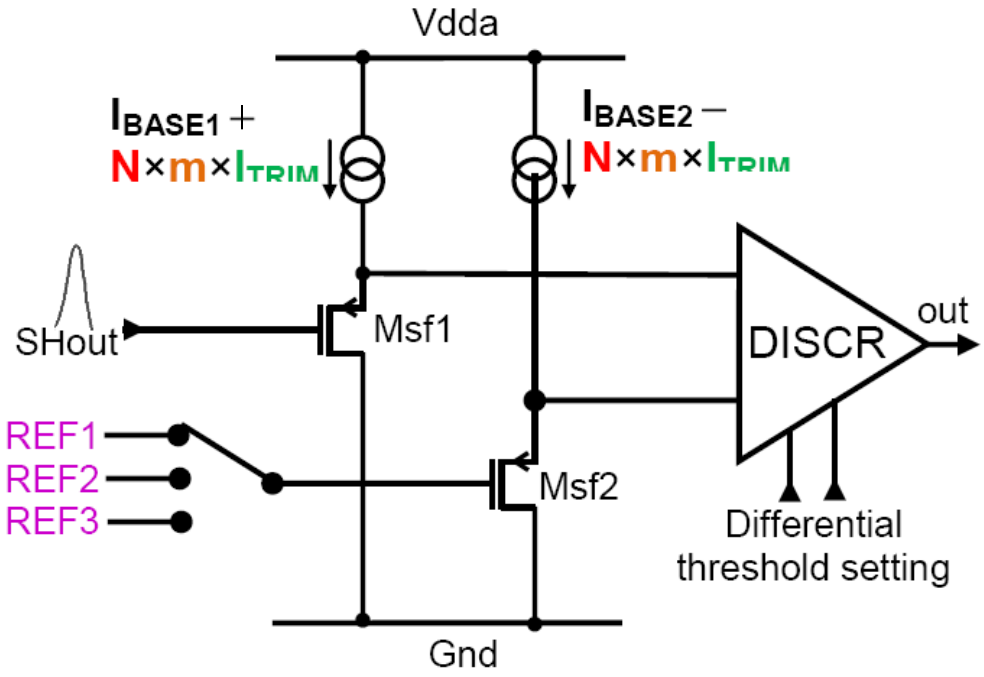
Weak inversion takes place for $i_f < 0.1$
while the strong inversion region is for $i_f > 10$

$$g_m = \frac{I_{DS}}{n\varphi_T}$$

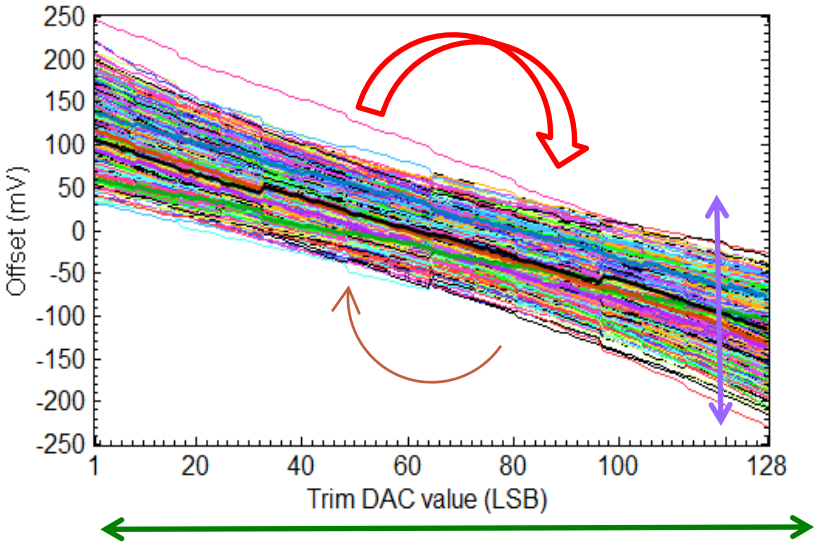
$$g_m = \sqrt{2\mu\, C_{ox}\frac{W}{L} I_{DS}}$$



Threshold trimming



TRIM DACs chracteristics (1000 MC)



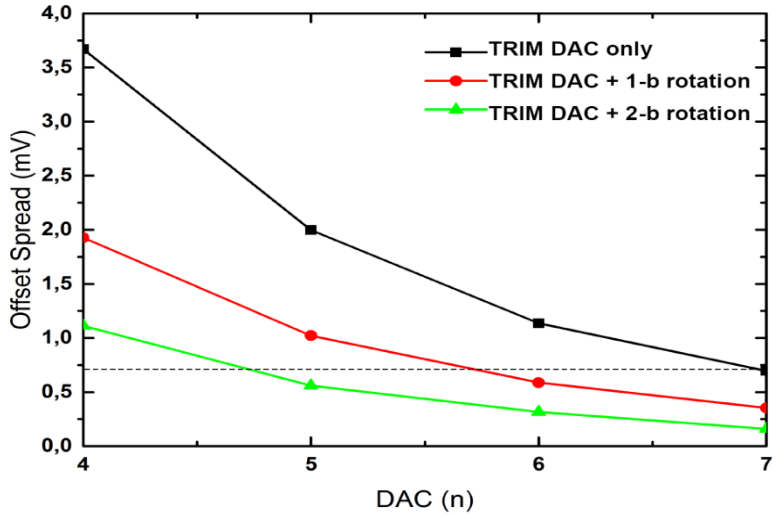
1. GLOBAL TRIM DAC RANGE

2. INDIVIDUALY IN EACH PIXEL

a) 7-bit trim DAC - I_{TRIM} current

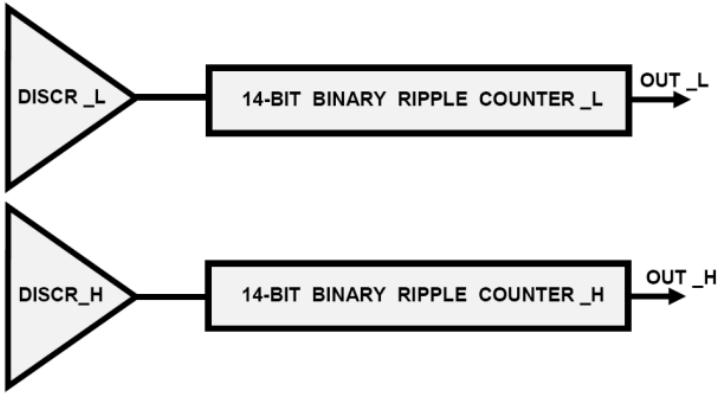
b) rotation of trim DAC characteristics

b) extra offsets (REF1-3)

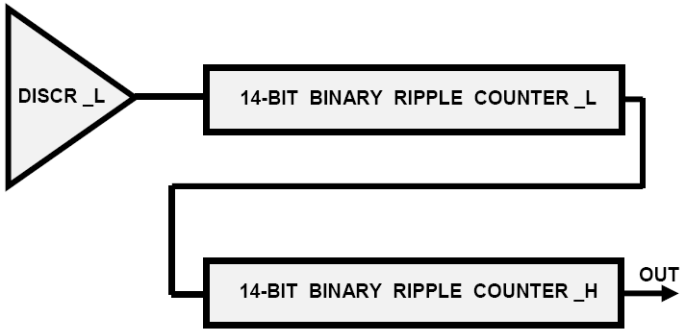


W

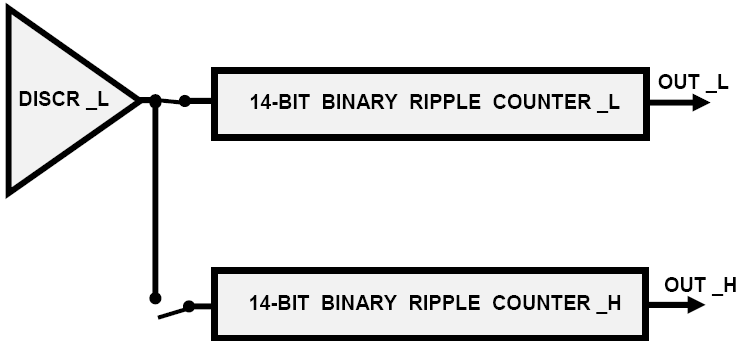
Two 14-bits counters in each pixel – 3 diffrent modes



STANDARD MODE
WITH ENERY WINDOW:
DISCR_L ⇒ COUNTER_L (14 bits)
DISCR_L ⇒ COUNTER_L (14 bits)



LONG COUNTER MODE
WITH SINGLE THRESOLD
DISCR_L ⇒
COUNTER_L + COUNTER_H (28- bits)



CONTINOUS MODE WITH SINGLE THRESOLD:
Phase 1 : DISCR_L ⇒ COUNTER_L (M-bits)
COUNTER_L (M-bits) ⇒ data readout

Phase 2: DISCR_H ⇒ COUNTER_H (M-bits),
COUNTER_L(M-bits) ⇒ data readout

Number of readout bits M can be controlled
2-4-8-14 to increase the frame rate

Tests

power consumption, functionality

The following tests were performed for UFXC32k:

- power consumption,
- functionality of the digital block,
- effective threshold spread and its correction,
- gain measurement and noise performance,
- count rate test – dead time of FEE
- continuous readout

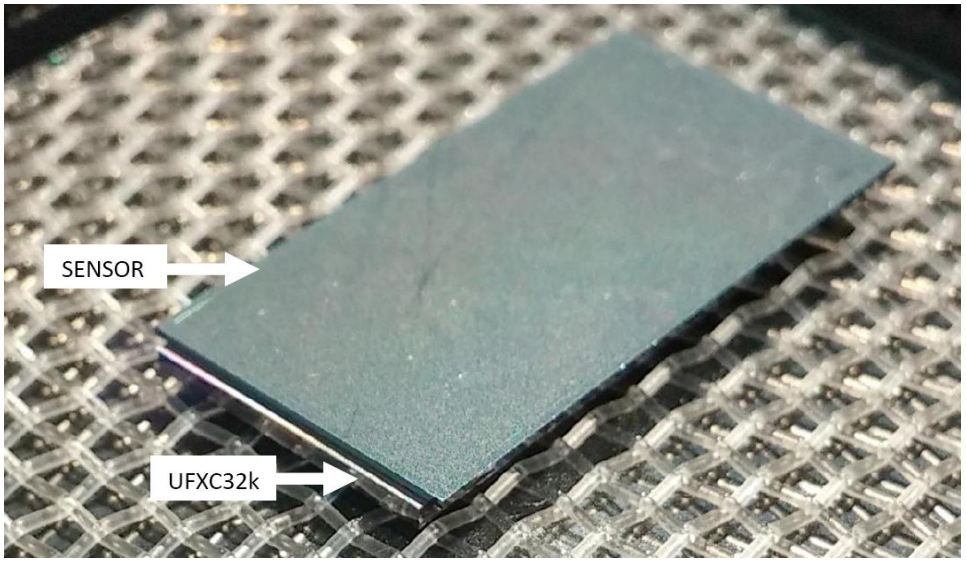
Power supply voltage:

- analog part: 0.8 V (CSA input) and 1.2V
- digital part: 1.2V (core) and 2.5V (LVDS)

Measured power consumption per pixel:
26 μW/pixel (analog part)

Functionality: OK.

LVDS input/output;
nominal frequency of 200 MHz

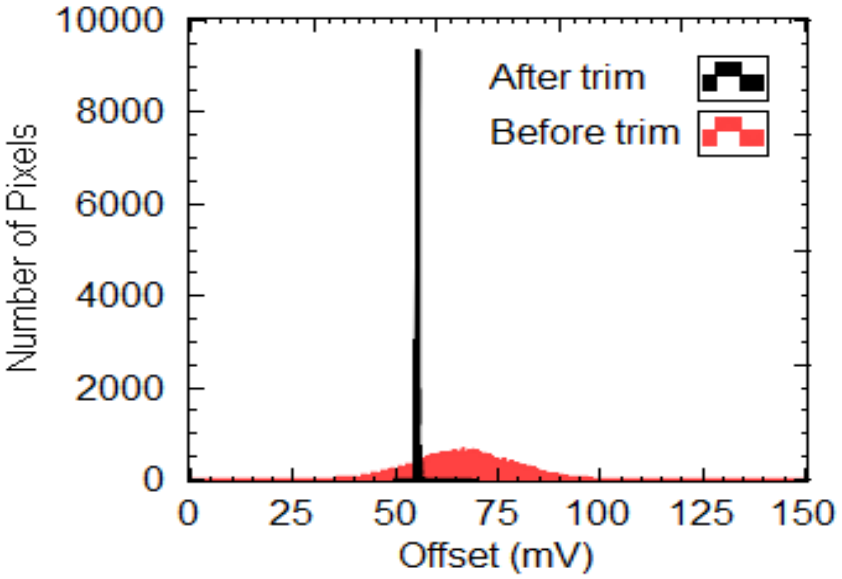


Hardware used:

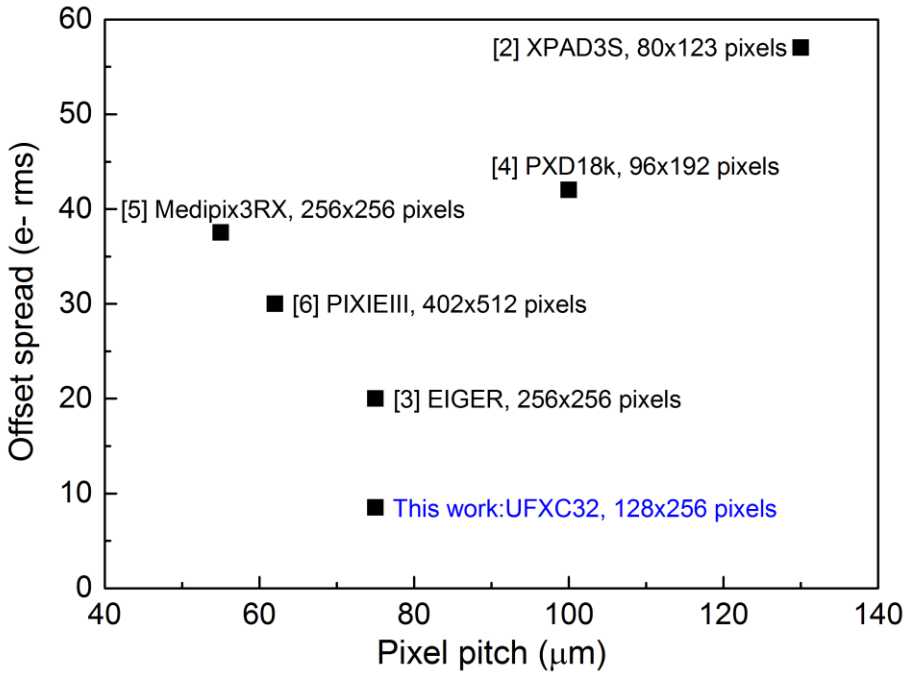
- **NI PXI-1062Q with PXIe-8106 embedded controller**
- **NI PXI-6562 - Digital Waveform Generator/Analyzer**
- **NI PXI 7975 flexRIO FPGA with 6583 LVDS interface**

DC offsets

before and after correction



Before trim: sd = 12.1 mV



After trim: sd = 0.43 mV

nominal gain ⇩

After trim: sd = 8.5 e⁻ rms

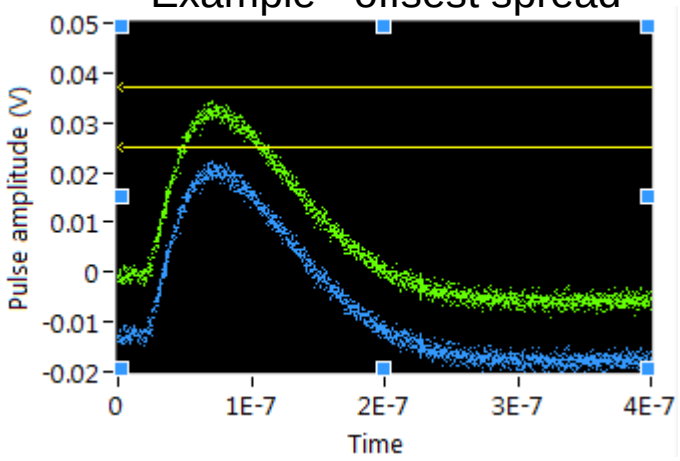
Offsets spread in large area integrated circuits working in the single photon counting mode vs. pixel pitch – reference and pixel matrix size is speficied for each solution.

Comments:
correction time: 20 - 60 sec

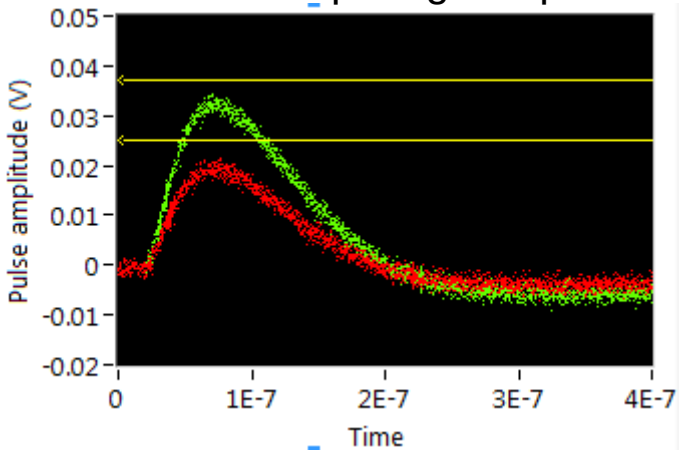
Single photon counting system

Offset usually corrected, gain should be corrected too

Example - offsest spread

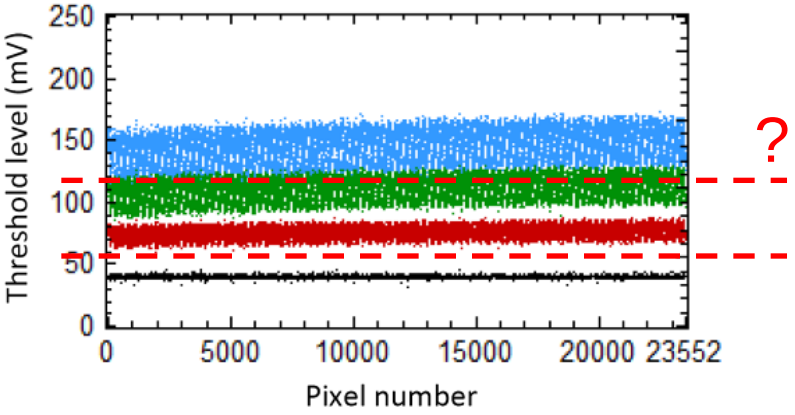


Example - gain spread

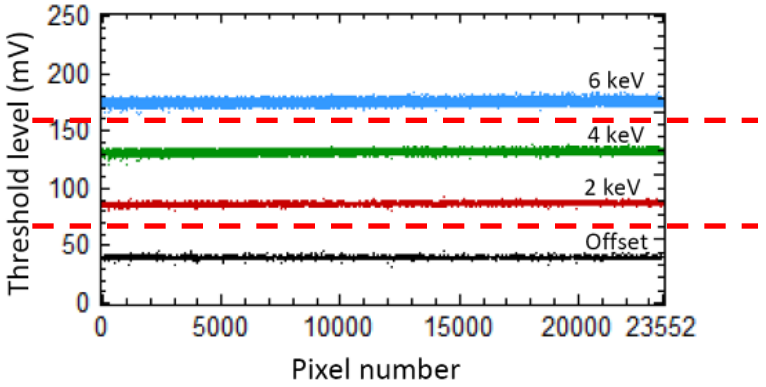


Solution:

use very precise offset trim



+ add gain trim



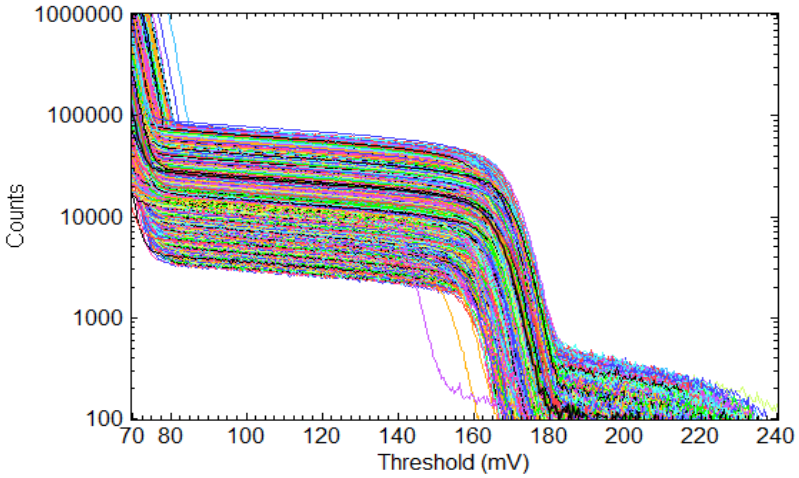
Offset and amplitudes of test pulses - prototype chip 128x184 pixels

Measurements with X-ray source (8.4 keV)

to calculate gain and noise

Integral spectra of 32761 pixels

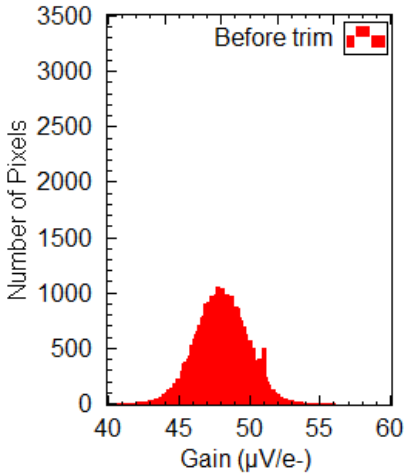
(only 7 pixels are missing due to errors in bump-bonding)

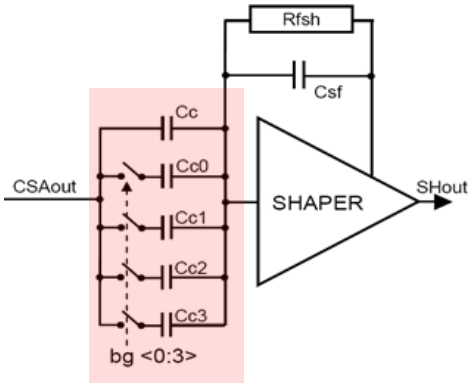


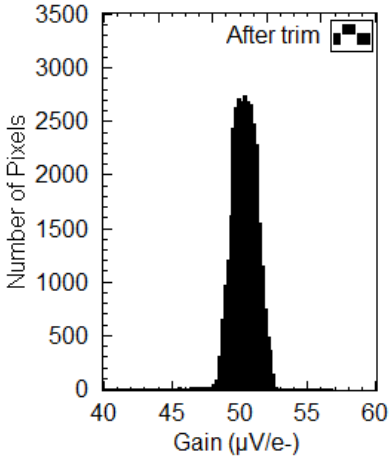
$$f(x) = \frac{a}{2}\left(1 - \mathrm{erf}\left(\frac{x-\mu}{\sqrt{2}\sigma}\right)\right)(bx + c)$$

a - average number of input pulses of given energy,
μ - threshold of the pixel for the given X-ray energy,
σ - related to the electronic noise and energy spectrum
(*bx*+*c*) - linear term to model the charge sharing.

Gain histograms

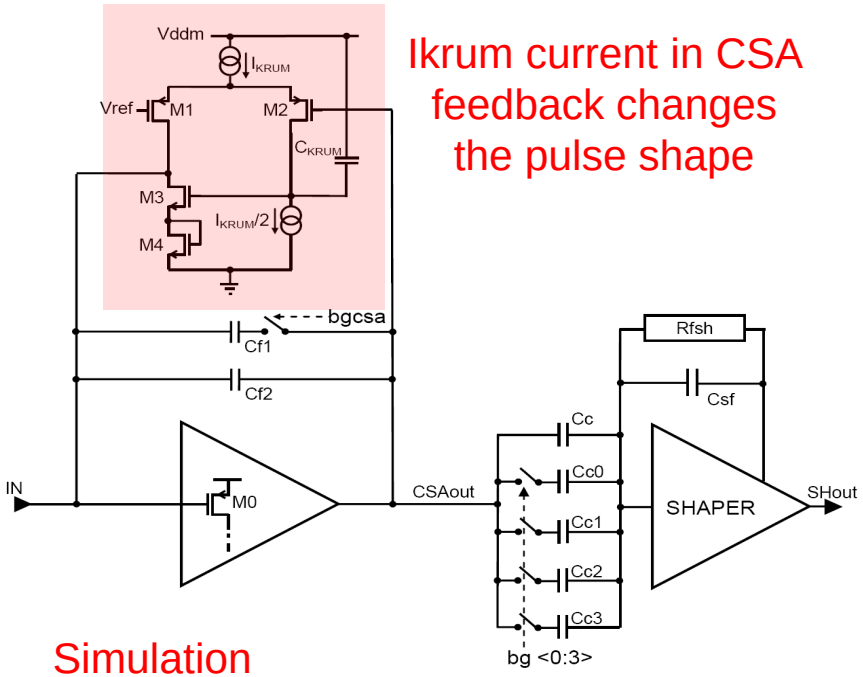






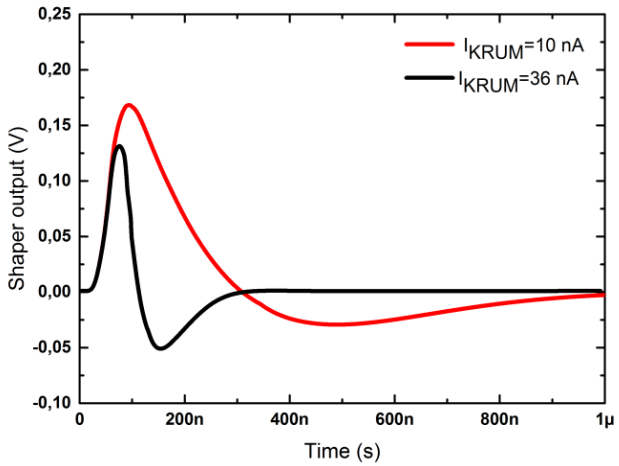
mean = 50.3 μV/e⁻
sd/mean = 1.9%

Equivalent Noise Charge vs. Ikrum in CSA feedback



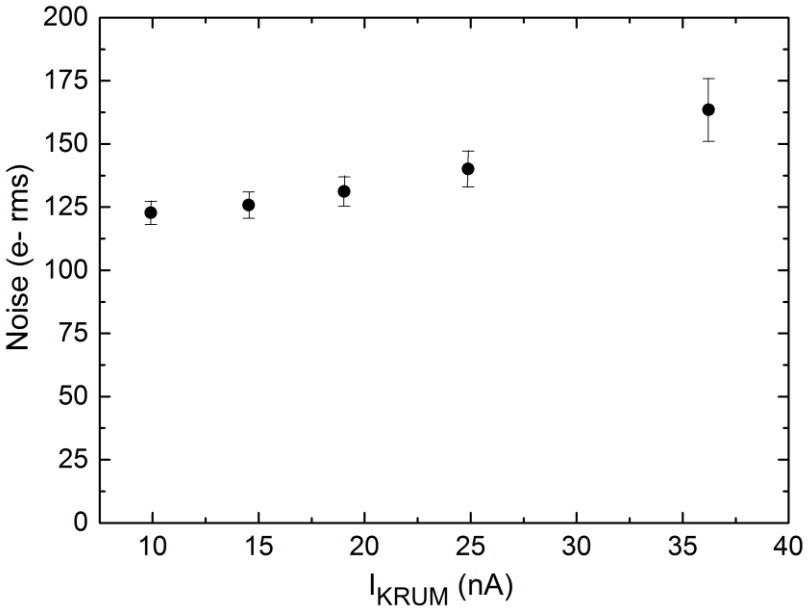
Ikrum current in CSA feedback changes the pulse shape

Simulation



Noise calculated using **measured integral spectra of X-ray source**

$$f(x) = \frac{a}{2}\left(1 - \mathrm{erf}\left(\frac{x-\mu}{\sqrt{2}\sigma}\right)\right)(bx + c)$$



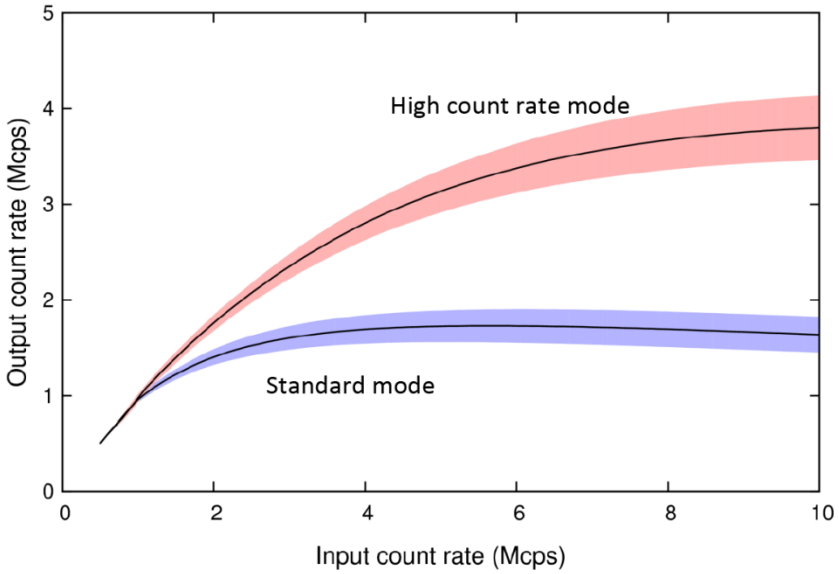
Ikrum = 10 nA, ENC=123 e⁻ rms
Ikrum = 36 nA, ENC=163 e⁻ rms

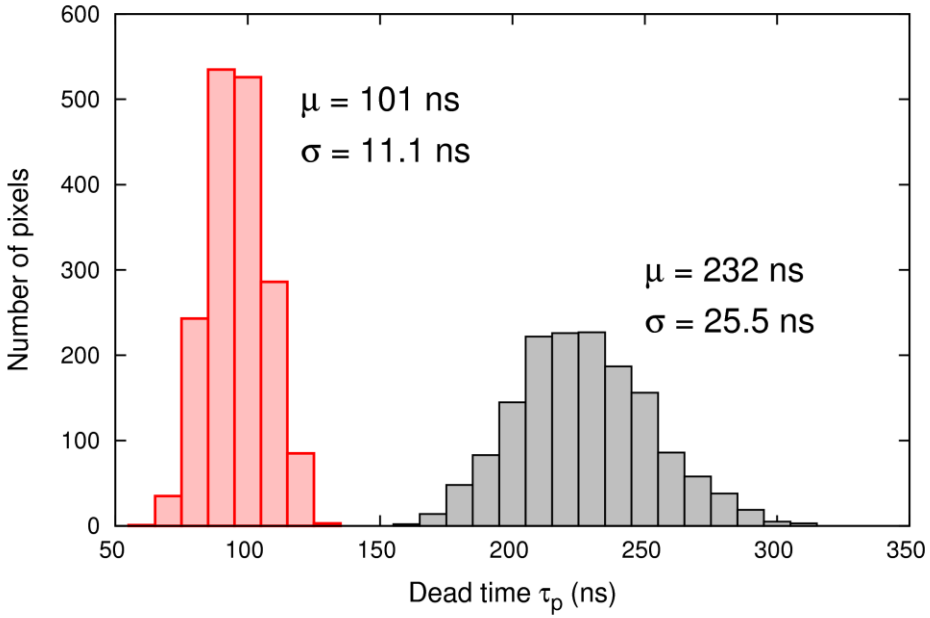
Count rate performance – part 1

1. X-ray tube with Cu anode (8 keV) operated at 45 kV and the current: from 20 mA up 190 mA
2. The results of the threshold scans for nominal setting in bias current of CSA feedback: *Ikrum* = 10 nA (SD mode) and *Ikrum* = 36 nA (HCR mode)
3. The illuminated detector area with the input pulse rate above 10 Mcps ⇒ 1200 pixels
4. Model of paralyzable photon counter

Threshold set at half of X-ray energy

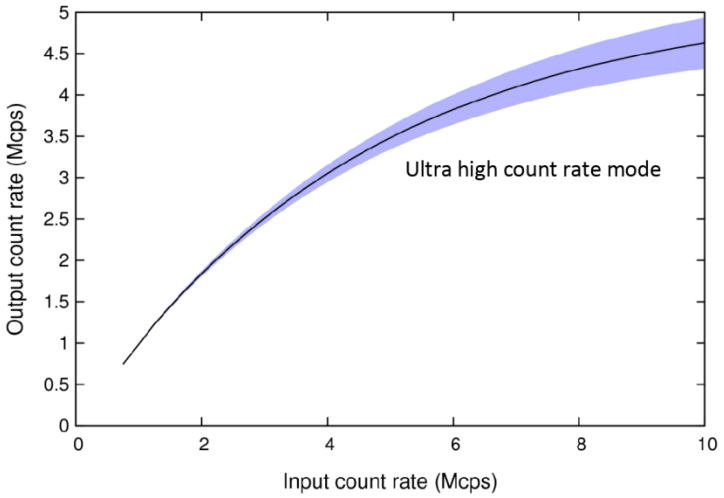
$$N_{OUT} = N_{IN} \exp(-N_{IN}\tau_P)$$

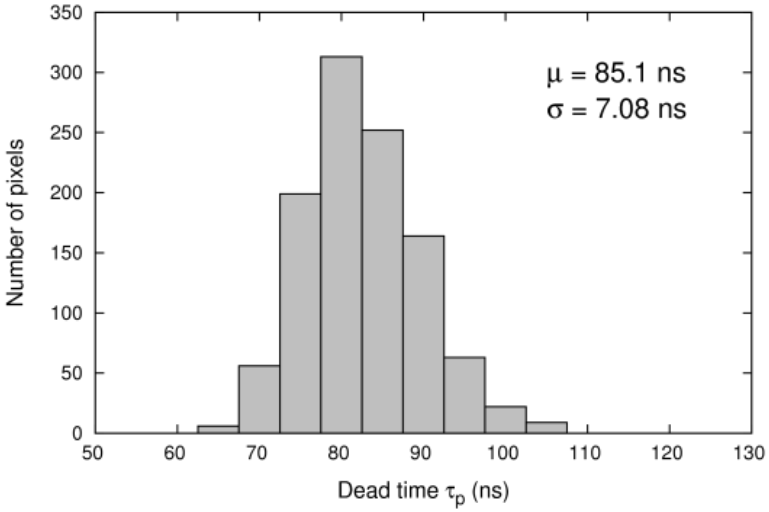




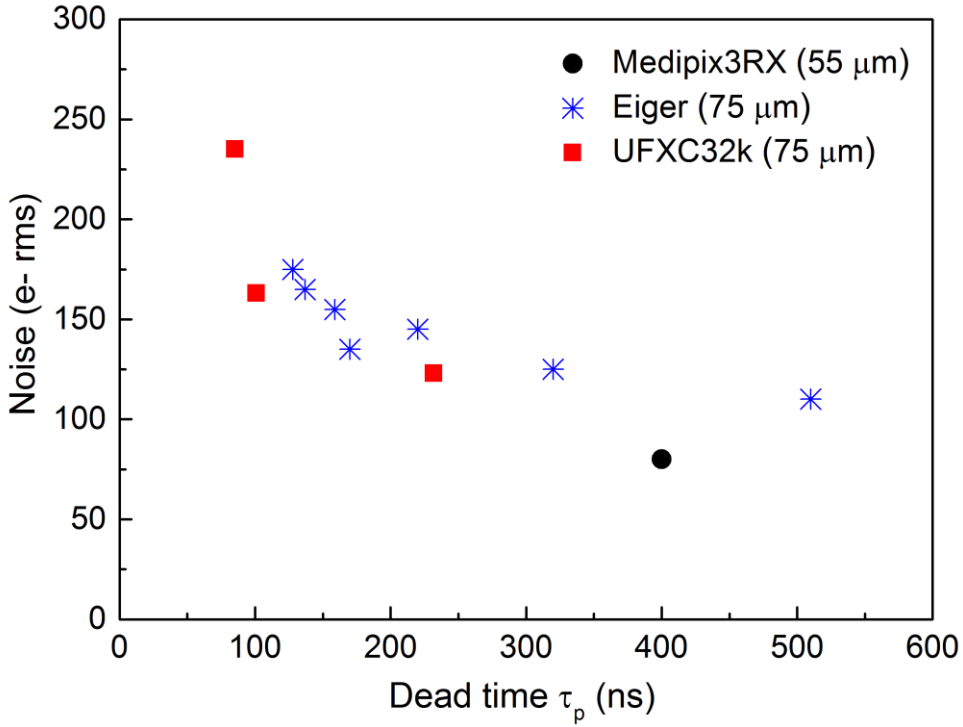
Count rate performance – part 2

Ultra high count rate mode





Comparision with others chips



Measured ENC as a function of the dead time for different chips – in all cases the chips were bump-bonded to silicon detectors. It should be noted that UFXC32k and Eiger chips have the same pixel pitch of 75 um and noise was measured using X-ray tube - this can lead to an overestimation of real noise [5]. The Medipix3RX has pixel pitch of 55 um and noise was measured using electrical test pulse [2, 19].

Count rate performance – comparision

$$N_{OUT} = N_{IN} \exp(-N_{IN}\tau_P)$$

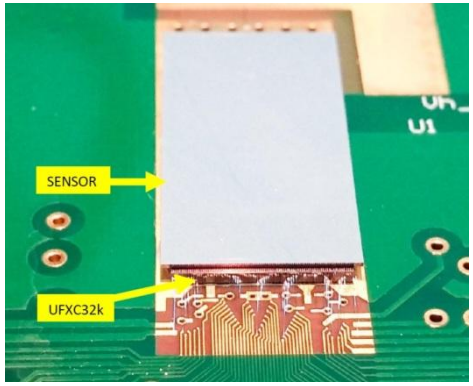
COMPARISON OF COUNTING RATE IN PIXEL CHIPS

Chip [ref]	Medipix 3RX [2, 19, 23]	PILATUS3 [20]	PXD18k [4]	Eiger [5]	UFXC32k this work
Pixel matrix	256×256	60×97	96×192	256×256	128×256
Pixel size [μm^2]	55×55	172×172	100×100	75×75	75×75
Min. dead time [ns]	400	67	172	128	85
10% dead time loss input rate: N_{OUT}/N_{IN} = 0.9 [photons mm^{-2} s^{-1}]	0.87×10^8	0.53×10^8	0.61×10^8	1.46×10^8	2.20×10^8
Max. conunt rate: N_{OUT}/N_{IN} = 1/e [photons mm^{-2} s^{-1}]	$8{,}26 \times 10^8$	$5{,}05 \times 10^8$	$5{,}81 \times 10^8$	13.9×10^8	20.9×10^8

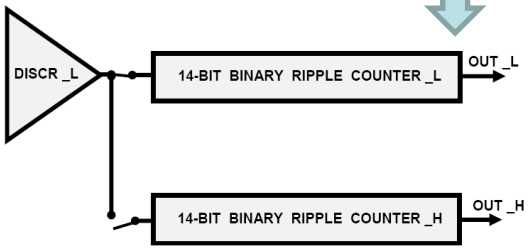
The shortest dead time of 67 ns, reported in literature, was measured for PILATUS3 IC with pixel size of 172×172 μm^2 . In our case for UFXC32k the dead time as small as 85 ns can be obtained, however the pixel area is 5.2 times smaller (only 75×75 μm^2) than for PILATUS3 IC, so the count rate per detector area is significantly higher.

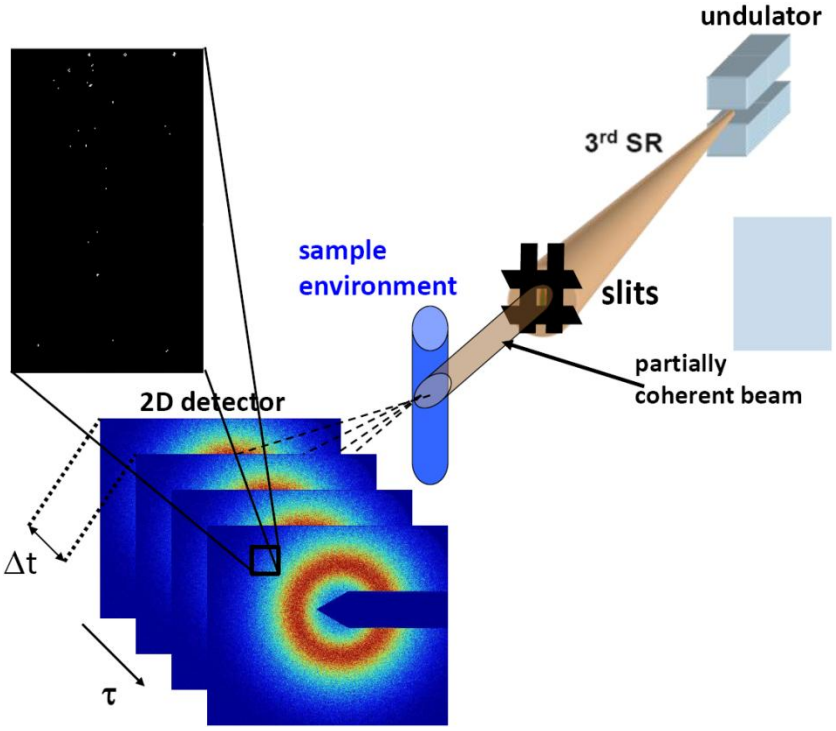
Tests for continuous mode of operation of UFXC32k
(X-ray Photon Correlation Spectroscopy at Advanced Photon Source in ANL)

Unique technique to probe the motion of nanoscale structures over a wide range of length (100 nm – 1 nm) and time scales (10^{-6} – 10^{3} seconds) in materials



continuous mode (zero dead time)

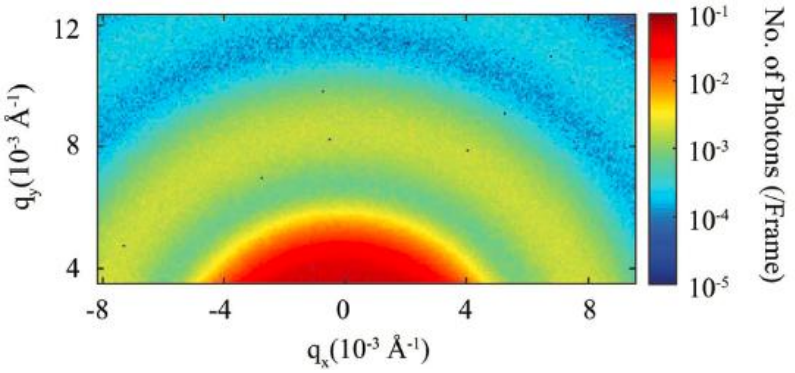




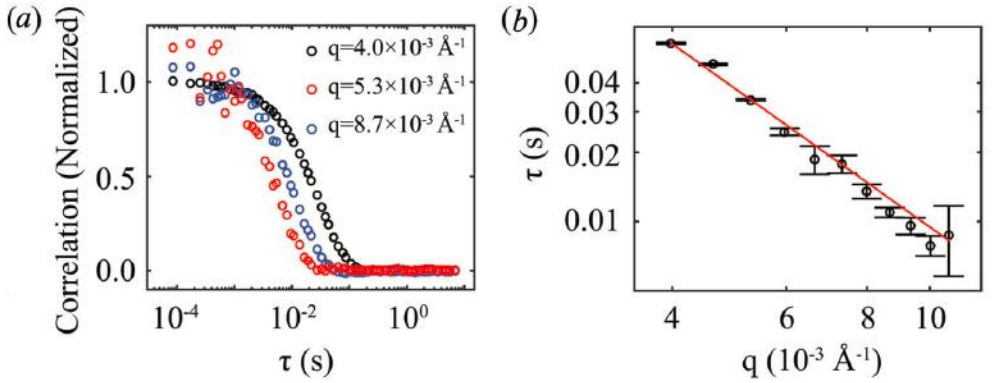
Phase 1 : DISCR_L ⇒ COUNTER_L (M-bits)
COUNTER_L (M-bits) ⇒ data readout
Phase 2: DISCR_H ⇒ COUNTER_H (M-bits),
COUNTER_L(M-bits) ⇒ data readout

First tests for UFXC32k usability for XPCS experiments at APS at ANL

UFXC32k was set to operate in 2-bit readout mode at 100 MHz allowing to receive up to 180 000 images with 11.8 kfps (15 sec.)



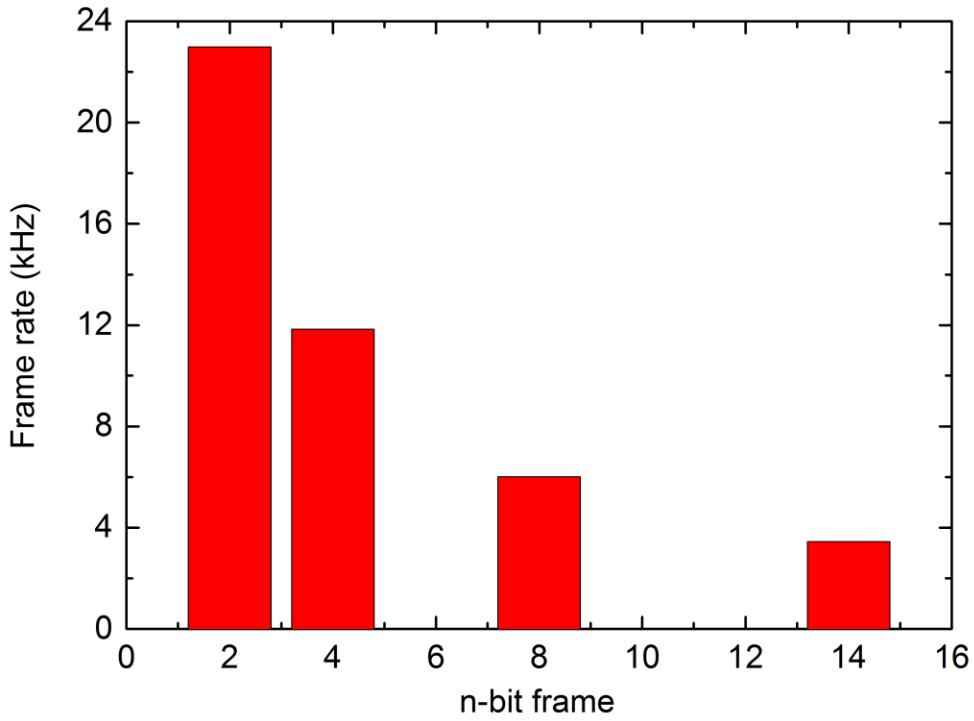
(*a*) Time-averaged scattering from the latex nanoparticle suspension. The scattering intensity is indicated by the logarithmic color bar.



(*a*) Dynamics of latex nanoparticles indicated by $g_2(\tau)$ at different q. (*b*) Decorrelation time $\tau(q)$ *versus* q. The red line shows the inverse-square decay of the correlation time.

Ref. [24] Q. Zhang, et al, "Submillisecond X-ray photon correlation spectroscopy from a pixel array detector with fast dual gating and no readout dead-time", Journal of Synchrotron Radiation vol. 23, p. 679–684, 2016.

Continuous mode of operation - max frame rate?

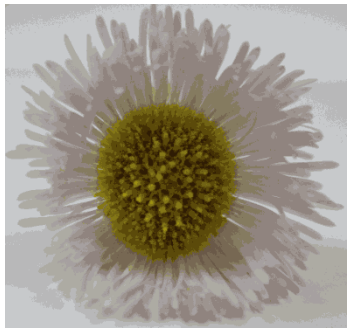


For reading out 2 bits/pixel with 200 MHz clock the frame rate is equal to 23 kHz. The performed tests have a significant limitation in the maximum clock frequency (Single Data Rate clock of 200 MHz) because of our test system based on NI PXI-6562 Digital Waveform Generator/Analyzer.

The next step will be rebuilding of the test system to allow operation of chip readout with Double Date Rate clock of 400 MHz according to UFXC32k design specification.

Example of X-ray image

Photos

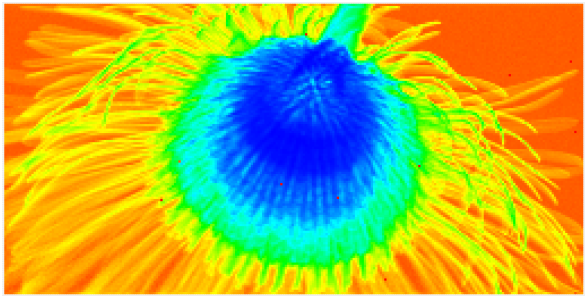


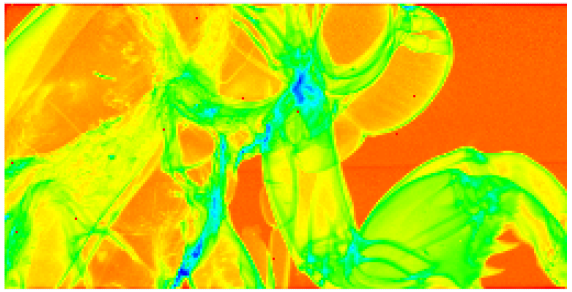
Flower

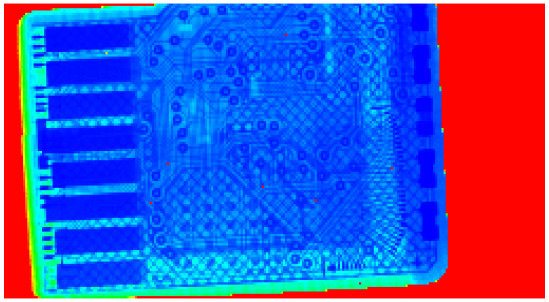
Insect

SD card

Radiograms







Summary

comparison of counting pixel chips in submicron technology

COMPARISON OF COUNTING PIXEL CHIPS IN SUBMICRON TECHNOLOGY

Chip [ref]	Medipix 3RX [2, 19, 23]	PIXIE III [6]	PILATUS3 [20]	XPAD3S [3]	PXD18k [4]	Eiger [5]	UFXC32k this work
Process	130 nm	160 nm	250 nm	250 nm	180 nm	250 nm	130 nm
Chip area [mm^2]	15.9 ×14.1	25 ×32	10.5 ×17.5	10.4 ×17.4	9.6 ×20	19.3 ×20	9.6 ×20.1
Pixel matrix	256×256	402×512	60×97	80×120	96×192	256×256	128×256
Pixel size [μm^2]	55×55	62×62	172×172	130×130	100×100	75×75	75×75
Power/pix. [µW]	9	–	15*	40	23	–	26
Offset spread [e^- rms rms]	37.5&	30	–	57	42	20–30	8.5
ENC [e^- rms]	80	50	–	130	168	110 / 135 / 175	123 / 163 / 235
Dead time [ns]	400&	–	67	–	172	510 / 170 / 128	232 / 101 / 85
10% dead time loss input rate # [photons mm^{-2} s^{-1}]	0.87×10^8	–	0.53×10^8	–	0.61×10^8	1.46×10^8	2.20×10^8
Double threshold	Yes	Yes	No	No	Yes	No	Yes
Counters per pixel	2 ×12 bit	2 ×15 bit	1 × 20 bit	1 × 12 bit	2 ×16 bit	1 ×12 bit	2 ×14 bit
TSV option	Yes	No	No	No	No	No	Yes
Frame rate max [kHz] (readout bits)	–	0.5	0.5	0.5	7.1 (4-bits)	~23 (4-bits)	23 (2-bit)

*static PWR consumption.

&min. reported value – for details see [2, 19].

calculated using min. dead time and assuming $N_{OUT}/N_{IN} = 0.9$ – see formula (1).

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