An asynchronous pixel front-end channel in 65 nm CMOS for the HL-LHC experiment upgrades

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Phase 2 upgrade of the experiments at the HL-LHC

Asynchronous front-end for pixel detectors
- design choices
- main features

Front-end characterization
- charge sensitivity
- equivalent noise charge
- behavior in the presence of large detector leakage currents

Ionizing radiation effects
- charge sensitivity and signal shape
- equivalent noise charge

Summary & outlook
Activity funded by INFN through the CHIPIX65 project, carried out also in the framework of the RD53 collaboration

**CHIPIX65**
- Italian collaboration funded by INFN (~700 kEuro/3 years, started 2014)
- INFN units from Bari, Milano, Padova, Pavia, Perugia, Pisa & Torino
- develop a chip for pixel detectors using a 65 nm CMOS process
- organized in 5 WP: radiation hardness, digital electronics, analog electronics, chip integration and management
- develop analog front-end circuits, IP blocks, explore new digital readout architectures, fabricate & test a 64x64 readout channel array

**RD53**
- joint CMS-ATLAS effort to develop pixel front-end for the phase 2 upgrades
- 22 institutions from Europe and US, >100 members
- 65 nm CMOS is the common technology platform
- about 50% of the people are microelectronic designers
- synergies with other collaborations (e.g., CLIC)
- study radiation effects, develop a simulation & verification environment, design & share rad-hard libraries, design small size prototypes & a full size pixel array (>1 cm²) from a common engineering run and test it on a beam
Very challenging requirements for the innermost layers of the pixel detectors in ATLAS and CMS

- very high particle rate: ~500 MHz/cm² \(\Rightarrow\) hit rates of 2 GHz/cm² or larger
- smaller pixels: 25 x 100 or 50 x 50 um² \(\Rightarrow\) increased resolution, improved track separation
- increased trigger rate: 1 MHz
- low mass, low power, <0.5W/cm²
- harsh radiation environment: 10 MGy(SiO₂) TID, 10^{16} eq. n/cm² fluence
- low threshold: 600-1000 e⁻ \(\Rightarrow\) severe requirements on noise and dispersion
Front-end channel scheme

![Diagram of a front-end channel scheme](image)

- **Single ampli stage for minimum power dissipation**
- **Krummenacher feedback to comply with the expected large increase in the detector leakage current (up to ~10 nA)**
- **30000 electron maximum input charge expected, ~450 mV preampli output dynamic range**
- **Selectable gain, recovery current and detector emulating capacitance**
- **40 MHz clock, 5 bit dual edge counter, 400 ns maximum ToT**

**Parameters:**
- $I_K$: 25, 50 nA
- $C_F$: 10, 20 fF
- $C_D$: 0, 50, 100, 150 fF
- $C_{\text{inj}}$: 30 fF

**Equations:**
- $i_{\text{inj}} = Q \delta(t)$
- $I_K/2$ recovery curr. sel
- $V_{\text{out}}$
- $V_{\text{REF}}$
- $C_K$
- $C_D$
- $C_F$
- $C_{\text{inj}}$

**Diagram notes:**
- Injection enable
- Gain sel
- Discriminator
- 5 bit counter
- ToT clock
Gain stage based on a folded cascode configuration (~3 μA absorbed current)

Area is slightly less than 25 μm x 50 μm, even smaller in the new version of the channel

L. Ratti, “An asynchronous pixel front-end channel in 65 nm CMOS for the HL-LHC experiment upgrades”, FEE 2016, Krakow, Poland
CHIPIX-VFE-1 chip & test setup

2 mm x 2 mm chip including two different versions of a charge preamplifier with Krummenacher-style feedback network
Preamplifier response in different configurations

Preamplifier output, feedback MOS capacitor, high and low gain and restoring current - high $G$, low $I_K$ for operation @5 bit/40 MHz (dual edge counter)

$C_D^*$ also accounts for the injection cap ($C_{inj} = 30$ fF)

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Good ToT linearity for $Q \geq 2000 \text{ e}^-$ (and well in excess of 30000 e^-)

In-time overdrive smaller than 600 e^- for a threshold of 600 e^- @$C_D^* = 80 \text{ fF}$
MIM capacitor
- charge sensitivity $\sim 13.7 \text{ mV/ke}^-$, ($\sim 7$ % smaller than design value)
- $\leq 1$% dispersion,
- $\leq 3$% non-linearity

PMOS capacitor
- charge sensitivity $\sim 12.4 \text{ mV/ke}^-$, ($\sim 17$ % smaller than design value)
- $\sim 1$% dispersion,
- $\leq 4$% non-linearity
Equivalent noise charge

- chip 1
- PMOS fb cap

- high $i_k$
- low $i_k$

Best behavior in the nominal configuration (high gain, low recovery current) - smaller parallel contribution, predominant contribution from the input device

Smaller noise measured at the discri output $\leftrightarrow$ bandwidth limitation

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ENC as a function of the input device current

![Graph showing ENC as a function of $C_D^*$ for different input device currents.]

- No advantage in increasing the input device current, small ENC increase for a 500 nA current decrease.
Measurements in the presence of a leakage current

If a ramp signal is applied to the injection capacitance, a quiescent current will be flowing through the input terminal of the preamplifier (after an initial transient)

\[ I_{\text{leak}} = -C_{\text{inj}} \frac{dV}{dt} \]

ramp starts - expect a transient at the preamplifier output
dV
dt

time needed for recovery after large pulse injection

very large pulse injected at the input - expect a long transient at the preamplifier output

Leakage current is limited to 15 nA by the maximum excursion of the ramp - limits are set by ESD protections

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Signal shape and charge sensitivity

No significant change in the shape, independent of the kind of feedback cap, input cap, channel configuration

<4% increase in charge sensitivity for leakage currents in the 10 nA range

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Irradiation procedure

Two separate irradiation campaign (one other under way)

10 MeV protons at the SIRAD facility in Legnaro - 15 MV Tandem accelerator

Irradiation steps: 300, 650, 800 Mrad

Samples irradiated as bare dice (no bias applied)

3 MeV protons at the CN facility in Legnaro - 7 MV Van de Graaff accelerator

Irradiation steps: 100, 200, 500 Mrad

Samples mounted on a PCB and biased during irradiation as in the real application

Extremely high dose rates (~500 Mrad/h at SIRAD, ~2 Grad/h at CN) ➔ possible low dose rate sensitivity effects not accounted for

Samples irradiated at room temperature (possible increase in temperature during irradiation)

After irradiation, samples kept at T≈0 °C while not being glued to the daughter board/wire bonded/characterized
Charge sensitivity: PMOS feedback cap

- PMOS fb cap
- high gain
- low recovery current
- $C_D = 130$ fF

**Slight increase of the charge sensitivity with the dose**

+3.8%

+5%

+7.7%
Charge sensitivity: MIM feedback cap

No such effect observed in the case of the CSA with MIM feedback cap

Effect independent of bias condition (DUT biased or unbiased) during irradiation
CSA response: PMOS feedback cap

- Negligible variation in peaking time
- Change in the peak amplitude $\leftrightarrow$ decrease in $C_F$
- Change in the time to return to baseline $\leftrightarrow$ decrease in $C_F$ and increase in $I_K$
- Change in $C_F$ likely due to the same mechanism underlying RISCE effect (F. Faccio et al., IEEE TNS, vol. 62, no. 6, pp. 2933-2940, Dec. 2015)

**Graph:**
- Peak proportional to $1/C_F$
- Slope proportional to $I_K/C_F$
- PMOS fb cap proportional to source/drain to gate overlap
- PMOS cap proportional to source/drain to gate overlap

**Equation:**
$$p_{p} + p_{LDD} + \text{spacers}$$

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CSA response: MIM feedback cap

- MIM fb cap
- high gain
- low recovery current
- $C_D = 130 \, \text{fF}$

**slope proportional to $I_K/C_F$**

- No variation in the peaking time nor in the peak amplitude
- Change in the time to return to baseline $\rightarrow$ possible increase in $I_K$
- $I_K$ almost back to the starting value at 500 Mrad
- Change in $I_K$ likely due to a radiation induced mismatch in the current mirrors setting the bias current in the Krummenacher stage
Equivalent noise charge

Increase in the slope compatible with an increase in the series noise contribution (likely in flicker noise, see Valerio Re’s talk)
ENC slope vs dose

- high gain
- low recovery current

- biased PMOS cap
- biased MIM cap
- non-irradiated

- unbiased MIM cap
- unbiased PMOS cap

Worse radiation tolerance in biased DUTs

Larger fractional yield in the presence of a field across gate oxide and STI → larger radiation induced trap density at the gate oxide/channel and STI/channel interface
Channel for the CHIPX65 demonstrator

- About 33 um x 33 um in area (analog section only, overall cell area is 50 um x 50 um)
- In deep N-well (except for the output stage of the discriminator)
- Programmable gain (1 bit, local) bias current in the Krummenacher stage (10 bit, global) and threshold (4 bit, local, and 10 bit, global)
- Post-layout simulation performance as in the prototype
Summary & outlook

- A front-end channel for phase 2 upgrade of CMS has been designed and tested
  - Noise performance and response timing fully compliant with the specs
  - No significant effects of leakage current on signal shape and charge sensitivity (up to 15 nA, limited by measurement technique)
  - Present design sitting in its optimum point as far as noise is concerned

- TID characterization has been performed with doses up to 800 Mrad
  - Minor changes with dose observed in the charge sensitivity and signal shape
    - slight increase for PMOS fb cap, negligible change for MIM fb cap
  - Significant variations detected in the equivalent noise charge slope, still ENC<120 e- @C_d*=50 fF

- Next steps:
  - radiation tolerance tests on the discriminator (irradiation campaign with X-ray source in Padua)
  - final contribution to the CHIPX65 demonstrator and RD53A chip design and subsequent chip characterization