The Pinned Photodiode

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- IS sales amount has grown mainly by camera phone in this 10 years. But, it became diminished in Q4, 2015.
- IS spreads into various applications, “Others” includes scientific, industrial, …

(Source: TSR)
- Shrinkage speed becomes slower recently.
- In 2015, 1 um pixel began to be mass produced.

Pixel Shrinkage Trend

50% shrinkage in 3.5 years

Mass Production Year

Minimum Pixel Area (um²)

Microlens

Inner Microlens

Shifted Microlens

Pinned PD (PPD)

Lightpipe

BSI

Stack

DTI

CCD

CMOS
1. Introduction
2. Pinned Photodiode (PPD) Structure and Effects
3. Image Lag
4. Transfer Noise
5-1. Dark Current Reduction
5-2. New Diffusion Current Model Including Non-Uniformity
5-3. Recent Approaches for Dark Current Reduction
6. Vertical Overflow Drain (VOD) Shutter with PPD
7. Visible Light Photon Counting Image Sensors
8. Conclusion

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Contents

1. Introduction
2. Pinned Photodiode (PPD) Structure and Effects
3. Image Lag
4. Transfer Noise
5-1. Dark Current Reduction
5-2. New Diffusion Current Model Including Non-Uniformity
5-3. Recent Approaches for Dark Current Reduction
6. Vertical Overflow Drain (VOD) Shutter with PPD
7. Visible Light Photon Counting Image Sensors
8. Conclusion
1. The P\(^+\) pinning layer prevents the interface from being depleted, and stabilizes the PD electrically.
   - Low dark current
   - Large saturation
   - High sensitivity
   - Electronic shutter

2. Complete charge transfer
   - No image lag
   - No transfer noise
Contents

1. Introduction
2. Pinned Photodiode (PPD) Structure and Effects
3. Image Lag
4. Transfer Noise
5-1. Dark Current Reduction
5-2. New Diffusion Current Model Including Non-Uniformity
5-3. Recent Approaches for Dark Current Reduction
6. Vertical Overflow Drain (VOD) Shutter with PPD
7. Visible Light Photon Counting Image Sensors
8. Conclusion

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The driving force is $\psi_{TG} - V_{PD}$, or $V_{GS}$. 
($\psi_{TG}$ : TG channel potential)

Step 1. At first, TG operates in the saturation region.
Step 2. A few ns later, it enters the subthreshold region.

The subthreshold region causes image lag and transfer noise.
Time evolution of $V_{PD}$ is governed by the equation of continuity;

$$C_{PD} \frac{dV_{PD}}{dt} = I = I_0 e^{-\frac{qV_{PD}}{mkT}}$$

$V_{PD}(t)$ is derived as

$$V_{PD}(t) = \frac{mkT}{q} \ln \left\{ e^{\frac{qV_{PD}(0)}{mkT} + \frac{qI_0}{mkTC_{PD}}} \right\}$$

The $n^{th}$ frame lag, $n_{lag}(n)$, is obtained with

$$n_{lag}(n) = \frac{mkTC_{PD}}{q} \ln \frac{n+1-ne^{-\frac{q^2n_{sig}}{mkTC_{PD}}}}{n-(n-1)e^{-\frac{q^2n_{sig}}{mkTC_{PD}}}}$$

$$\sim \frac{mkTC_{PD}}{q} \frac{1}{n} \quad \text{when } n_{sig} \gg 1 \text{ and } n \gg 1$$
Image Lag in Conventional PN PDs (3)

The subthreshold model matches the measurements!

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(N. Teranishi et al., IEDM, 1982)
Causes of Image Lag in PPDs (1)

(A) Small electric field

(B) Barrier at the PD edge

(C) Pocket at the TG edge

(D) Pump back when the signal is large

(E) Traps at the TG interface

On the next slide.
(E) Traps at the TG interface

If the electron transfer path touches the interface, some electrons are captured by traps.
- Some of them are detrapped in the following frames, causing lag.
- Some of them are annihilated, causing non-linearity.

- The signal electron annihilation exhibits this kind of non-linearity.
- A buried transfer path is needed to suppress these phenomena.
Contents

1. Introduction
2. Pinned Photodiode (PPD) Structure and Effects
3. Image Lag
4. Transfer Noise
5-1. Dark Current Reduction
5-2. New Diffusion Current Model Including Non-Uniformity
5-3. Recent Approaches for Dark Current Reduction
6. Vertical Overflow Drain (VOD) Shutter with PPD
7. Visible Light Photon Counting Image Sensors
8. Conclusion

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Transfer Noise in Conventional PN PDs (1)

\[ V_{PD}(t) = V_{PDa}(t) + V_n(t) \]  \hspace{1cm} (1)

\[ \uparrow \quad \text{Average} \quad \uparrow \quad \text{Noise} \]

The equation of continuity is

\[ C_{PD} \frac{dV_{PD}}{dt} = I + I_n = I_0 e^{-\frac{qV_{PD}}{mkT}} + I_n \]  \hspace{1cm} (2)

\[ I_n: \text{Noise}, \langle I_n(t_1)I_n(t_2) \rangle = qI(t_1)\delta(t_1 - t_2) \]  \hspace{1cm} (3)

The procedure to calculate the transfer noise is

Step 1: Obtain \( V_{PDa}(t) \).
Step 2: Obtain \( V_n(t) \).
Step 3: Obtain the variance, \( \langle V_n^2 \rangle \).
Transfer noise, \( <V_n^2> \), is obtained as

\[
<V_n^2> = \frac{qI_0 t}{2C_{PD}} \frac{mkT}{mk TC_{PD}} e^{-\frac{qV_{PDa}(0)}{mkT}} \left( 2 + \frac{qI_0 t}{mk TC_{PD}} e^{-\frac{qV_{PDa}(0)}{mkT}} \right)^2 
\]

\[
+ \frac{1}{1 + \frac{qI_0 t}{mk TC_{PD}} e^{-\frac{qV_{PDa}(0)}{mkT}}} \langle V_n(0)^2 \rangle
\]

Not an exponential decay, and the convergence is slow.
When $t \to \infty$, (4) becomes

$$\langle V_n^2 \rangle \rightarrow \frac{mkT}{2C_{PD}}$$

(5)

Caution:
- This convergence is very slow, and the initial noise decay is also slow.
- If the TG ON period is 1 µs, we should not use this limit. We should use (4) and calculate the value at $t = 1$ µs, considering the initial condition.
Contents

1. Introduction
2. Pinned Photodiode (PPD) Structure and Effects
3. Image Lag
4. Transfer Noise
5-1. Dark Current Reduction
5-2. New Diffusion Current Model Including Non-Uniformity
5-3. Recent Approaches for Dark Current Reduction
6. Vertical Overflow Drain (VOD) Shutter with PPD
7. Visible Light Photon Counting Image Sensors
8. Conclusion
Dark Current Reduction Mechanism by SRH (1)

Schockley-Read-Hall Process

\[ U = \sigma_{th} N_t \frac{pn - n_i^2}{n + p + 2n_i \cosh \left( \frac{E_t - E_i}{kT} \right)} \]  \hspace{1cm} (1)

\( U \): Recombination Rate

(Sze: “Semiconductor Devices,” Chap. 1 Eq.(59))

1. If depleted, \( n, p \ll n_i \)

\[ U = \sigma_{th} N_t \frac{-n_i^2}{2n_i \cosh \left( \frac{E_t - E_i}{kT} \right)} \]

When \( E_t = E_i \) where \( U \) is maximum, then,

\[ U \approx -\sigma_{th} N_t \frac{n_i}{2} \]  \hspace{1cm} (2)

Large dark current!

2. If not depleted, \( p \gg n_i \gg n \),

\[ |U| \approx \left| \sigma_{th} N_t \frac{pn - n_i^2}{pn} \right| \leq \sigma_{th} N_t \frac{n_i^2}{p} \]  \hspace{1cm} (3)

Small dark current!

PPDs configure this non-depleted situation!
(1) Estimate the interface dark current reduction ratio, assuming that:
- Hole density \( p \) at the P\(^+\) pinning layer: \( 10^{17} \) cm\(^{-3}\)
- Intrinsic carrier density, \( n_i \): \( 1.45 \times 10^{10} \) cm\(^{-3}\)

\[
\frac{|U(\text{Not depleted})|}{|U(\text{Depleted})|} \leq \frac{\sigma v_{th} N_t n_i / 2}{\sigma v_{th} N_t n_i^2 / p} = \frac{p}{2n_i} \sim 10^{-7}
\]

(2) Dark current comparison by image sensors.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel size</td>
<td>23 x13.5</td>
<td>1.12 x 1.12</td>
<td>( \mu m )</td>
</tr>
<tr>
<td>Dark current</td>
<td>1,300</td>
<td>5.6</td>
<td>( e^-/s/\mu m^2 \text{ at } 60^\circ C )</td>
</tr>
</tbody>
</table>
If the dark current is reduced, the dark current FPN and dark current shot noise will also be reduced.

Example of Dark Current Reduction (1)

Conventional PD

PPD

The dark current FPN is suppressed, therefore, picture quality is much improved.
1. Introduction
2. Pinned Photodiode (PPD) Structure and Effects
3. Image Lag
4. Transfer Noise
5. Dark Current Reduction
6. New Diffusion Current Model Including Non-Uniformity
7. Recent Approaches for Dark Current Reduction
8. Vertical Overflow Drain (VOD) Shutter with PPD
10. Conclusion
A Question About the Dark Current Reduction Mechanism

Even if the P+ pinning layer neutralizes the interface states, the N-type PD is still depleted nearby the P+ pinning layer. The assumption of “spatial uniformity,” which is implicitly used in SRH, is not realistic!

To understand the effects and limitations of PPDs, a new, correct model is needed.
Modified Diffusion Current Model:

- 1-Dim (Along $-x_{GR}$)
- Put the GR centers at $x = -x_{GR}$ in the neutralized region.
- Assume still “stationarity,” but no more “spatial uniformity.”
- No electric field in the neutralized region. Low injection.
- Use the same notation of Sze’s “Semiconductor Devices.”
Introduce the GR centers’ effect into the diffusion equation:

\[ D_n \frac{\partial^2 n_p}{\partial x^2} - \frac{n_p - n_{p0}}{\tau_n} - GD_n (n_p - n_{p0}) \delta(x + x_{GR}) = 0 \]  

- At \( x = -x_{GR} \), the GR centers force \( n_p \) toward \( n_{p0} \), the equilibrium.

- \( G \): Intensity of the GR Centers. Unit is 1/cm.

  \( GL_n \) is a dimensionless parameter for the GR centers’ intensity.

  \( L_n \equiv \sqrt{D_n \tau_n} \) : Diffusion Length

**Boundary Conditions:**

- Same as in the diffusion current model without GR centers

  \[ n_p = n_{p0} \] at \( x = -\infty \)  

  \[ n_p = n_{p0} e^{qV/kT} \] at \( x = -x_p \)
Derived Solution

Diffusion Current (Dark Current) with GR Centers

\[ J_n^{(GR)}(-x_p) = J_n^{(0)}(-x_p) \times EDCF \]  \hspace{1cm} (6)

where

\[ J_n^{(0)}(-x_p) \equiv \frac{qD_n n_p^0}{L_n} \left( e^{qV/kT} - 1 \right) \]  \hspace{1cm} (7)

Diffusion Current (Dark Current) without GR Centers

\[ EDCF \equiv \frac{GL_n + 1}{GL_n + 1 - GL_n e^{-(x_{GR}-x_p)/L_n}} \]  \hspace{1cm} (8)

\[ EDCF: \text{ Extra Dark Current Factor} \]

\[ L_n \equiv \sqrt{D_n \tau_n} : \text{Diffusion Length} \]

\[ GL_n : \text{Dimensionless Parameter for the GR Centers’ Strength} \]
Characteristics of the New Diffusion Current Model

When \((x_{GR} - x_p)/L_n = 0\), GR centers become not neutral; \(EDCF = GL_n + 1\)

When \(GL_n \to \infty\), then, \(EDCF \to \frac{1}{1 - e^{-(x_{GR} - x_p)/L_n}}\)
No divergence; instead, saturation.

Temperature dependence: \(J_n^{(GR)} \propto J_n^{(0)} \propto e^{E_g/kT}\)

When \(GL_n \to 0\), \(J_n^{(GR)} \to J_n^{(0)}\)
Reasonable.

When \((x_{GR} - x_p)/L_n \to \infty\), \(EDCF \to 1\).
The GR centers’ effect becomes negligible.
Characteristics of New Diffusion Current Model (2)

When \((x_{GR} - x_p)/L_n \rightarrow 0\), \(EDCF\) increases, because the GR centers’ position approaches the depletion region.

When \(GL_n \rightarrow 0\), \(J_n^{(GR)} \rightarrow J_n^{(0)}\)

Reasonable.

When \((x_{GR} - x_p)/L_n \rightarrow \infty\), \(EDCF \rightarrow 1\).

The GR centers’ effect becomes negligible.
Is the P⁺ Pinning Layer Thickness Sufficient?

- How large is the diffusion length, $L_n$, in the P⁺ pinning layer?
- The surface dead zone depth, $L_1$, might be a good alternative for $L_n$.
- $L_1$ is derived from the spectral response, to be ~0.08 μm.
- P⁺ pinning layer thickness $\approx$ 0.05 – 0.5 μm

The GR centers at the silicon surface possibly contribute to the dark current! We should reduce the GR centers.

(SONY ICX658ALA data sheet
Pixel size: 6.35 x 7.4 um)

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Contents

1. Introduction
2. Pinned Photodiode (PPD) Structure and Effects
3. Image Lag
4. Transfer Noise
5-1. Dark Current Reduction
5-2. New Diffusion Current Model Including Non-Uniformity
5-3. Recent Approaches for Dark Current Reduction
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Macroscopically Flattening

Itonaga et al. (Sony), IEEE IEDM, 2011

No isolation grooves/ridges and no substrate etching as in STI

Less process damage, less stress and no STI side surface.

Structure of “FLAT,” comparing with STI
Atomically Flattening

Kuroda et al. (Tohoku Univ.); “Highly Ultraviolet Light Sensitive and High Reliable Photodiode with Atomically Flat Si Surface”

- Low Dark Current, High QE for UV at PD.
- Low 1/f noise at MOS Tr.

- Atomically flat surfaces reduce GR centers/traps.

Typical (100) after RCA Cleaning.

AFM Images

Atomically Flat (100). Atomic step is 0.135nm.

N+PN PD
1. Introduction
2. Pinned Photodiode (PPD) Structure and Effects
3. Image Lag
4. Transfer Noise
5-1. Dark Current Reduction
5-2. New Diffusion Current Model Including Non-Uniformity
5-3. Recent Approaches for Dark Current Reduction
6. Vertical Overflow Drain (VOD) Shutter with PPD
7. Conclusion
Vertical Overflow Drain (VOD) Shutter

For Anti-blooming and electronic shutter
- The VOD is used in CCD image sensors
- TG is used as LOD (lateral overflow drain) in CMOS image sensors.

Blooming

Electronic Shutter
(Object is rotating at 720 rpm.)

1/60 s  1/125 s  1/250 s
1/500 s  1/1000 s  1/2000 s
Definitions

- **High speed shutter**: Short exposure time / sharp shutter
- **High speed camera**: High frame rate

Motivations of high speed shutter

- High speed motion capture, ToF, fluorescence lifetime imaging.
- Replace the streak tube and gated image intensifier.

Shutter speed is limited by:

1. Photo-generated carrier collection time into the PD storage region.
2. Driving pulse delivery time, \( C \times R \).
3. Carrier transferring time from the PD storage to analogue memory in the pixel.

- The VOD shutter mechanism with PPD has a merit on item (2).
High Speed Shutter (2) --- Load Capacitance ---

**VOD shutter**
- **Substrate capacitance**
  \[ C_{Sub} = \frac{K_{Si} \varepsilon_0 S}{d} \]
  where,
  - \( K_{Si} \): Si dielectric constant
  - \( \varepsilon_0 \): Permittivity in vacuum
  - \( S \): Area,
  - \( d \): distance (depletion thickness)

For example, 1/3 inch
  \( S = 28 \text{ mm}^2 \)
  \( d = 7.5 \mu m \)

\[ C_{sub} = 400 \text{ pF} \]

**LOD shutter**
- **Gate capacitance, \( C_{gate} \)**
  + parasitic capacitance of wires, \( C_{wire} \)
  \[ C_{Gate} = N_{pixel} \frac{K_{SiO_2} \varepsilon_0 WL}{t} \]
  where,
  - \( N_{pixel} \): Pixel number
  - \( K_{SiO_2} \): SiO\(_2\) dielectric constant
  - \( W \): Channel width,
  - \( L \): Channel length,
  - \( t \): Gate SiO\(_2\) thickness

For example, \( N_{pixel} = 1.3 \text{ M} \),
  \( W = L = 0.4 \mu m, t = 6 \text{ nm} \)

\[ C_{Gate} = 1,200 \text{ pF} \]
\[ C_{Wire} = ? \]

The load capacitance of the VOD shutter is smaller than that of the LOD shutter.
High Speed Shutter (3) --- Parasitic Resistance

Two methods for driving pulse delivery:

(a) From the periphery

(b) From the backside

- A small parasitic resistance and small variations of the parasitic resistance are achieved with (b) backside feeding.
- A skew smaller than the measurement accuracy limit (0.2 ns).

(E. Tadmor et al., 2014 IEEE Sensors)
1. Introduction
2. Pinned Photodiode (PPD) Structure and Effects
3. Image Lag
4. Transfer Noise
5-1. Dark Current Reduction
5-2. New Diffusion Current Model Including Non-Uniformity
5-3. Recent Approaches for Dark Current Reduction
6. Vertical Overflow Drain (VOD) Shutter with PPD
7. Visible Light Photon Counting Image Sensors
8. Conclusion
Visible Light Photon Counting Image Sensor

SPAD
(Single photon avalanche diode)

4-Tr CMOS + High conversion gain + CMS (Correlated multiple sampling)

- QVGA (320x240 pixel) SPAD, 20 fps, at room temperature, at night
- High avalanche gain makes following circuit noise negligible.
- Large dark count. Small fill factor

(MW. Seo, S. Kawahito et al., IEEE EDL 2015)
- In 2015, several organization reported low noise < 0.3 e- rms.

ref. DEPFET (Max Plank) uses CMS.
Contents

1. Introduction
2. Pinned Photodiode (PPD) Structure and Effects
3. Image Lag
4. Transfer Noise
5-1. Dark Current Reduction
5-2. New Diffusion Current Model Including Non-Uniformity
5-3. Recent Approaches for Dark Current Reduction
6. Vertical Overflow Drain (VOD) Shutter with PPD
7. Conclusion
1. The PPD is a primary technology for CCD and CMOS image sensors. It exhibits low noise, low dark current, no image lag, large saturation, high sensitivity, and allows electronic shutter operation.

2. Conventional non-PPDs have long tail lag and transfer noise.

3. A new diffusion dark current model considering the GR centers is proposed. If the P+ pinning layer is thin compared with diffusion length, they contribute to the dark current. The temperature dependence is \( J_n^{(GR)} \propto e^{E_g/kT} \).

4. Both macroscopically and atomically flatness of the silicon surface reduce the dark current.

5. VOD shutters with PPDs are capable of high speed shutter operation.