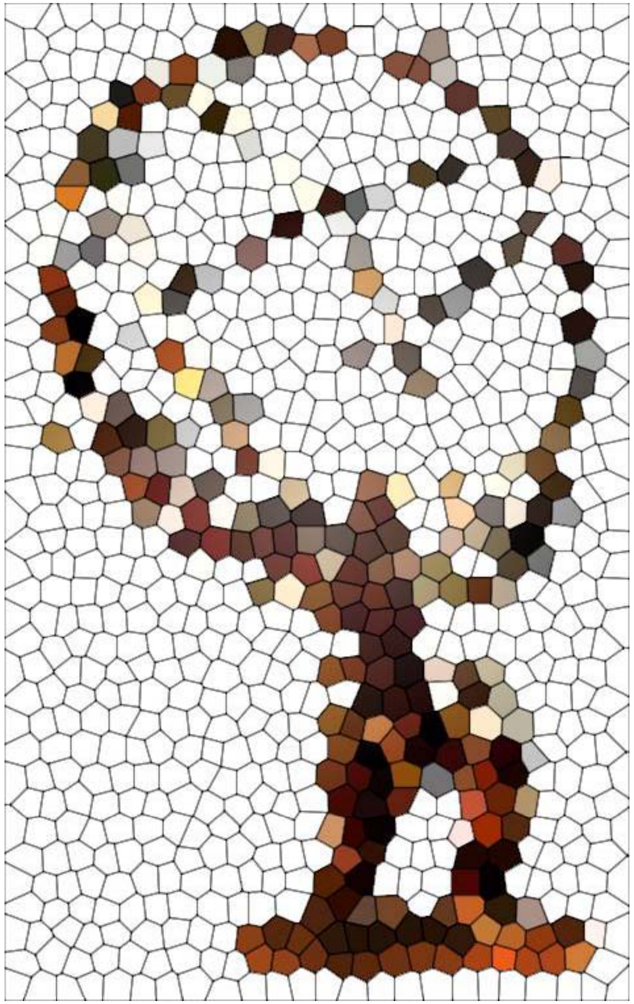
ATLAS Insertable B-Layer (IBL)

LHCC Upgrade Review
CERN, February 16, 2009

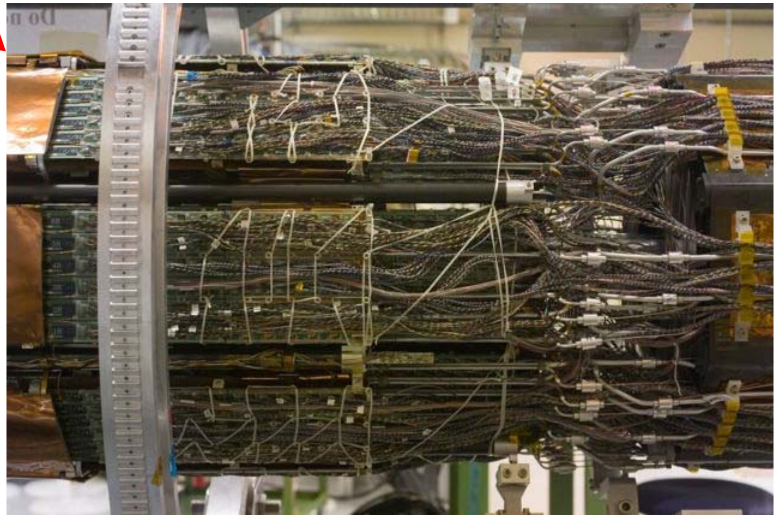
G. Darbo - INFN / Genova



LHCC Review Agenda page:
http://indico.cern.ch/conferenceDisplay.py?confId=52276

From Replacement to Insertable BL

- *One and half year ago (29/9/2007) the B-Layer Replacement Workshop.*
  - Serious difficulties found in the original idea of replacement:
    - Longer than foreseen shutdown of LHC for replacement (>1 year);
    - Activation of present detector ← safety issues;
    - Need to dismount service panels, disks, etc to access B-Layer ← time, risk of damage.



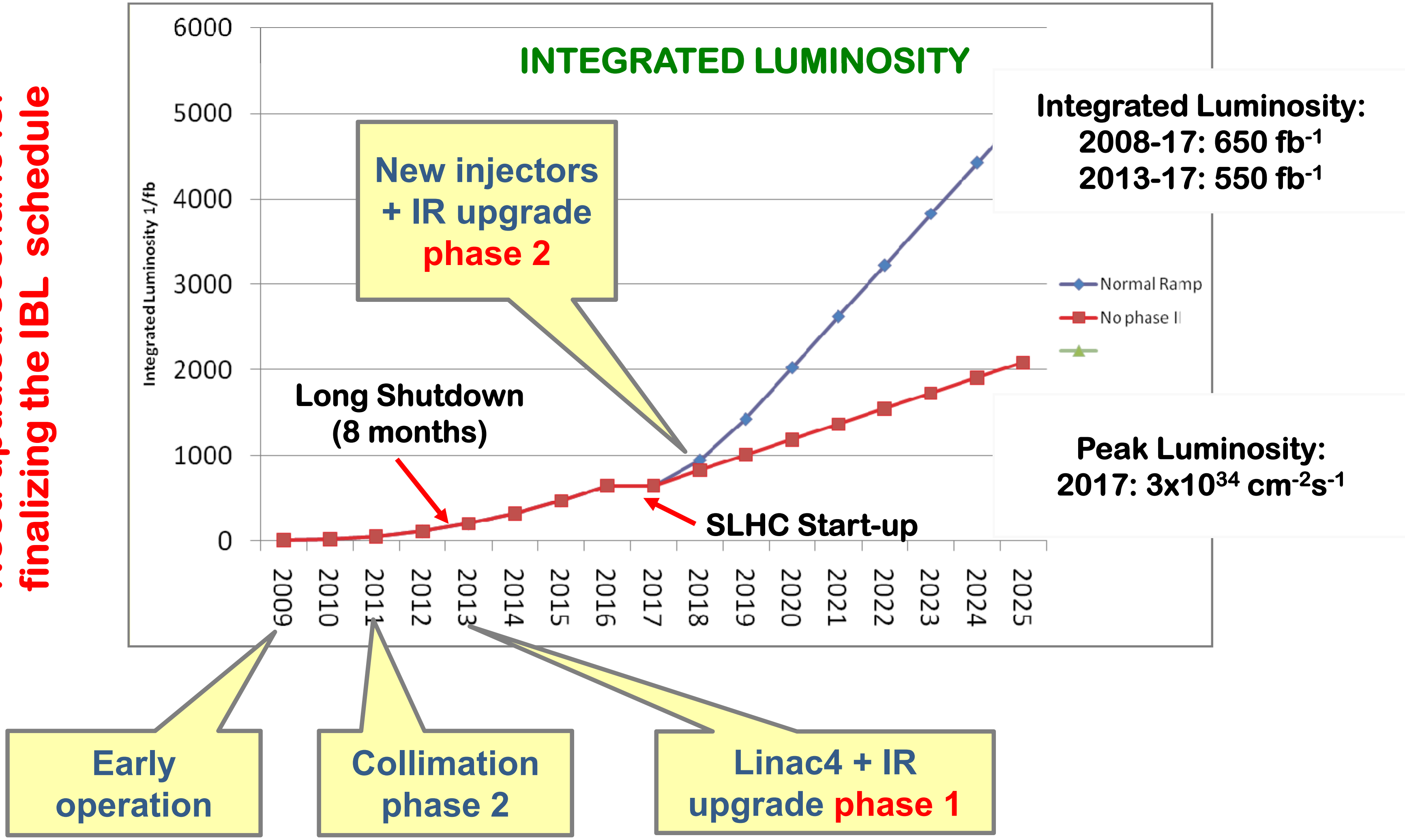
- *ATLAS appointed a B-Layer Task Force (BLTF):*
  - Jan to Jun 2008 – BLTF convened every two weeks, chairs: A.Clark & G.Mornacchi;
  - July 2008 – BLTF Reported at Bern ATLAS Week, written document sent to the ATLAS EB.

- *An Insertable B-Layer (IBL) was the main recommendation of the BLTF:*
  - ATLAS will appoint the IBL Project Leader this week;
  - Very motivated Pixel and Project Office groups, fully behind it.

LHCC: Integrated Luminosity

- *Integrated luminosity affects detector life – Peak Luminosity affects R/O*

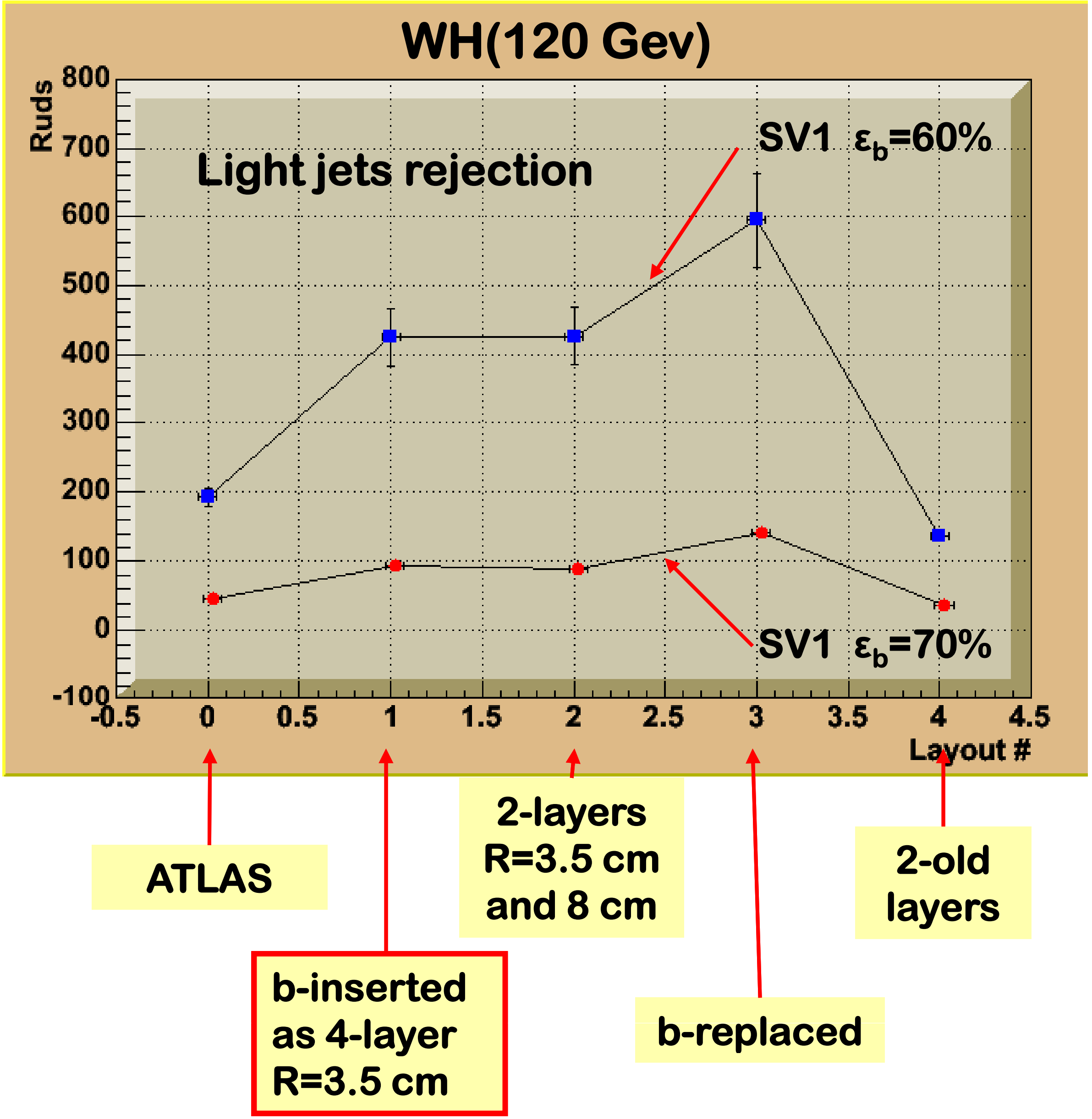
Before LHC accident.
Need updated scenario for finalizing the IBL schedule



Ref: LHCC 1/7/2008 – Roland Garoby

B-Layer Scenarios

- *To maintain Pixel Detector performance with inserted layer, material budget is critical.*
- *Development of new local support structure with carbon-carbon foams.*



Component	% X_0
beam-pipe	0.6
New-BL @ R=3.5 cm	1.5
Old BL @ R=5 cm	2.7
L1 @ R=8 cm	2.7
L2 + Serv. @ R=12 cm	3.5
Total	*11.0*

Main IBL Challenge

- *Beam pipe extraction and installation of the IBL + new Beam pipe*
  - Complicated by material activation.

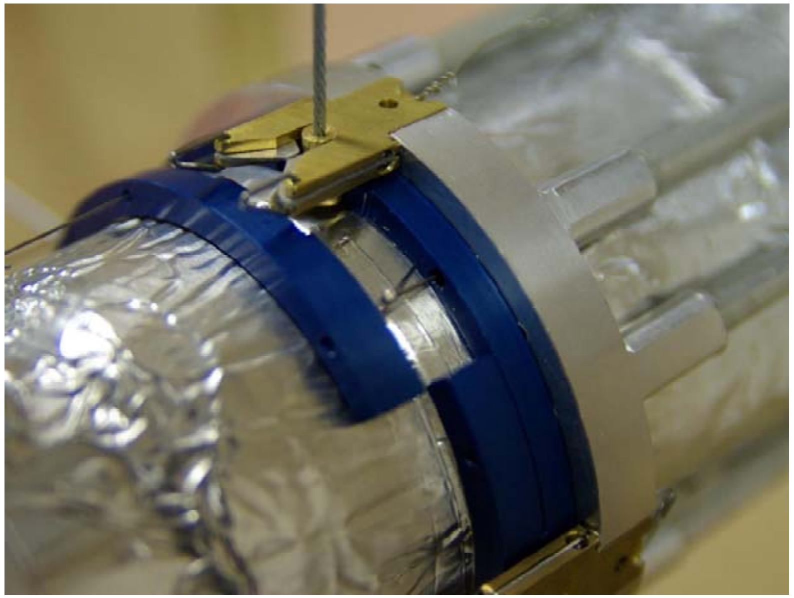
- *Fight everywhere for space: engineers are starting with making a real design.*
  - Layout to fit into tight envelopes between present B-Layer and beam pipe.
  - Additional services (pipes, opto-fibers, electrical services).
  - Reduce beam pipe radius (Current internal r = 0.29). IBL assumes r = 0.25, with reduced isolation (from 8mm to 4mm). Smaller radius is investigated.

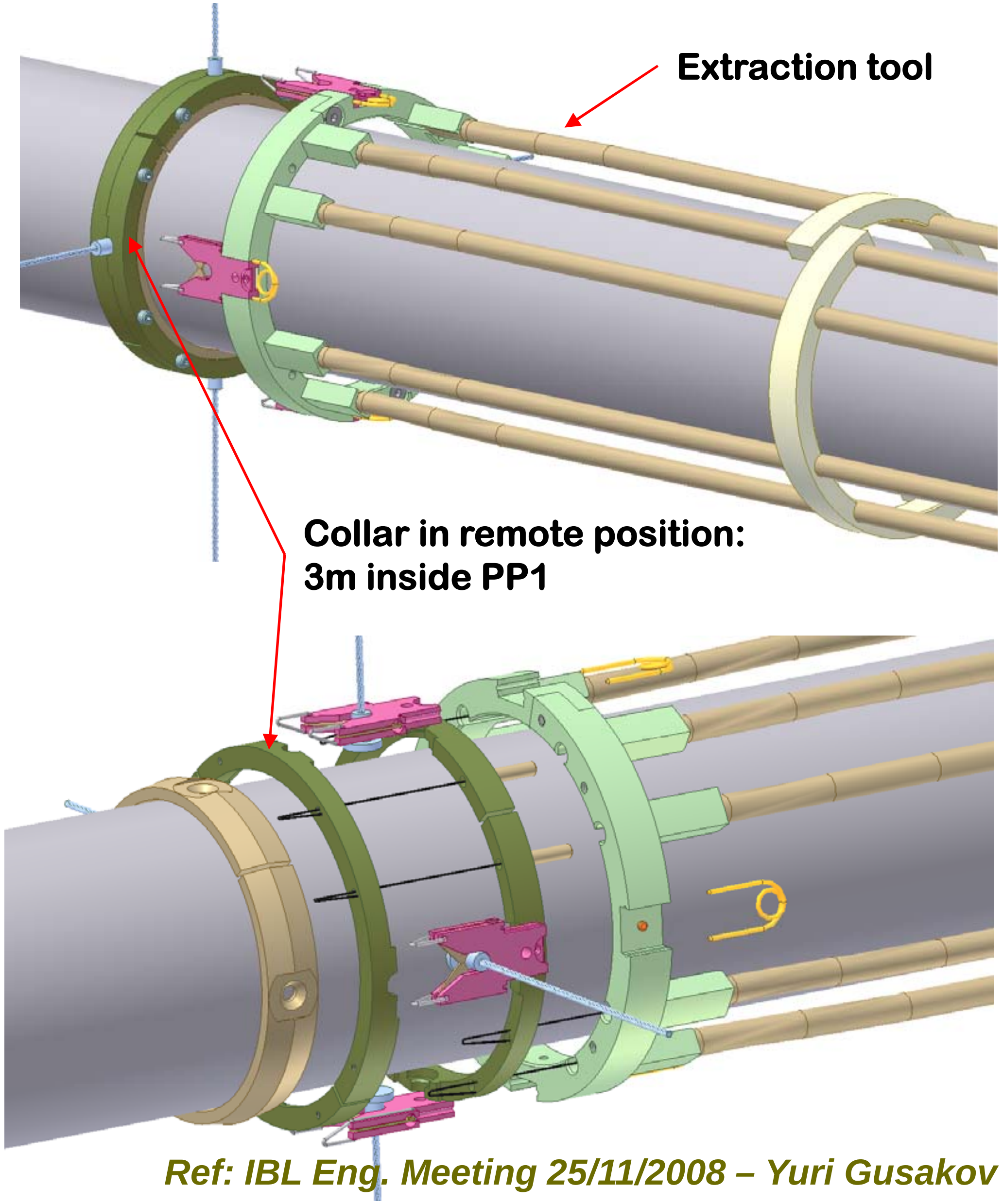
- *Keep low the IBL radiation-length:*
  - Low radiation length (X_0 = 60% of B-Layer) and smaller detector radius improve current Pixel detector physics performance (even with inefficient B-Layer).
  - Carbon-carbon foams with low density ($\rho \sim 0.1 \div 0.2$ g/cc) and reasonable thermal conductivity ($K \sim 6 \div 18$ W/m•K).
  - Head room in the cooling: low T, small fluid mass.
  - Electrical services low mass: Al (instead of Cu); high signal bandwidths.
  - Large active area in the modules (big FE chips).

- *Front-end chip and sensor design:*
  - Higher radiation dose (200Mrad, 2x1016 n_{eq}/cm^2), higher R/O bandwidths.

Challenges: Beam Pipe Removal

- *Tools to dismount Beam Pipe support collars:*
  - Remote access >3 m inside
  - Activated material – fast operation
- *Beam pipe must been supported from inside.*
  - Tool has to compensate gravity bow (7m long pipe).





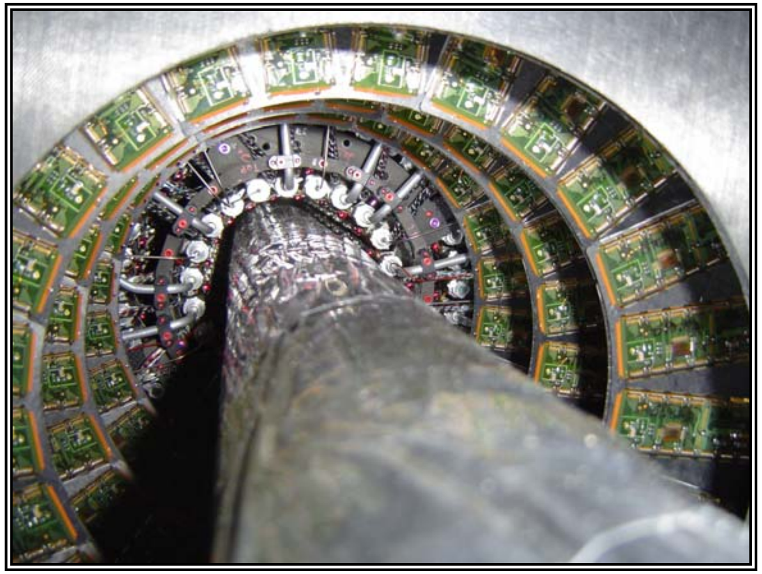
Ref: IBL Eng. Meeting 25/11/2008 – Yuri Gusakov

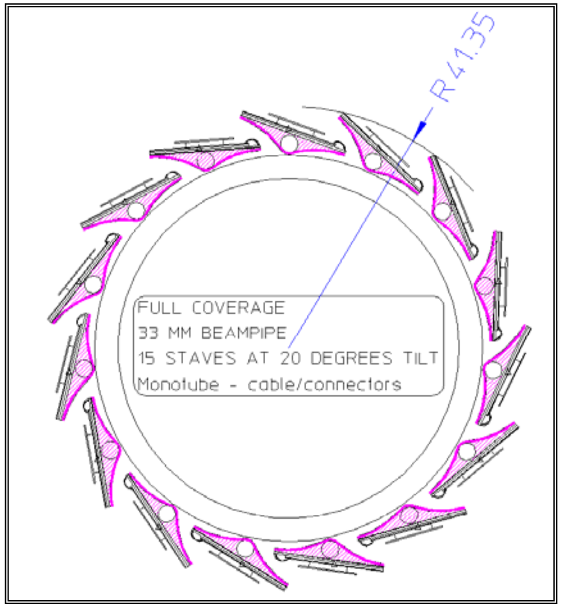
B-Layer Replacement - Insertion

Smaller radius B-layer to insert in the existing Pixel

- 16-staves (current module "active" footprint gives hermetic coverage in phi, but current total width does not fit); IBL will be not shingled in Z (no space). Requires new smaller beam-pipe; beam-pipe Ø is the most important inputs
- Pixel Modules: increase live area of the footprint:
    - New chip design (FE-I4) – live fraction, I/O bandwidth, 200 Mrad;
    - Sensor – increase radiation hard (smaller radius and ramping up LHC luminosity): $3x10^{15}$ n_{eq}/cm^2. New radiation dose simulation is going on with new release of Fluka.

R&D and prototyping in 2009, construction 2010-2012;

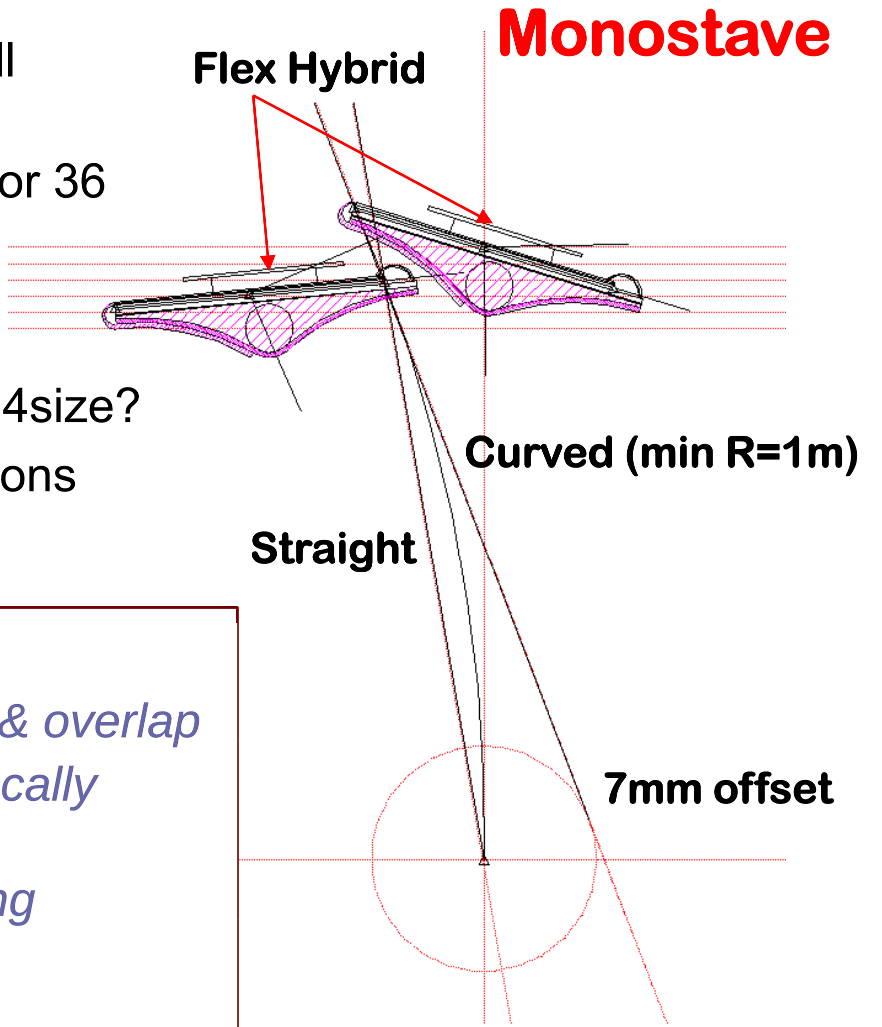




Possible Layouts

With "agreed" FE-I4 size full coverage

- Fighting for space to old b-layer against full coverage
- 15 staves looks the most promising, at 35 or 36 mm radius, but mechanically is tight
- We may not profit from smaller radius beampipe so much if we want full coverage (agreed module size). Tune FE-I4size?
- We are also looking at several bistave options with inependent cooling circuits

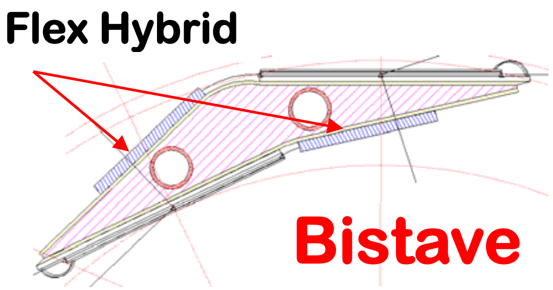


Coverage Diagram

Ref.: Neal Hartman

Castellated layer

- *7 bistaves*
- *0 tilt*
- *32.5 IR, 41.5 OR*



Bistave atractive:

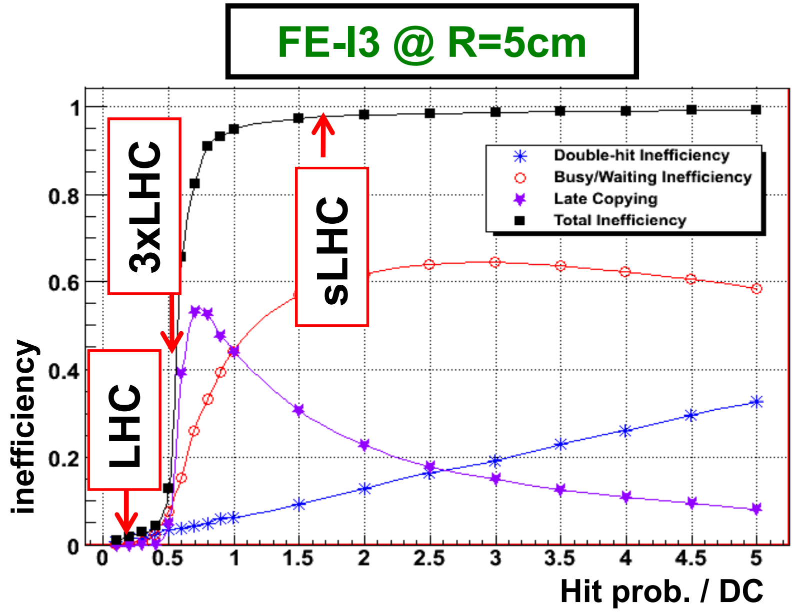
- *Good clearace & overlap*
- *More mechaniccally stable*
- *Potenzial cooling redundance*

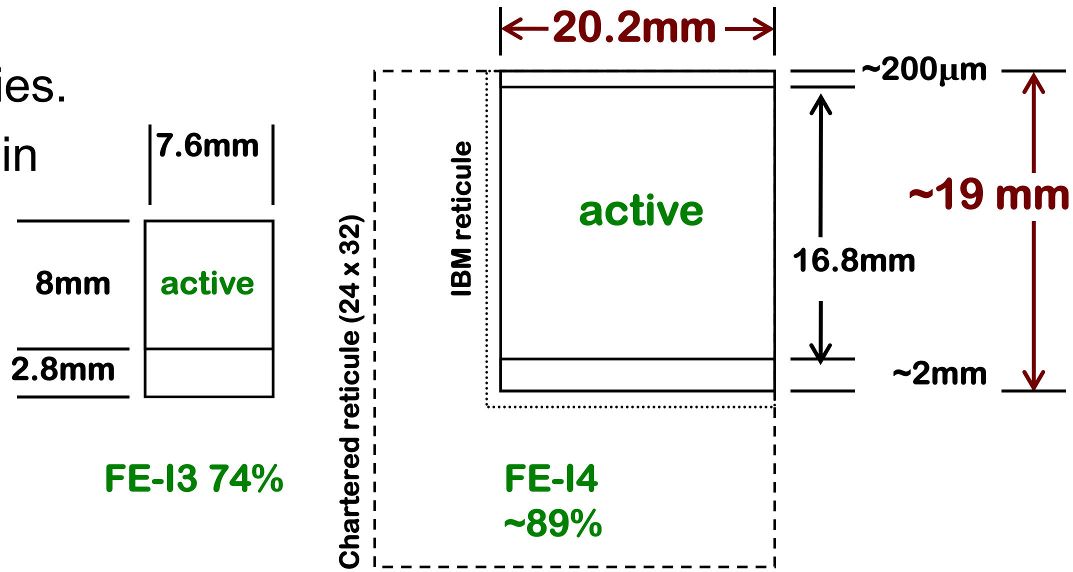
However:

- *More difficult handling*
- *Support may only be possible on one end*

Frontend Chip - FE-I4

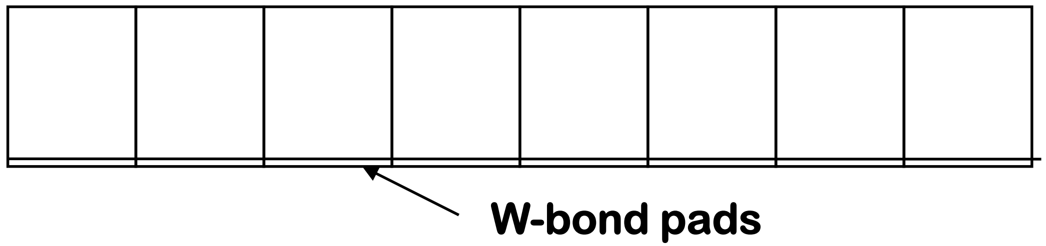
- *Reasons for a new FE design:*
  - Increase live fraction
  - New architecture to reduce inefficiencies ($\mathcal{L}$=3xLHC)
- *New FE-I4*
  - Pixel size = 250 x 50 μm^2
  - Pixels = 80 x 336
  - Technology = 0.13μm
  - Power = 0.5 W/cm^2
- *FE-I4 Design Status*
  - Contribution from 5 laboratories.
  - Main blocks MPW submitted in Spring 2008.
  - Full FE-I4 Review: 2/3/3009
  - Submission in Summer



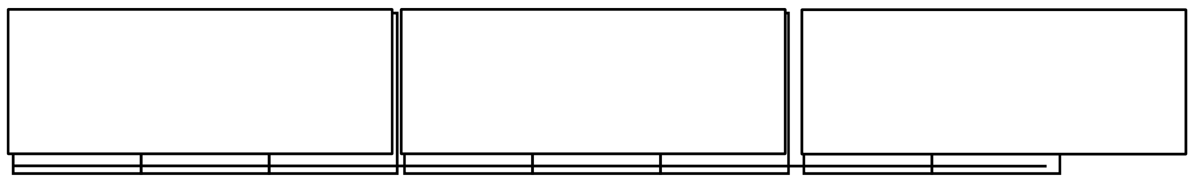


Modules & Stave Arrangement

- *Two module options:*
  - Single chip modules abut one against the next
  - Small sensor type: like 3D, active edge



  - Multi chip modules: chip look the same if using multi-chip modules
  - As present sensor size (~3xFE-I4) : like planar n-on-n



  - assuming no Z-shingling, no space.

Sensors Options

- *Two "silicon" technologies considered: Planar and 3D sensors.*
  - Could profit from 2 large "SLHC" R&D communities.

3D sensor

- *pro's:*
  - Larger charge collection after irradiation (but more power in the FE for same time-walk)
  - Active edge (butting modules)
  - Lower voltage (<150 V), power after irradiation
- *Con's:*
  - column Inefficiency at 90º
  - Higher C_{det}
  - No experience in "scale" production
  - Several options and design flavours
  - Higher cost. Yield?

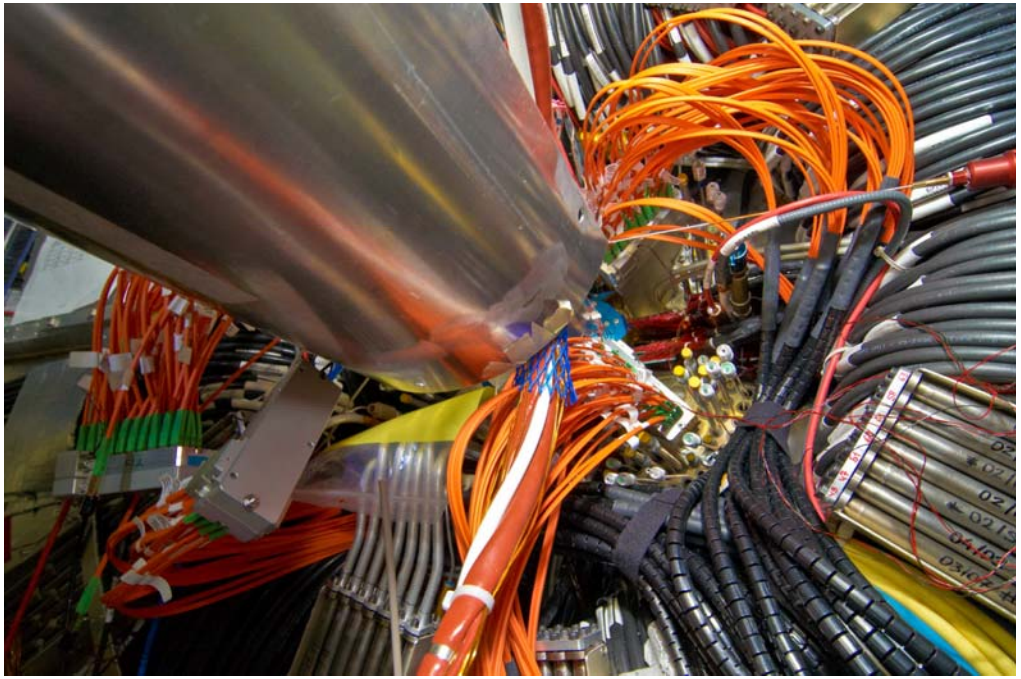
Planar (n-on-n)

- *Pro's*
  - n-on-n is a proven technology
  - Lower C_{det} -> lower noise, lower in-time threshold for same power settings in the FE.
  - Partially depleted sensors collect charge
- *Con's*
  - No active edge (?)
  - Guard ring -> dead area in Z, constraints the envelope (?)
  - Charge collected at $600V_{bias}$

- *Other options? Diamonds could be a compatible technology*
  - No cooling issues, low capacitance, no leakage current make them appealing…
  - Smaller community than silicon…

External Services – ID Endplate

- *Final services arrangement necessitated improvisation*
  - Cable over-length, mapping changes. Not all improvisations are documented ← in situ cross check is going on before closing of ATLAS.
  - Entering of nose region is critical even for few additional services, as available envelope is basically taken



External Services

- *Installation of additional services for IBL is certainly not straight forward*
- *Careful design on flange (and in ID endplate region) is necessary, which must combine*
  - Verification in situ – happening now before closing ID end-plate & ATLAS
  - New design/drawings (in CATIA for flange)
- *Pipe routing for eventual CO_2 cooling up to USA 15 should be o.k.*
- *Radiation protection aspects have to be considered early enough*

All installation aspects of new IBL services have to be considered from the very beginning !

Cooling – CO_2 vs C_3F_8

- *IBL cooling parameters:*
  - 15 staves with 112W each ← P_{total} =1.68kW
  - T_{sensor} -25°C, ΔT to coolant ≤10°C ← $T_{coolant}$ -35°C
- *Options (limited by main constraint: develop time & working experience):*
  - CO_2: copy of the LHCb VELO system, similar in cooling power.
  - FC: present C_3F_8 system (after modifications).
- *Consider the new ATLAS and CERN reorganisation of the Cooling group:*
  - ATLAS long term Upgrade and the improvement of present C3F8 system
  - Available Nikhef interest in contributing in the CO2 system ("cooling guru").

	C_3F_8	CO_2
$P_{evaporation}$	1.7 bar	17 bar
ΔT for ΔP=+-0.1bar	+1.4 C / -1.5C	+0.2 C / -0.2 C
ΔT for ΔP=+-1.0bar	+12 C / ~-20 C	+1.8 C / -1.9 C
ΔH for evaporation	100 J/g	280 J/g
Flow for 100 W	1.0 g/sec	0.4 g/sec
Volume flow	0.6 cm^3/sec	0.4 cm^3/sec

IBL Project Organization

- *IBL Project Leader (IBL PL) reporting to ATLAS and Pixel community:*
  - Final round of IBL PL search – (probably) ATLAS CB nominates this week

- *Project Documents*
  - Draft WBS exists: used to assign deliverables, costs and interest from ATLAS groups;
  - TDR in late 2009 (early 2010): TDR should not have options inside (sensor could be the exception);
  - Schedule: it will be agreed with CMS and LHC. Long shutdown for new triplet used to install. This will happen before the B-Layer will have seen life dose.

- *Funding Model*
  - The overall model for the B-Layer Replacement was that this part of the detector was a "consumable".
  - A dedicated line of funding, contained inside the Pixel M&O B, exists for the B-Layer Replacement. This will cover part of the costs.
  - First estimate would indicate a cost of about 7-8 MCHF, including new beampipe.

Conclusions

- *Big progress in convergence to a B-Layer project: IBL*

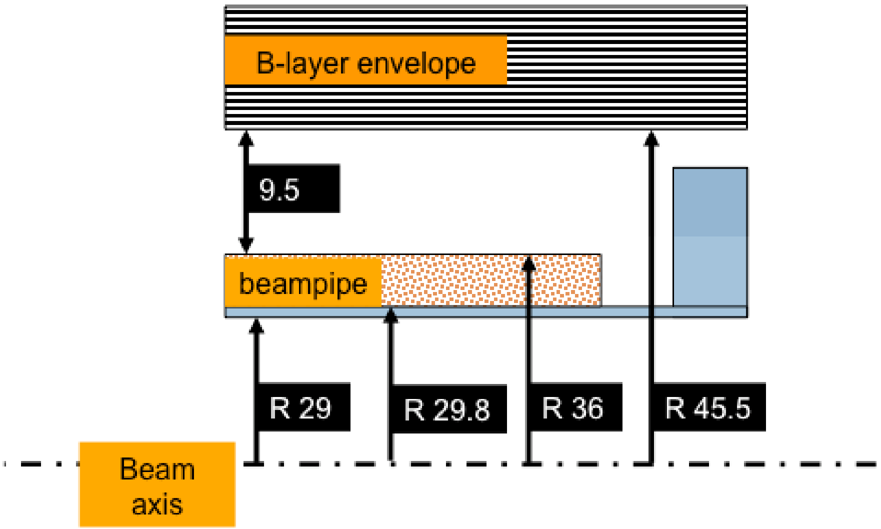
  - Feasibility studies on-going and “strawman” coming soon for several subparts
  - Organization structure will have soon Project Leader
  - Cost evaluation and funding model
  - Interest from groups to contribute. Open to Pixel and ATLAS

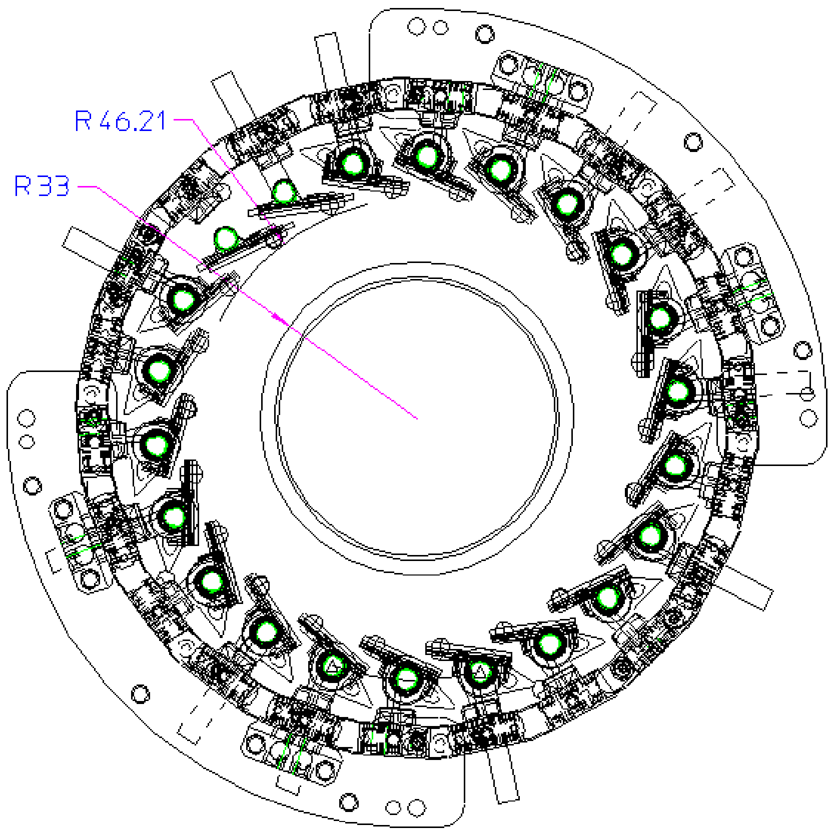
- *Challenging project*
  - It will be an “assurance” for present B-Layer both for radiation end-of-life and for hard failures
  - Time scale is short, need optimization of design and prototyping but no time for basic R&D
  - Options should be kept small: decision between option is usually long and require parallel efforts.

BACKUP SLIDES

Critical Issues – Available Envelopes

- *Nominal Current B-Layer inner radius is just over 46 mm.*
  - Envelope for B-Layer is 45.5 mm.
- *Assumed that is possible to reduce the beam pipe envelope*
  - Reduce beam pipe isolation
  - Smaller beam pipe? R=25mm?
- *Need also clearance for beam pipe alignment (together with IBL)*

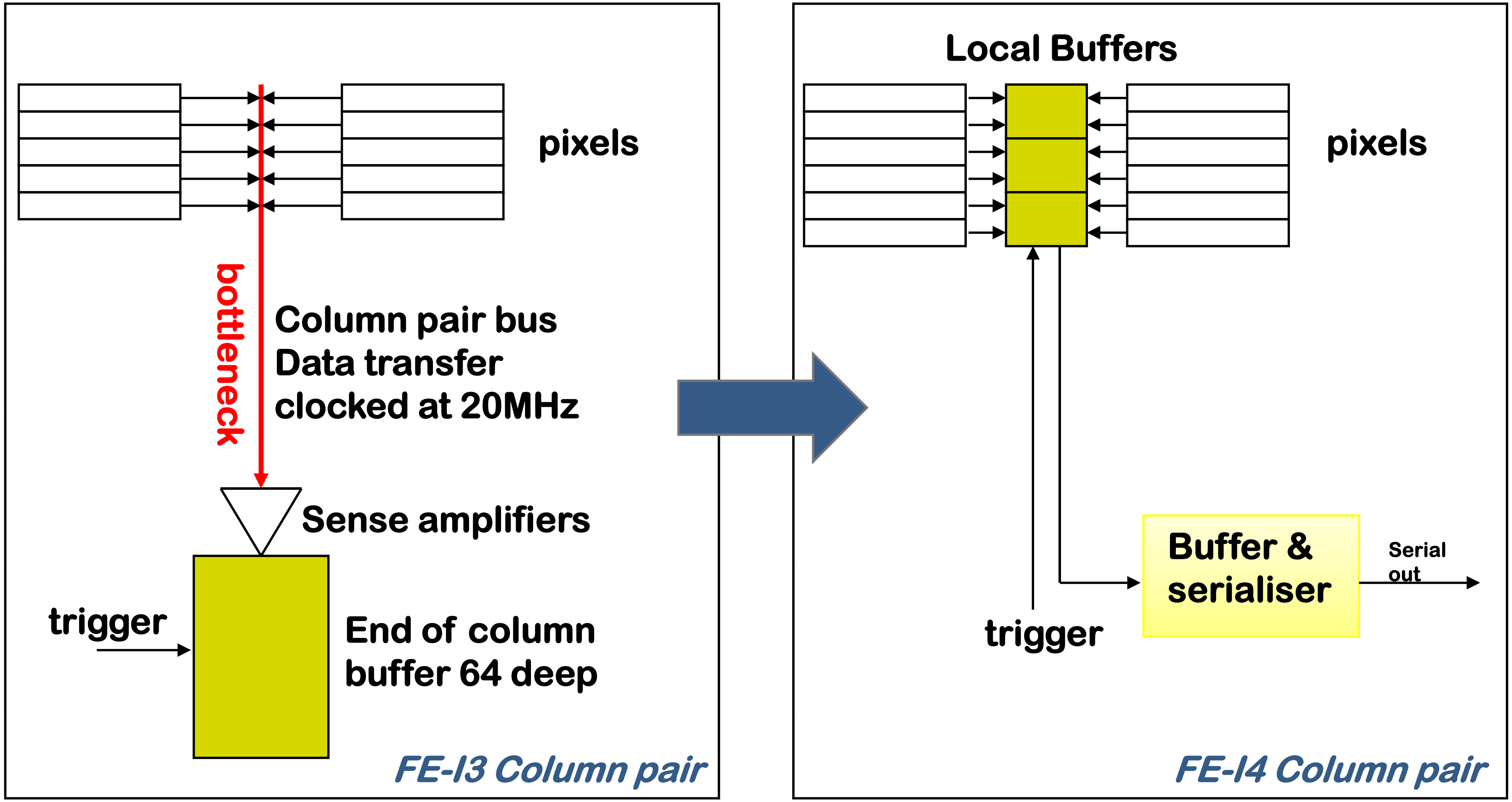




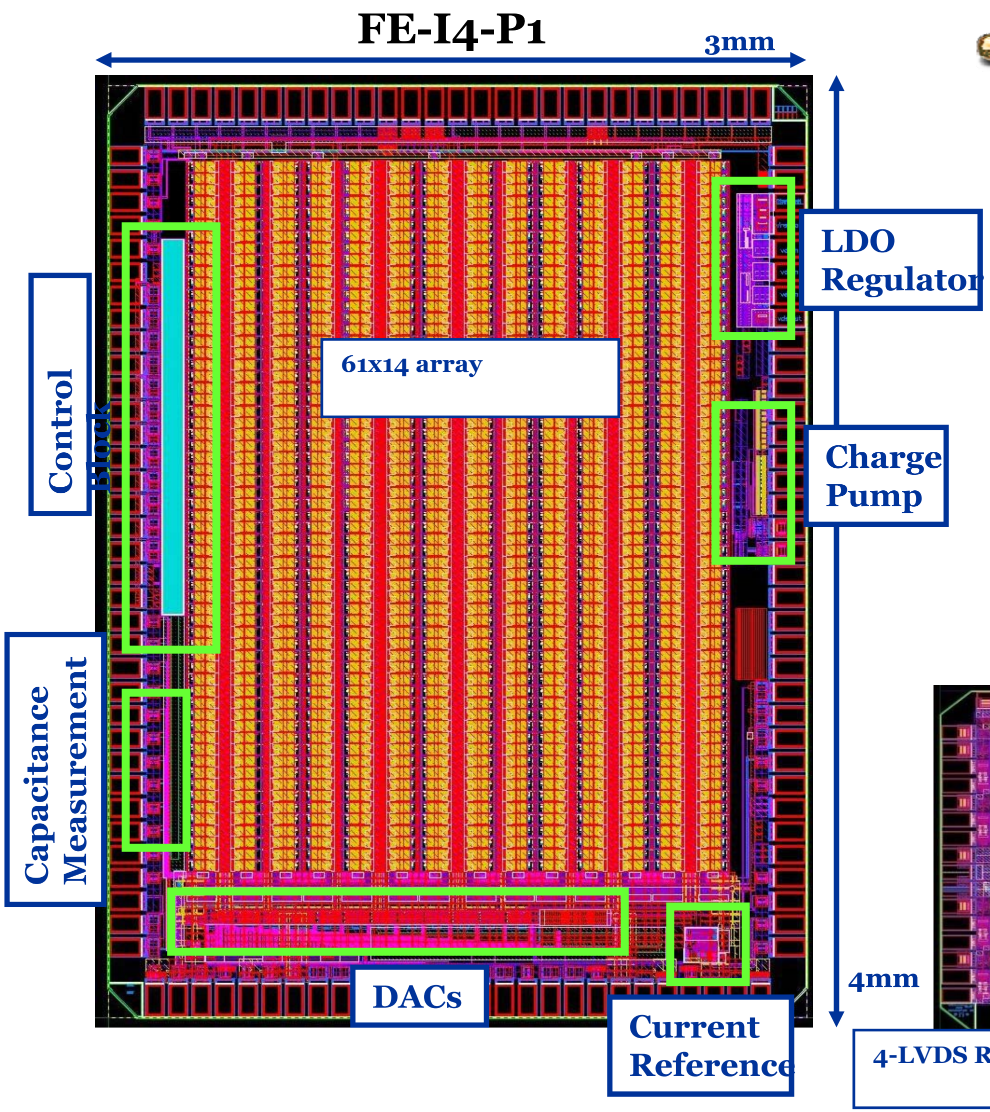
Current envelopes

FE-I4 Architecture: Obvious Solution to Bottleneck

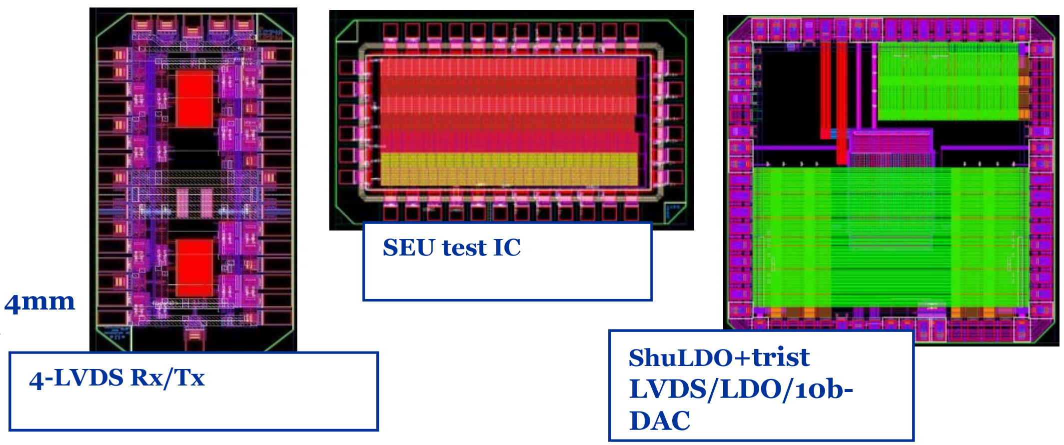
- *>99% or hits will not leave the chip (not triggered)*
  - So don't move them around inside the chip! (this will also save digital power!)
- *This requires local storage and processing in the pixel array*
  - Possible with smaller feature size technology (130nm)



FE-I4_proto1 Collaboration

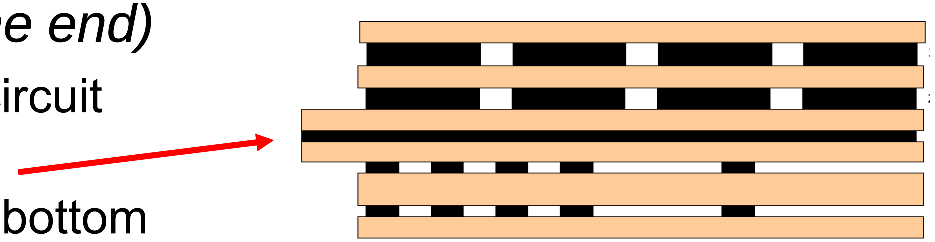


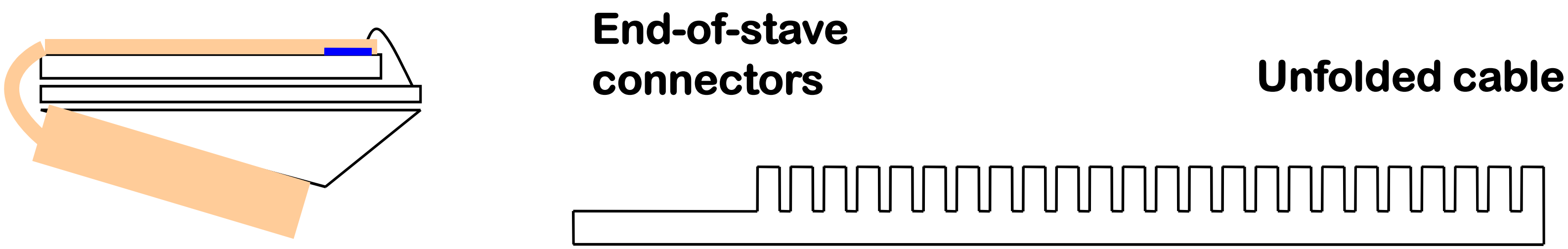
- *Participating institutes:*
  Bonn, CPPM, Genova, LBNL, Nikhef.
  Bonn: D. Arutinov, M.Barbero, T. Hemperek, M. Karagounis.
  CPPM: D. Fougeron, M. Menouni.
  Genova: R. Beccherle, G. Darbo.
  LBNL: R. Ely, M. Garcia-Sciveres, D. Gnani, A. Mekkaoui.
  Nikhef: R. Kluit, J.D. Schipper



Internal Services – Stave Cable

- *Stave cable still on conceptual stage:*
  - Cable using System Task force recommended signals + direct power.
  - Wire bonding MUST be done on stave
- *Many ideas (none developed to the end)*
  - Single cable (conceptually like a circuit board to connect the FE chips)
  - Monolithic cable on top or on the bottom
  - Single cable also possible
- *Space is limited, what about reworking?*





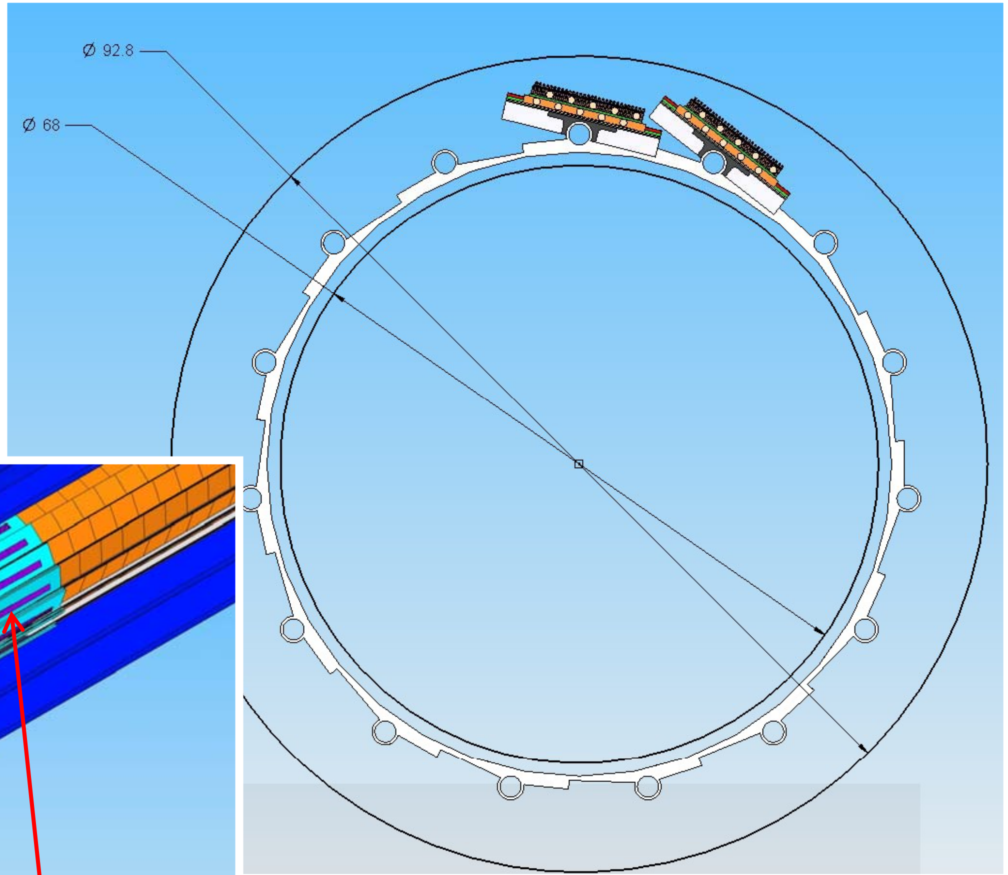
Monolithic Cable on the Bottom

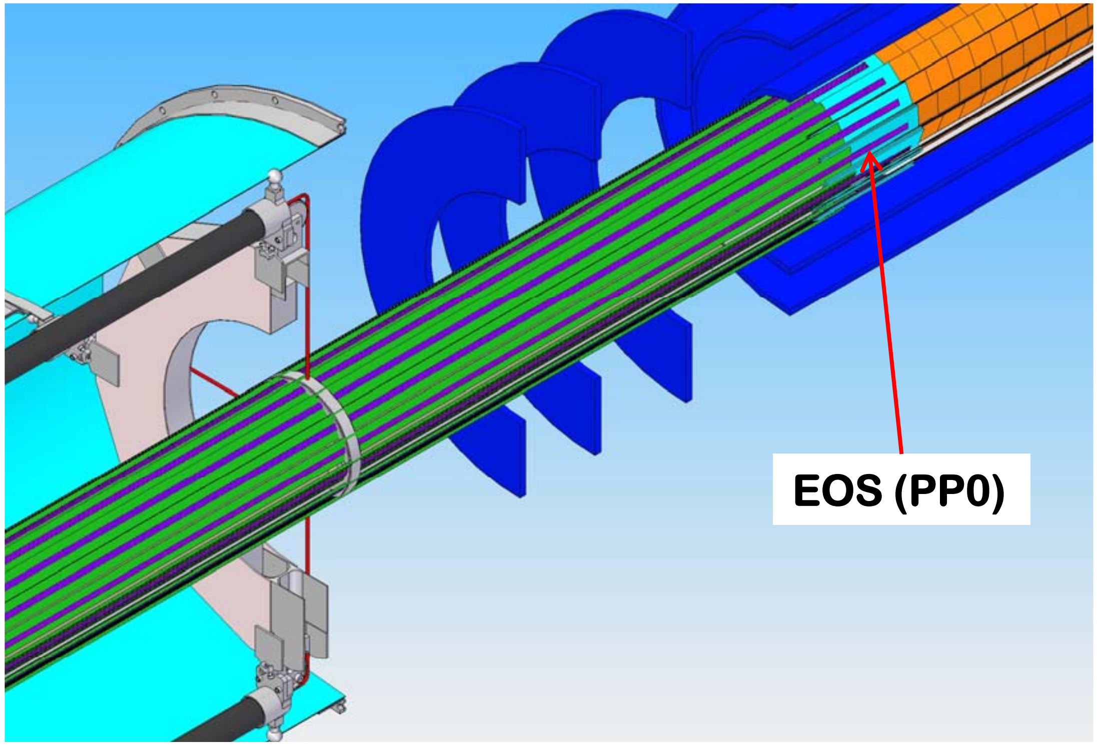
From End-of-Stave (PP0) to PP1

"Strawman" Issuess:

- *X-section of LV cables*
- *No active EOS -> 6m (FE-I4 to opto-board)*
- *Interconnection space at PP0.*
- *PP1 connectors…*

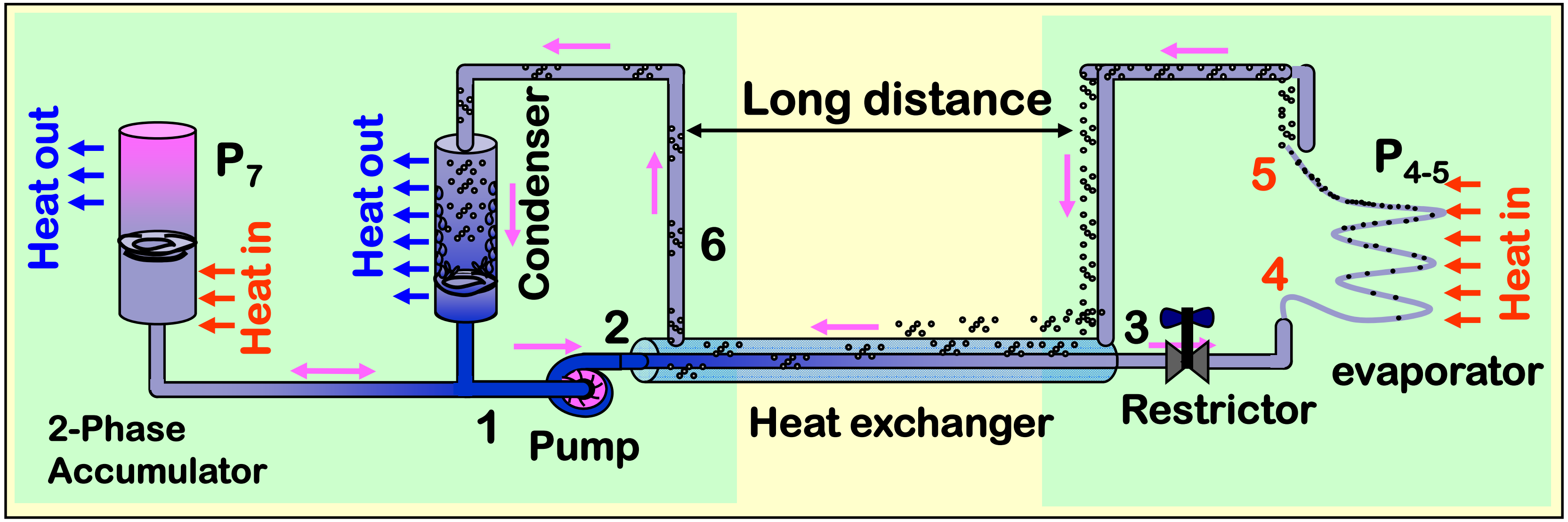
…more work to come to a design





Ref.: Marco Oriundo, Danilo Giugni, …

LHCb-VELO Cooling System



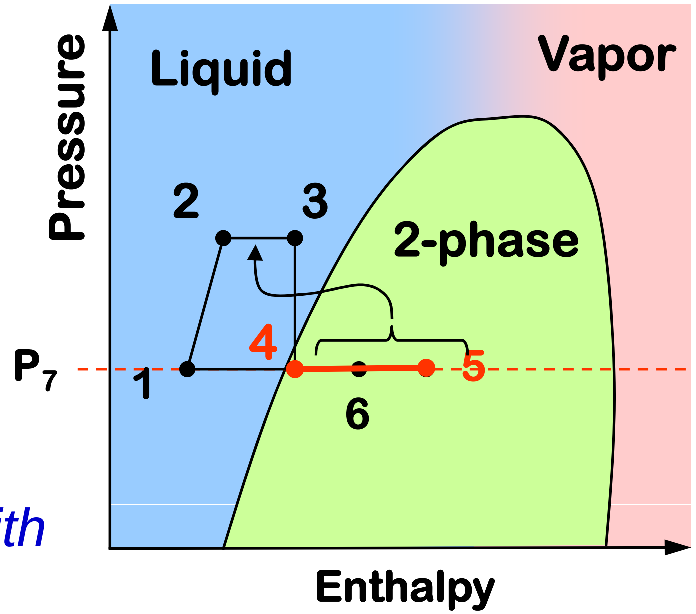
***2PACL** (2-Phase Accumulator Controlled Loop) principle of cooling:*

-Liquid overflow => no mass flow control

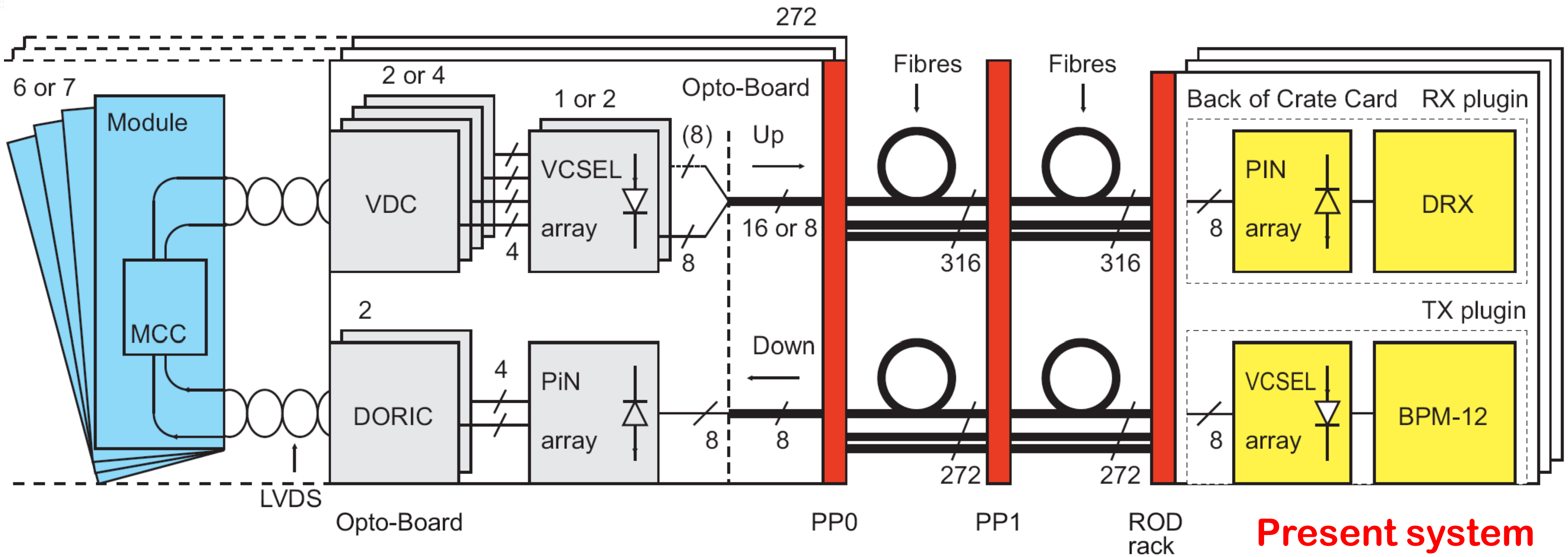
-Low vapor quality => good heat transfer

-No local evaporator control, evaporator is passive in detector

-Very stable evaporator temperature control with 2-phase accumulator ($P_{4-5} = P_7$)



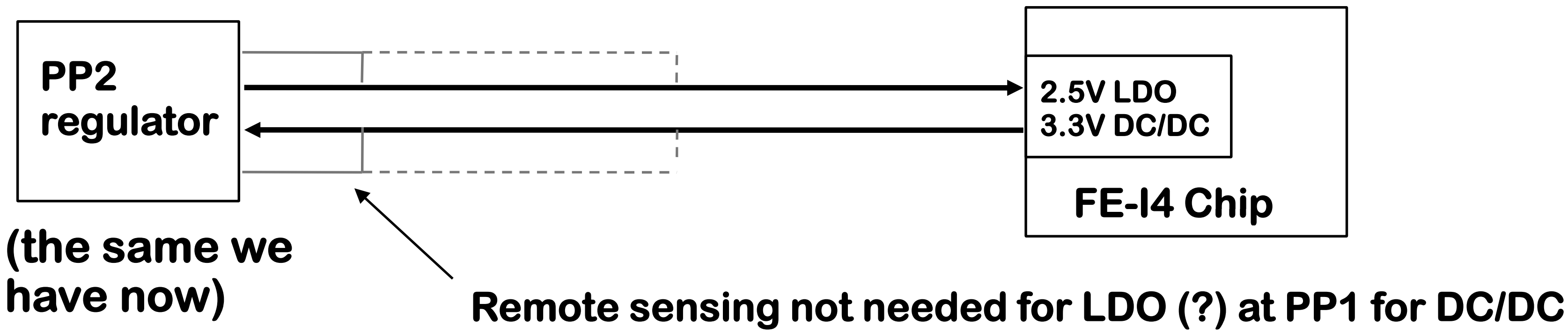
R/O Links



Present system

- *Changes (strawman R/O from System Task force):*
  - Down link (TTC) stay the same 40Mb/s (Manchester coding) – to 2 FE-I4 (?) – need clock multiplier in the FE-I4 (issues of SEU for clock multiplier).
  - Uplink use 160 Mb/s data+clock (8b/10b encode) – Single FE-I4
  - Need new BOC design (substitute custom ASIC(s) with FPGA)
  - ROD could stay the same: reprogram FPGA (or new design for x2 links: need also 2 S-Links)
  - Use GRIN fibers (under rad-test for SLHC, or new Ericsson)
  - Opto-board at PP1 – need test of reliable electrical signal transmission (~4m)

Powering and DCS



- *Power scheme – Independent powering with PP1 regulators:*
  - Use, on FE-I4 chip, x2 DC/DC and/or LDO conversion
- *DCS: similar implementation that today*
  - Temperature sensors not on each module, smaller granularity
  - More than 600V if planar sensors?
  - Minor changes needed but it has a lot of different components to build/acquire.