IC technologies, high speed links and precise timing clock distribution

Michael Campbell
EP Department
CERN
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- Paulo Moreira
- Jan Troska
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Disclaimers

1. The talk covers a very broad range of subjects and is therefore necessarily not too detailed

2. The IC technologies part is focussed on our mainstream microelectronics technologies. It does not address projects with special requirements such as DC-DC, MAPS, HR/HV CMOS, Bipolar etc
Outline

• Introduction
• Challenges for microelectronics at HL-LHC
• IC technologies
  • Common foundry access
  • Radiation hardness
  • Future
• High speed links
  • LpGBT project status
  • VL+
• Precise timing distribution
  • TTC-PON status
• Summary
Introduction

HL-LHC is set produce pile up collision rates of up to 200 per bunch crossing

This will put severe constraints on the detectors

All detector elements will see at least x10 increase in TID (pixels will see 1Grad over 10 years)

Hit rates will be as a high as 3GHz/cm² (roughly x10 higher than LHCb VELOpix in the hottest region)

Present day links will not be able to cope with the new rates

Precise timing (some 10s of ps) may help disentangle piled up events
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Challenges for microelectronics for HL-LHC

• Front-end ASICs must deal with:
  • Higher hit rates
  • Higher radiation hardness
  • Higher trigger rate (Atlas, CMS) or trigger-free operation (LHCb)

• Links must provide higher transmission rates with improved power efficiency

• If possible, high time precision detectors must be read out with time stamping at the level of 10’s of ps
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Technology Support Services

Partnerships with:
- Cadence EDA tool vendor
- Europractice IMEC, BE
- Europractice RAL, UK

Foundry vendors
IP block vendors
CAE Tools vendors

IMEC
Europractice

CERN
CAE tools & technology support

Cadence VCAD design services

CERN designers
External designers

Kostas Kloukinas
Design Kit Support in 2016-17

- All design kits will receive updates in the following months:
  - TSMC 130nm
    - Standard cell & IO pad integration fixes
    - Fixes on DRC and EXT rule files
    - Cumulative foundry PDK patches
    - CAE tools platform update*
  - TSMC 65nm
    - Possibly additional standard cell libraries
    - Cumulative foundry PDK patches
    - CAE tools platform update*
  - GF 130nm design kit
    - CAE tools platform update*

* (CADENCE GENUS_15.20, INNOVUS_15.20)
Foundry Access Services

- Organize prototyping Multi Project Wafer runs, for sharing fabrication costs
- Coordinate Engineering & Production runs

CERN designers

EUROPRACTICE (TSMC)

MOSIS (GF/IBM)

Kostas Kloukinas
Prototyping Activity

- Only prototyping works considered
- 2 engineering runs on 130nm (one using MLM)
- "new" nodes are picking up

Kostas Kloukinas
130nm GF is radiation tolerant up to ~ 100MRad but care must be taken to deal with ‘bump’ in leakage current for small devices. Alternatively Enclosed Layout Transistors can be used.

The position and height of the bump in leakage current depends on the operating temperature (lower is worse) and dose rate (higher is worse).
Radiation tolerance – TSMC 130nm

PMOS

25 C

-30 C

Stefano Michelis
130nm TSMC is radiation tolerant up to ~ 400Mrad with two caveats:
- PMOS are less degraded (x2) at low temperature.
- NMOS don’t leak but this is foundry dependent.

NB No large chips rad tested yet. VELOpix will be the first
Radiation Tolerance - TSMC 65nm

Narrow channel PMOS transistors do not work above 500Mrad, while NMOS are working without large damage up to 1Grad

Transistor size: W=120nm, L=1um
Irradiation conditions: T = 25°C
Bias: |Vgs|=|Vds|=1.2V
At low temp PMOS degradation is attenuated.

Transistors’ size: W=0.6um, L=60nm
Irradiation conditions:
Bias: $|V_{gs}|=|V_{ds}|=1.2V$
Low temp operation *may* be ok
Evaluating the Sensitivity of Standard Cell Libraries in 65nm (DRAD) – RD53

- Set of ring oscillators irradiated up to 700 Mrad (at room temperature):
  - No annealing step shown
  - As expected, from the tests of individual devices, libraries made out of large devices are more tolerant than the smaller devices counterparts
  - Large devices lead to large power dissipation!

INVD1 ring oscillator frequency (normalized to the pre-rad value)

Paulo Moreira
But beware of low dose rate effects

Room Temperature measurements
Radiation tolerance – TSMC 65nm

- PMOS transistors (and short channel NMOS) degrade strongly beyond 500MRad
- Measurements and simple defect modelling suggest effects are attenuated at low temp but only if this is maintained continuously
- Measurements at different dose rates would indicate that the effect is worse at low dose rate
- Measurements at low dose rate and low temp are needed urgently
Radiation tolerance – TSMC 28nm

Collaboration between CERN, EPFL, INFN and University of Bicocca, Milan and Universities of Udine and Padova. The Scaltech28 and GigaRadMOST projects are funded by INFN and SNSF respectively.

TID(Mrad): 0, 10, 50, 140, 340, 540, 940, 1000
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Why Optical Links in HEP?

- Small optical fibre cross section (material budget)
- Immunity to interference
- Non EMI generator
- No contribution to ground loops
[At least] Two “Strategies” Necessary!

Pixel systems (ATLAS)
- Very high readout rates:
  - 2 – 4 Gb/s per PROC in inner layer
- Very high radiation (10 years):
  - 1 Grad
  - \(2 \times 10^{16}\) n/cm²
- PROC drives directly the VCSEL driver: ~5 Gb/s

Outer detector systems
E.g. Tracker systems;
- Very high readout rates:
  - 5 – 10 Gb/s per Module
- Moderately high radiation (10 years):
  - 100 Mrad
  - \(10^{15}\) n/cm²
- ROC connects to the SerDes: 320 - 640 Mb/s

Paulo Moreira
The VL+ & LpGBT Projects

- Development of Radiation Hard Optical Links
  - For the Phase II Upgrades of the experiments (HL – LHC)
    - Installation during the Long Shutdown 3 (Centred around ~2024)
- Main objectives
  - Data rates:
    - 5.12 to 10.24 Gb/s for up links
    - 2.56 Gb/s for down links
  - Environment
    - Total Dose: 100 Mrad qualification (200 Mrad LpGBT chipset)
    - Total Fluence: $2 \times 10^{15}$ n/cm$^2$ and $1 \times 10^{15}$ hadrons/cm$^2$
    - Temperature: -35 to +60 °C
  - Reduce the power consumption of the data transmission systems
  - Reduce the footprint of the electronic and optoelectronic components
- Optoelectronic components (VL+):
  - A low-profile package
  - Configurable:
    - Number of channels
    - Unidirectional / bidirectional
LpGBT ASIC – High Speed SerDes

- Data transceiver with fixed and “deterministic” latency both for up and down links.
  - Clocks and Data
- Down link:
  - 2.56 Gb/s
  - FEC12
- Up link:
  - 5.12 Gb/s or 10.24 Gb/s
  - FEC5 or FEC12
- E-Links:
  - Data rates:
    - 160 / 320 / 640 / 1280 Mb/s
  - Count:
    - FEC5
      - Up to 28 @ 160 Mb/s
      - Up to 7 @ 1.28 Gb/s
    - FEC12
      - Up to 24 @ 160 Mb/s
      - Up to 6 @ 1.28 Gb/s
- Power dissipation:
  - Target: ≤ 500 mW @ 5.12 Gb/s
  - (GBTX is ~2W, all functions active)
- Small Footprint:
  - Size: 9 mm x 9 mm
  - Fine Pitch: 0.5 mm
  - Pin count: 289 (17 x 17)
- Radiation tolerance:
  - 200 Mrad
  - SEU robust

*FEC = Forward Error Correction

Paulo Moreira
Project Status : LpGBTXX

- Custom Design
  - Ring and LC oscillator based PLL
  - 10 Gb/s line driver
  - Fast LVT ELT digital library
  - Phase-aligner DLL
  - ePort Driver / Receiver

- RTL
  - I2C Slave
  - I2C Master
  - IC link
  - Scrambler/Descrambler
  - ePort RX/TX

- Project Schedule
  - Specification Q2 2015
  - Full chip prototype Q3 2017
  - Full chip prototype testing Q1 2018
  - Final Engineering run Q4 2018
  - First production batch Q4 2019
  - Completion of production 2020

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<td>Self Test BERT Rx</td>
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Paulo Moreira
VL+ module

- Versatile
  - multi-channel, Rx/Tx count configurable at build time
- MM only
  - 850 nm VCSEL
  - InGaAs PIN (TBC)
- Miniaturized
  - Target dimensions 20 x 10 x 2 mm
- Pluggable
  - Either optical or electrical (or both) connector
- Data-rate:
  - Tx: 5 and 10 Gb/s
  - Rx: 2.5 Gb/s (and 5 Gb/s?)
- Environment
  - Temperature: -35 to +60 °C
  - Total Dose: 1 MGy qualification (investigations up to 2 MGy)
  - Total Fluence: $2 \times 10^{15}$ n/cm² and $1 \times 10^{15}$ hadrons/cm²

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 michael.campbell@cern.ch

 Jan Troska
 Silicon Photonics

Silicon photonics Dream:

Dream: Lasers, waveguides, photo-detectors, modulators, and electronics all “grown” on the same piece of silicon

Implementation:

- A photonic system using silicon as an optical medium
- Silicon is patterned with sub-micron precision into planar micro-photonic components:
- Precise lithography technology already developed for CMOS
- Lasers and PIN-diodes have to be made in other technologies rather than Si

Silicon photonics research in HEP

- Study of radiation hardness of Mach-Zehnder modulators:
- Naturally hard to NIEL but not TID
- Successful design of a TID tolerant MZ modulator
- 10 Gb/s RadTol modulator driver design started

It has a high integration potential and it “opens the door” to:

- Multi channel links
- Advanced modulation schemes

But several challenges still to be solved for HEP systems to become a reality!

See: Francois Vasey, EP Detector Seminar, “Silicon Photonics for HEP Applications, Myth or Reality?”
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• Summary
Current TTC (Timing, Trigger and Control)

- Unidirectional system
- 1:32 split ratio
- 1310nm
- 40Mb/s per channel (2 channels CLK, data)
- Busy/throttle on a separate link
System jitter at top of CMS distribution tree
- After receiver and clock selection circuits

- NB Jitter is measured in ps rms

- e.g. SR4 jitter in range 100 Hz to 1 MHz: 1.3 ps
- RF2TTC output in same range: 9.7 ps

Jan Troska
Introduction to PONs (Passive Optical Networks)

- Technology used in FTTH (Fibre to the Home)
- Bidirectional
- Two wavelengths (1/direction)
- Downstream (OLT->ONU)
  - High bandwidth
- Upstream (ONU->OLT)
  - TDMA (shared bandwidth)

OLT= Optical Line Terminal (master)
ONU= Optical Network Unit (slave)
Introduction to the TTC-PON system

OLT = Optical Line Terminal (master)
ONU = Optical Network Unit (slave)

Sophie Baron
Downstream Jitter Map – PON only

- Phase Noise Analysis -
  source_40MHz

- MMCM - source_40MHz / jitter=43.3873ps
- PONSi5338 - source_40MHz / jitter=24.996ps
- PONSi5345_200BW - source_40MHz / jitter=4.9499ps

NB Jitter is measured in ps rms

Sophie Baron
Downstream Jitter Map – PON + GBT

- Phase Noise Analysis -
ELINK0

**NB Jitter is measured in ps rms**

Sophie Baron
Conclusions

- The radiation tolerance of 65nm CMOS is still under intense study. At low operating temperature it may be resistant to ~500Mrad but experimental confirmation at low dose rate is needed.

- Very preliminary measurements on 28nm are somewhat encouraging

- The LpGBT project aims to provide radiation hard (~200Mrad TID) high speed (10Gbps) and low power links (x4 less than GBTx). Progressing well.

- The VL+ project aims to provide a radiation tolerant (100Mrad TID) small footprint optical link. Design is underway and a commercial supplier being sought

- Transmission of timing data at < 10ps rms seems to be feasible under various realistic scenarios
Thanks for your attention!