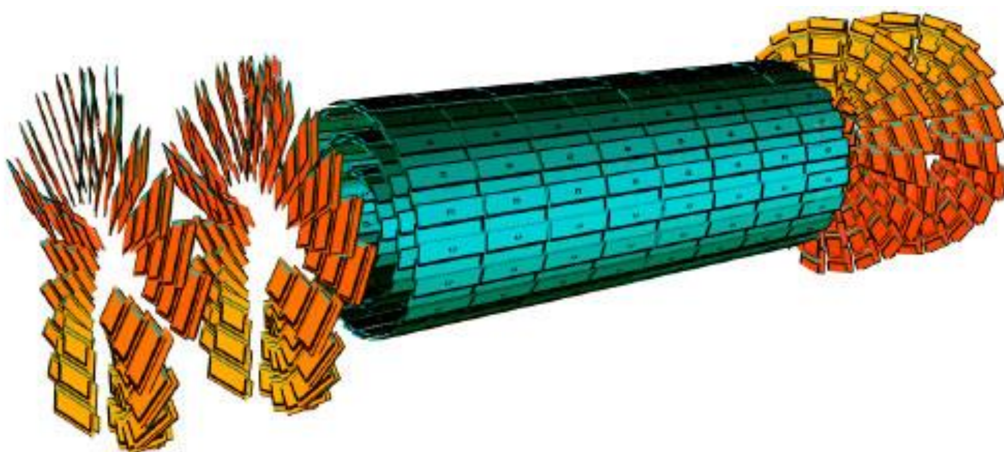
Cornell University
Floyd R. Newman Laboratory for
Elementary-Particle Physics

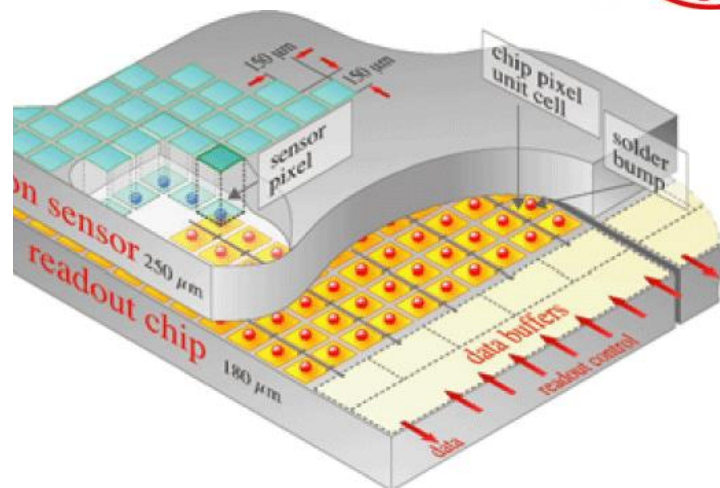
Pixel Tracker R&D

Julia Thom-Levy, Cornell University, for the CMS Collaboration

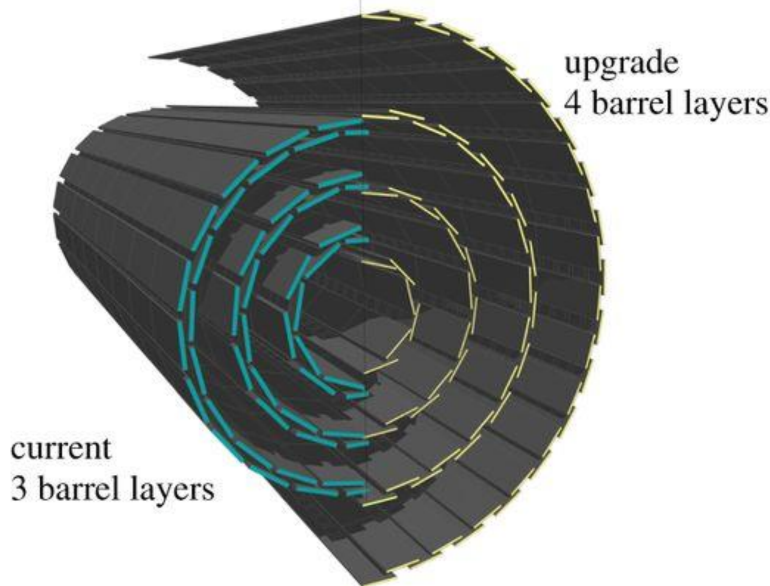
ECFA High Luminosity LHC Experiments Workshop-2016
October 3-6, 2016

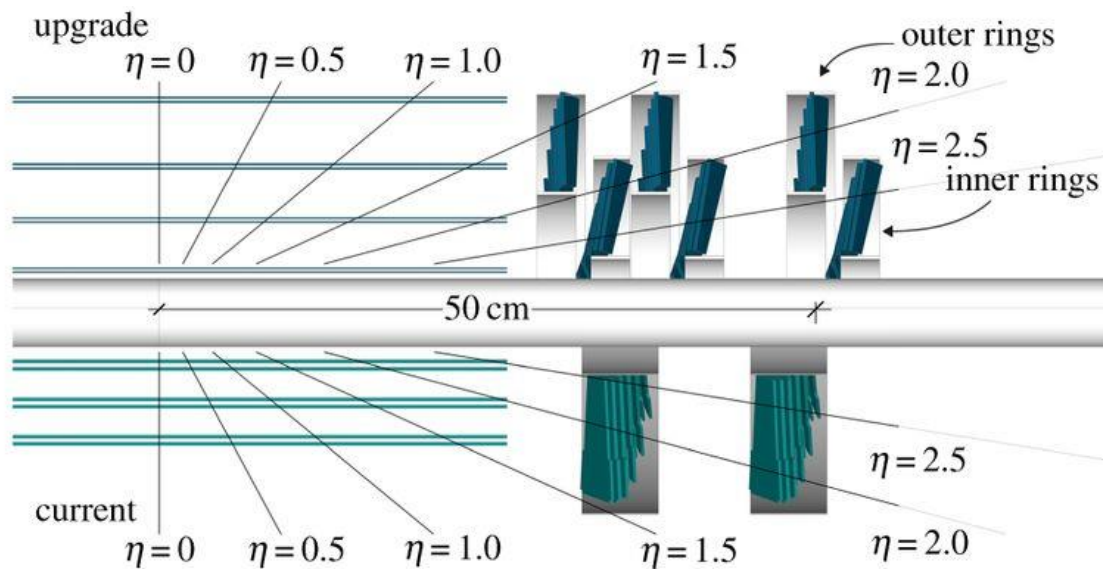
Current/Phase 1 Pixel Tracker in CMS





Phase 1 upgrade:





HL-LHC Conditions

- Integrated luminosity up to 3000 fb^{-1}, resulting in harsh radiation environment

- Instantaneous luminosity up to 7.5E34 $cm^{-2}s^{-1}$ and <PU>~200

→ particle rate up to 750 MHz/cm^2 (hit rate up to 3 GHz/cm^2)

For comparison, the current tracker is designed for 500 fb^{-1} and 1E15n_{eq}/cm^2, <PU>~50

HL-LHC CMS Pixels: Design

Preserve two track separation in high energy jets and maintain occupancy at ≈ % level

- higher granularity (smaller pixels)
- Pixel size ~ 25x100 μm^2 or 50x50 μm^2 (currently 100x150 μm^2)

Pileup mitigation, improvement of MET reconstruction, reconstruct high eta jets

- extend pixel coverage, extend $|\eta|$ to 4 ($|\eta| <2.5$ in Phase1)

Conserve or improve tracking performance, momentum resolution

- low material budget

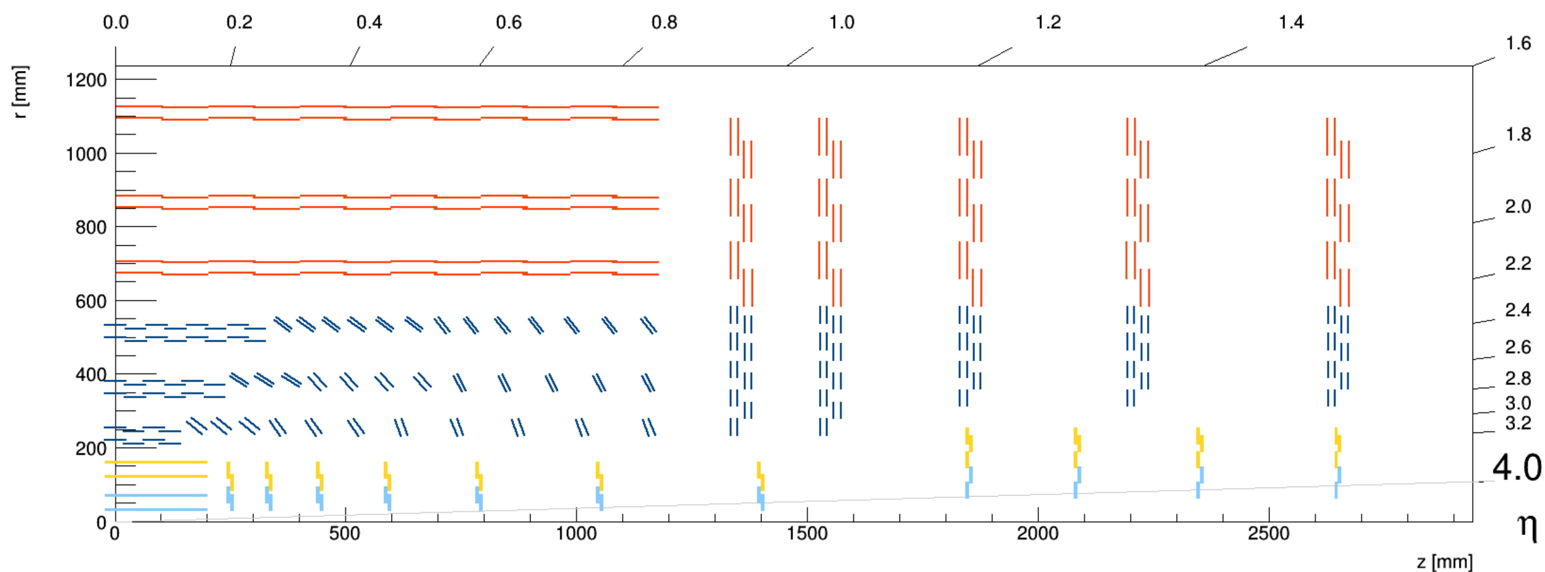
Operate efficiently in extremely harsh radiation environment

- new regime for Si sensors and readout chips, preserve the option to extract pixel detector and replace components

Pixel detector is inserted last, after beam pipe and outer tracker

- Constraints on mechanics

Phase 2 CMS Tracker Design

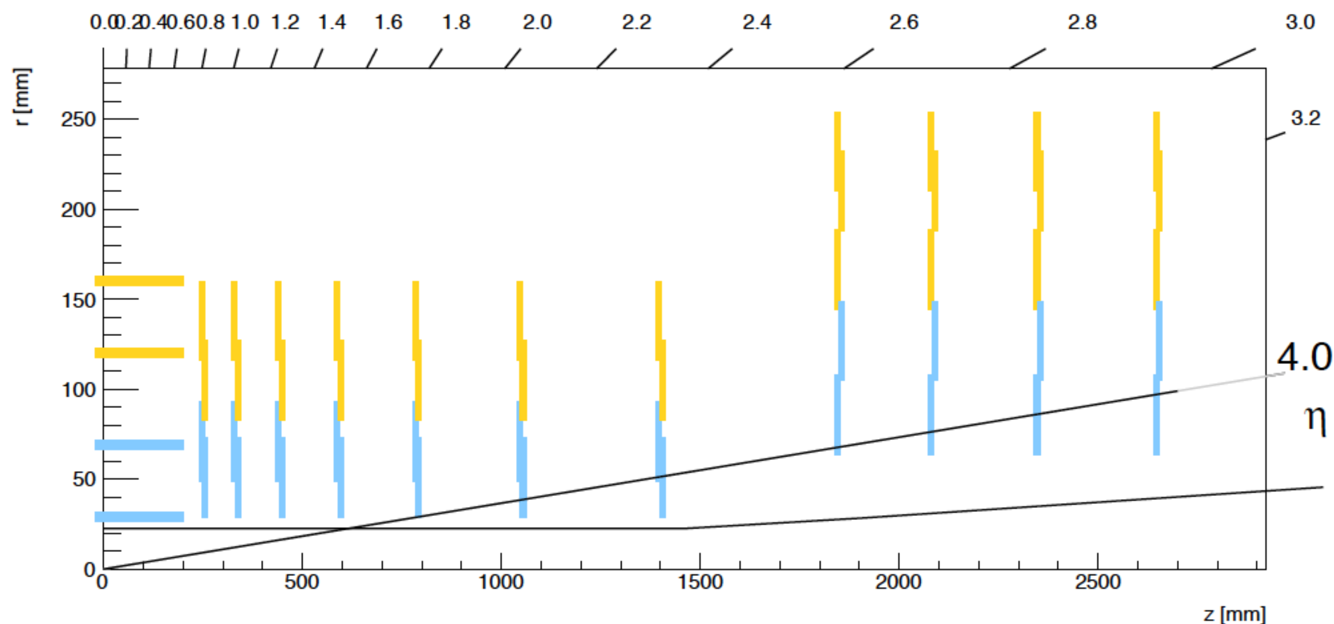


Pixel Detector:

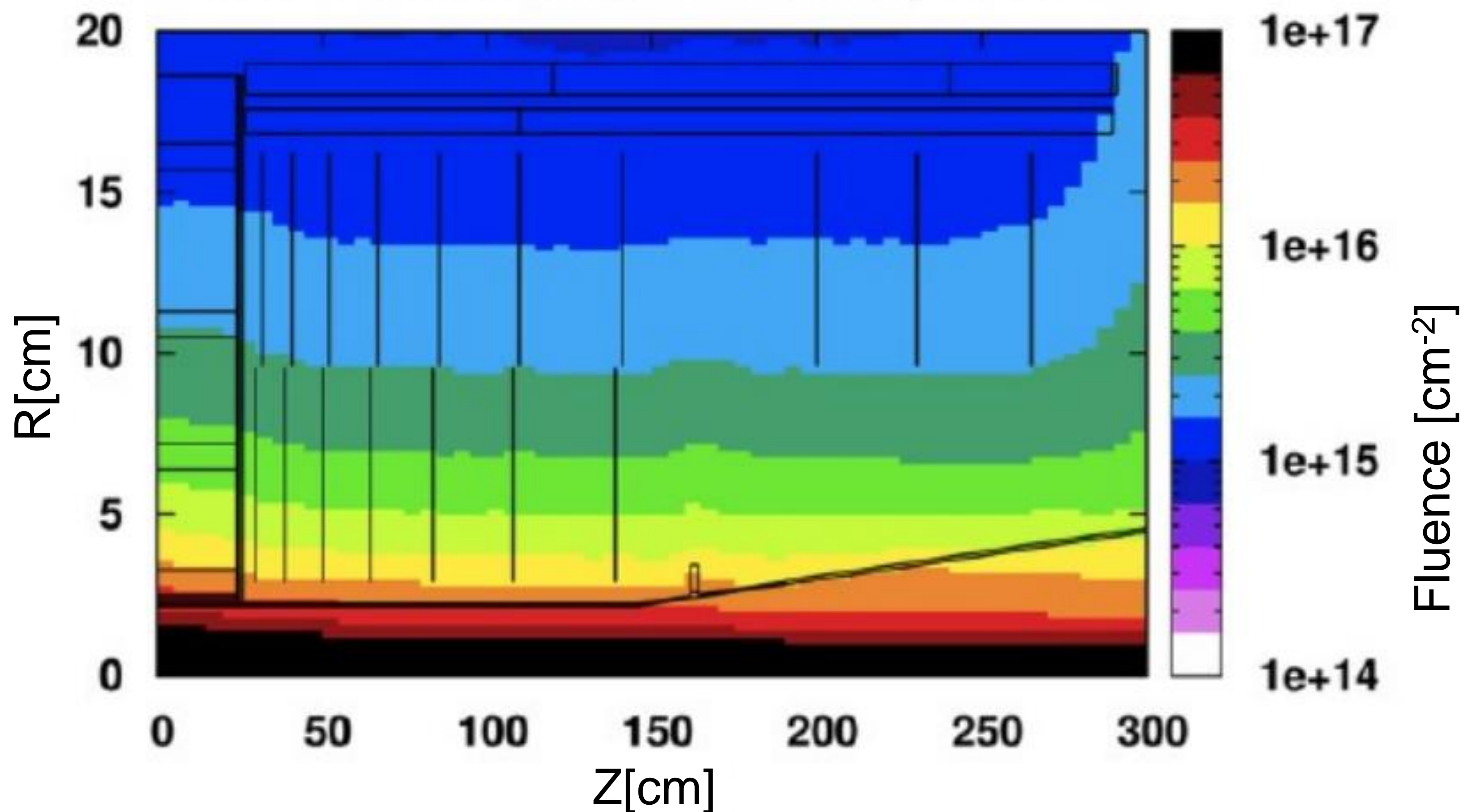
4 barrel layers a-la Phase 1
r_1=2.9 cm, r_4=16.0 cm

Increasing the number of discs(11+11) from (4+4)
z_1=±25 cm
z_{11}=±265 cm

Total: ~4.5 m^2 of Silicon!!



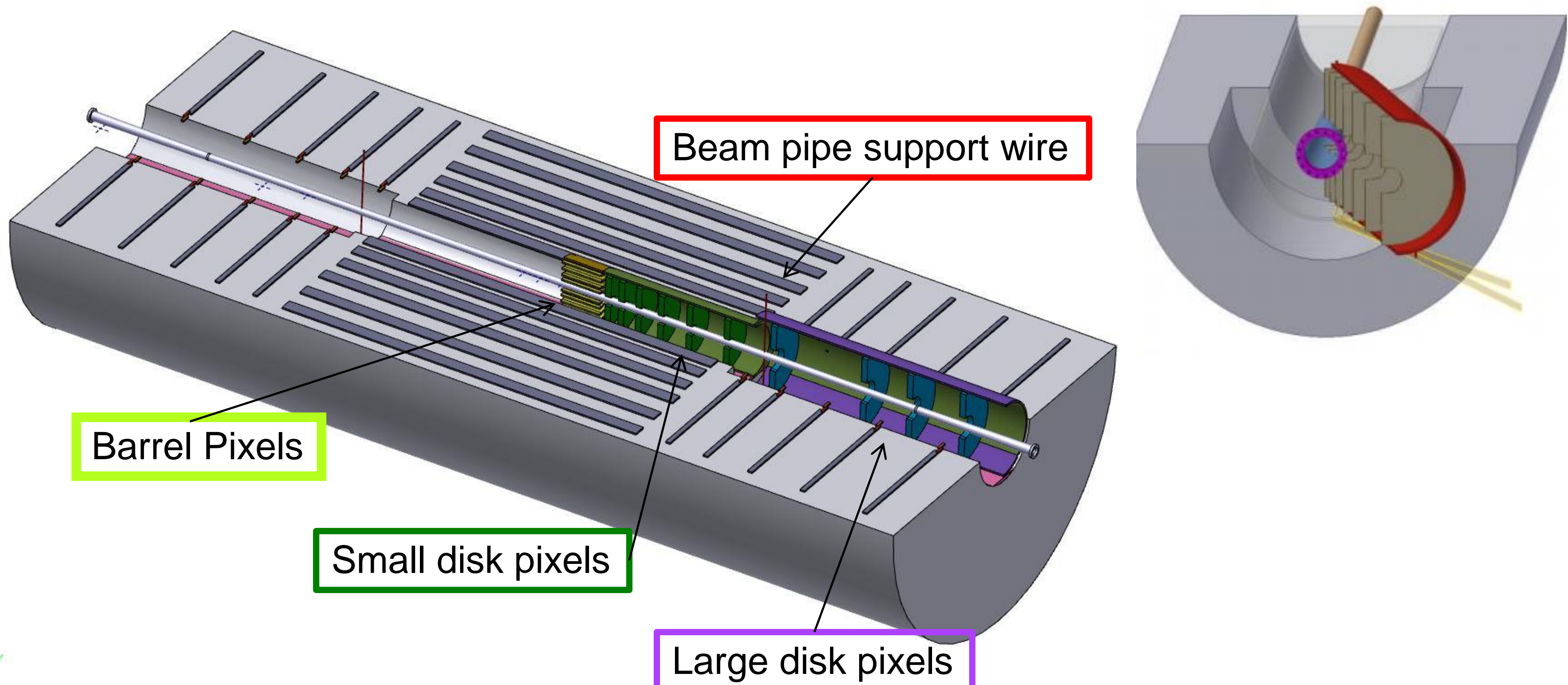
Pixel detector: Fluence



Layout considerations

Mechanics

Half-cylinders and a "step" to allow for installation after the beam pipe and outer tracker are in place:



Step in the pixel envelope (r=20 cm → r =30 cm at z=160 cm)

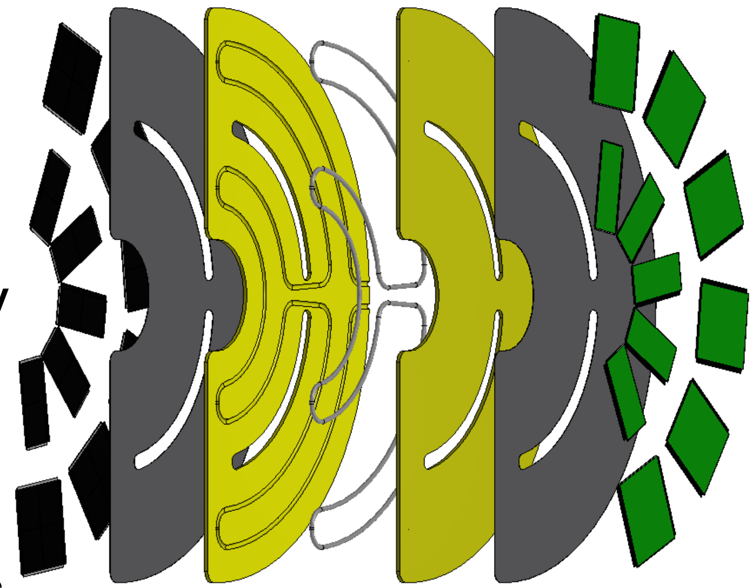
Installation of the barrel+small discs section using temporary rails that will be removed before large discs insertion

Mechanics

Cooling lines on the half cylinder to remove up to 220 Watts per disk.

Disks: simple layout, due to large number.
No turbine/blade design.

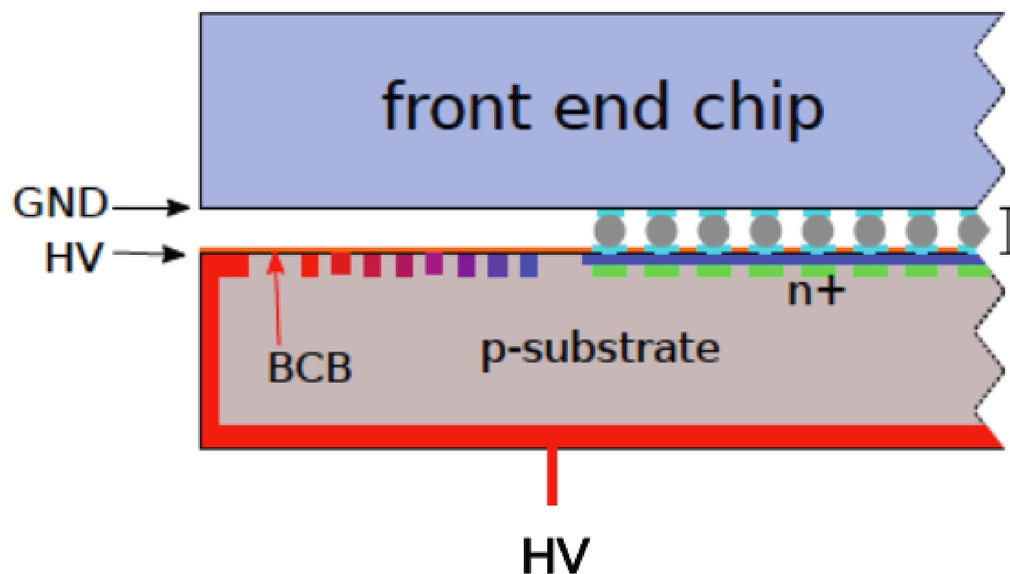
- CO_2 cooling tubes are embedded in thermally conductive foam with CF face sheets on either side (consider titanium pipes)
- Pixel half-disks are populated with sensor modules on both sides to create a hermetic layer.



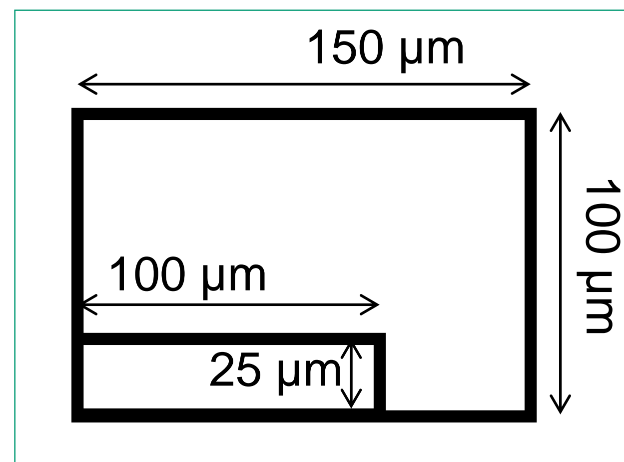
Granularity and radiation hardness of sensors

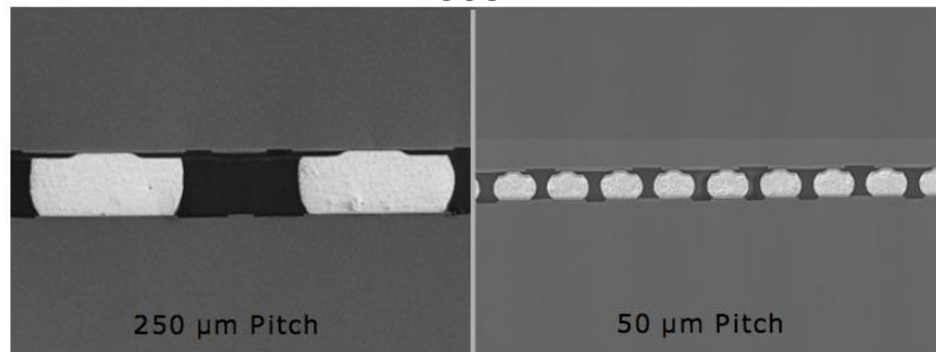
n-in-p, thin, small pitch pixels

Planar n-on-p pixel sensor (current detector: n-on-n)
–thin: <200 μm (current detector 285 μm)
–small pitch pixel cell (2500 μm^2 area) current detector 15000 μm^2 area
3D sensors an option for the layers most exposed to radiation damage



Phase II vs current and Phase I pixel size:





SEM pictures of bump-bonds for pixels with various pitches, from Phase 1 FPIX

Technical challenges:1

Fine pitch sensors:

- Pixel isolation: Not enough room for p-stop for each pixel
    - Alternative: common p-stop, p-spray
- Not enough space for conventional biasing scheme (needed for sensor tests)
    - Common punch through
    - Poly-silicon resistors
    - No biasing scheme
- Bias scheme at very high fluence

Thin sensors:

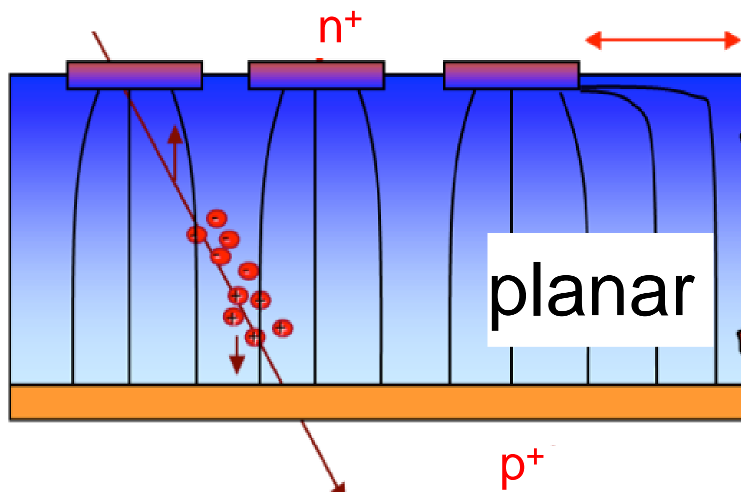
- Will we get bowing effects for <200 μm thick sensors (one sided process)? Handling during bump bonding challenging?

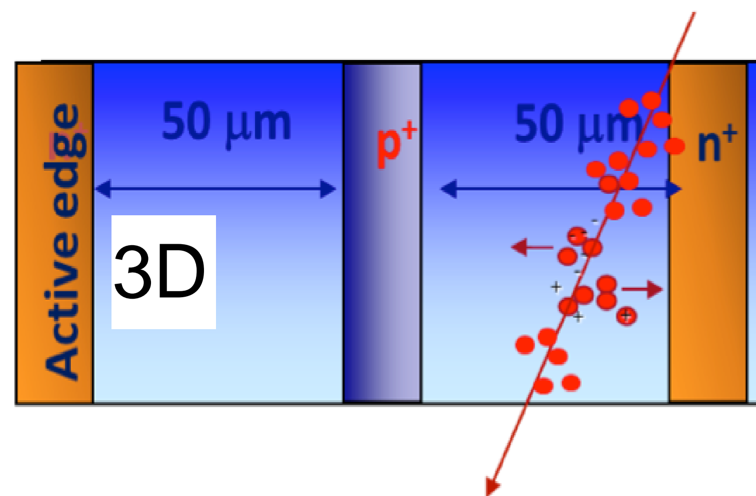
Sparking issues at outer edges, where HV sensor only 10s of microns from ROC at ground.

Technical challenges:2

Radiation hardness- we have not yet tested pixel sensors to 1-2E16 (problem: no radiation-hard ROCs available yet).
Alternative to planar n-in-p pixel sensors for the areas of highest exposure (Layer 1): 3D sensors

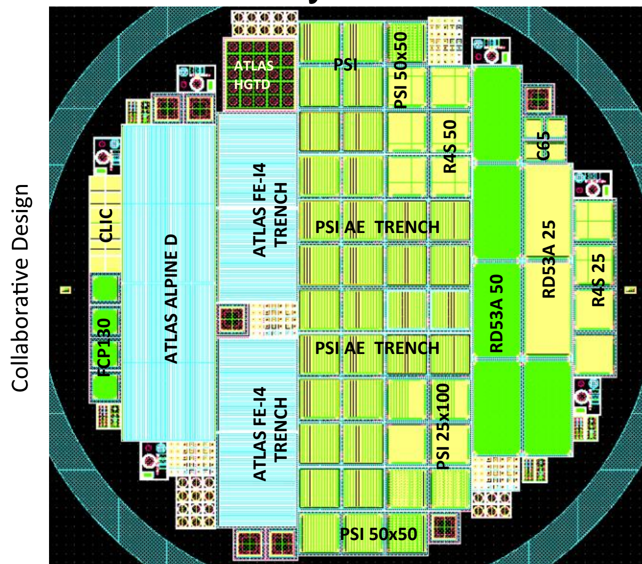
- Common advantage: short drift path, higher field at same V_{bias}
- 3D: thicker sensors possible, but higher cost, lower yield,..fabrication of small pixels has to be demonstrated
- Radiation hardness has to be demonstrated for both technologies.

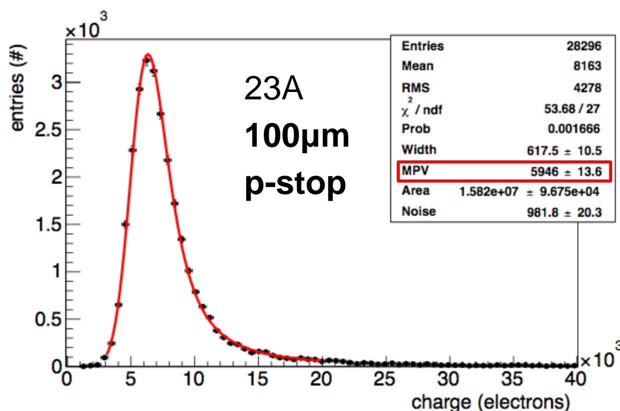




2 Planar Pixel R&D submissions

Common ATLAS and CMS pixel R&D at FBK Trento funded by INFN

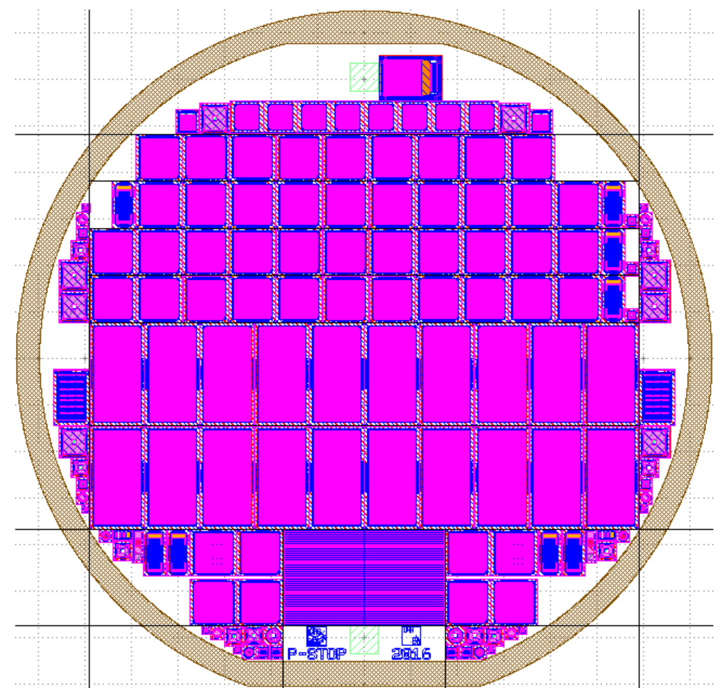




100µm and 130µm thickness, tested in lab+testbeam, irradiation and analysis ongoing
→Successful production of pixel sensor on 100 µm thin silicon!

Goal of both submissions is to test
thin sensors,
small pixels,
variations in bias schemes, and
pixel isolation
(and new ROCs)

HPK CMS Submission, led by University of Hamburg

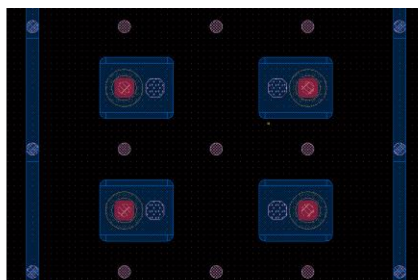


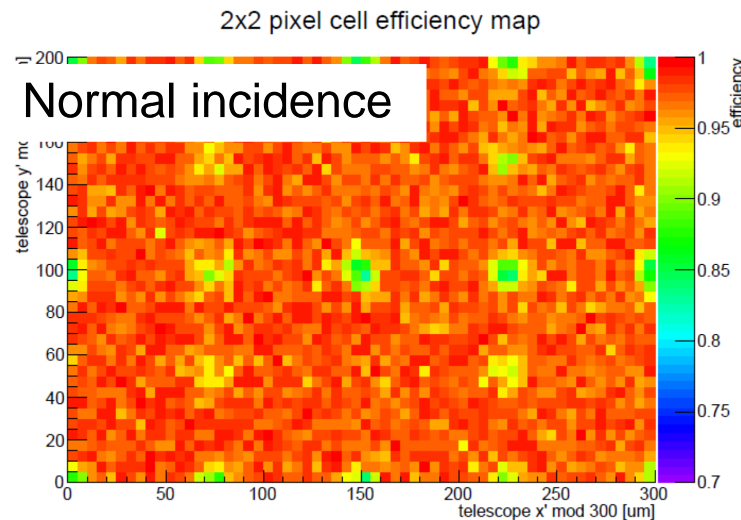
Design with HPK, wafers expected back early 2017

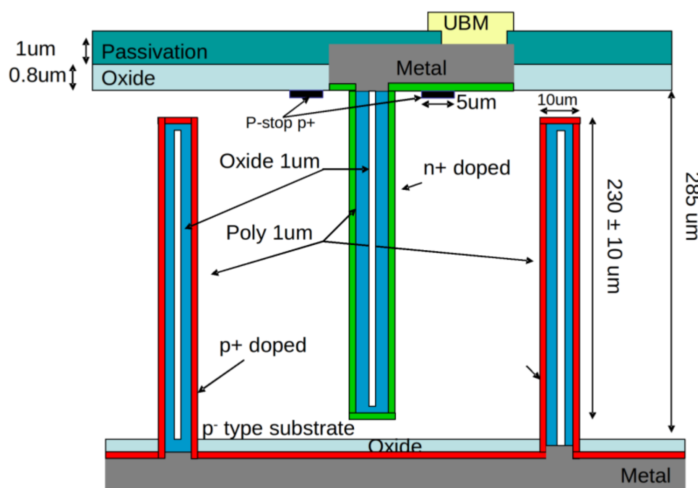
150 µm, no handle wafer
150 µm + 50 µm Si-Si direct bond
Deep diffused 150 µm + 50 µm
p-stop and p-spray isolation (only dir. bond)

3D Pixel R&D submissions

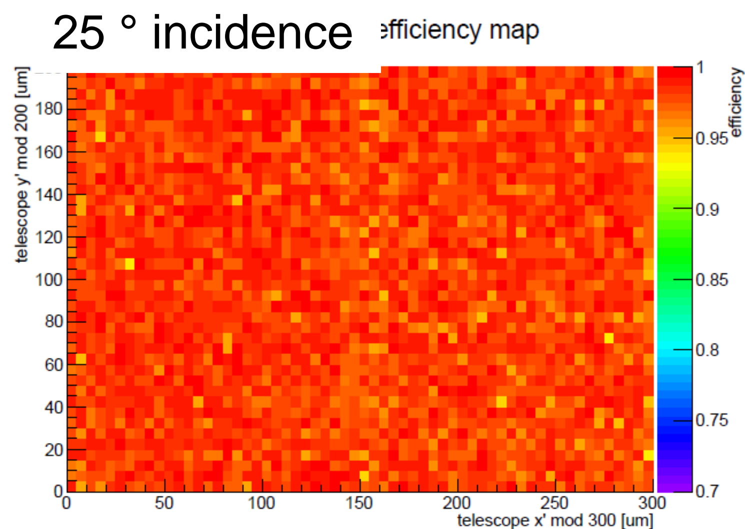
- 3D pixel sensors fabricated by CNM, Spain
- IBL run, read out with CMS PSI46dig ROC
- 100x150 μm²







Double sided 3D process yields good sensors with "standard" pixel size



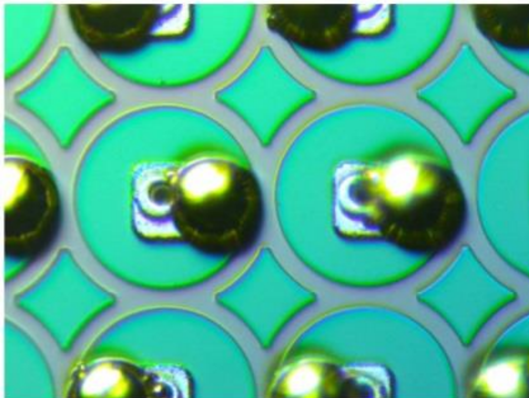
3D: Small Pitch Run at CNM

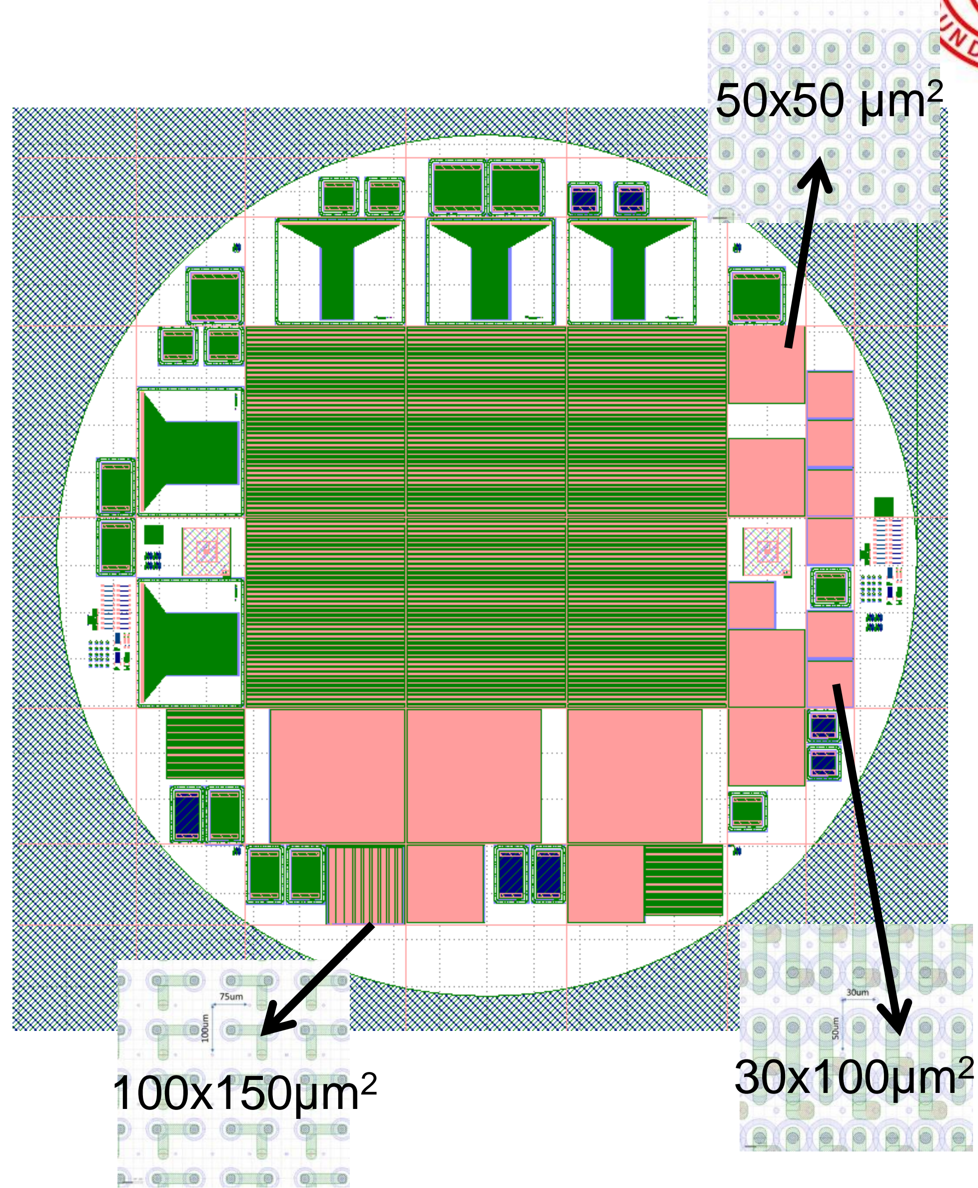
Joint RD50 project: ATLAS, CMS, LHCb

230 μm wafer, n-in-p, double sided

Aims:

- Test small pitches (25x100 and 50x50)
- **Aspect ratio: 8μm holes in 230μm (1:25)**
- 100μm and 200μm slim edges
- Radiation hardness of different layouts





Gomez, Vila

3D: Small Pitch Run at INFN (FBK)

3D sensors made with single sided DRIE (deep reactive ion etching) process at FBK Trento, Italy

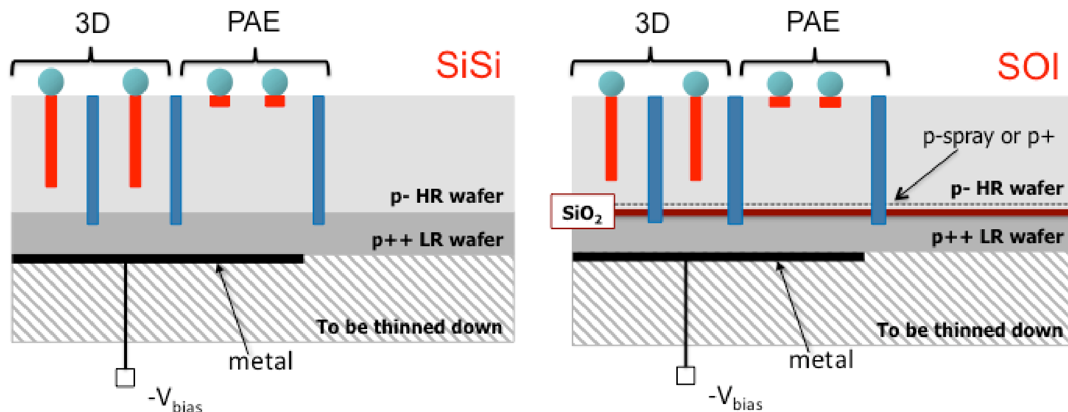
- Si-Si Direct Wafer Bond (DWB) **100um and 130µm active FZ**, 500µm handle CZ

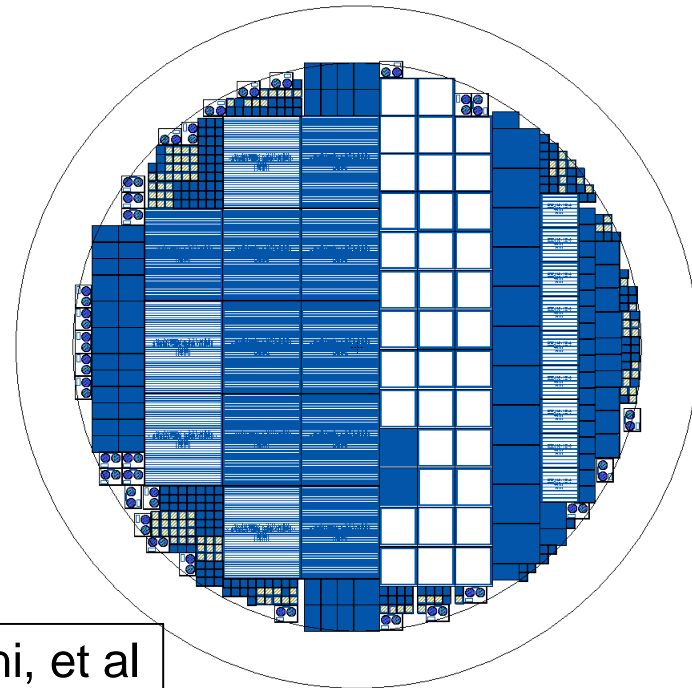
Trying "the technology limit" with many small pitch structures

Production completed, 3D wafer quality overall satisfactory

Bump bonding to FE-I4 and PSI46dig at Selex (Rome) in preparation

- Investigations of small pitch 3D pixels to come





M.Meschini, et al

Readout chip design: driving concepts

Compared to Phase 1, Phase 2 ROC has to cope with 5x hit rate, 10x higher trigger rate with longer latency, 10x radiation dose

- Rad hard chip w. low threshold

Small cells (2500 μm^2) in a large (4 cm^2) chip

- high density of transistors

Thin sensors giving small signals, especially after irradiation

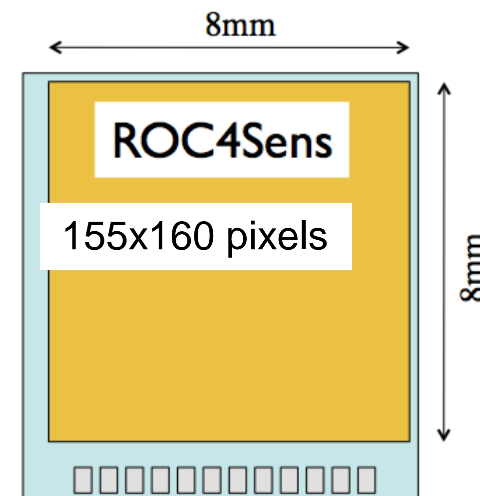
- low noise (<1200e)

Tight constraints due to CMS trigger and DAQ, e.g. deeper buffer to accommodate 12.5 μs latency, and faster readout to withstand 750 kHz L1A rate

65 nm CMOS chip being developed as part of joint CMS/ATLAS RD53 collaboration

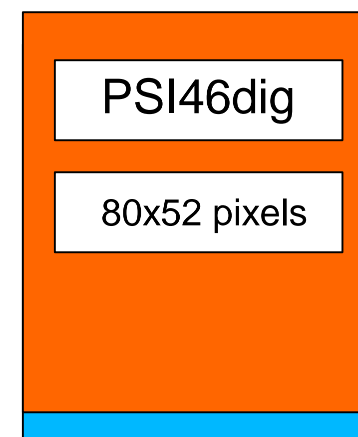
Test ROCs for R&D

Name	Pixel Size (μm^2)	Technology	Rad hard	Available ?
ROC4Sens	50x50	250 nm (IBM)	5 MGy	end-2016
FCP130	30x100	130 nm (GF)	5 MGy	end-2016
RD53A	50x50	65 nm	Up to 10 MGy	mid-2017?



“Fallback”:

Name	Pixel Size (μm^2)	Technology	Rad hard	Available?
PSI46dig	100x150	250 nm (IBM)	1.1 MGy	In hand



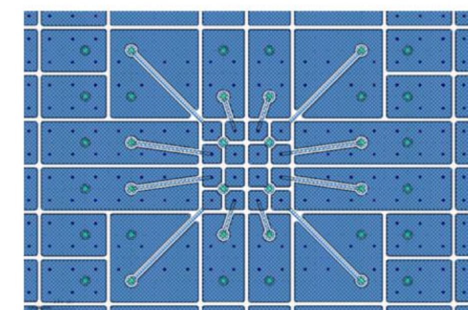
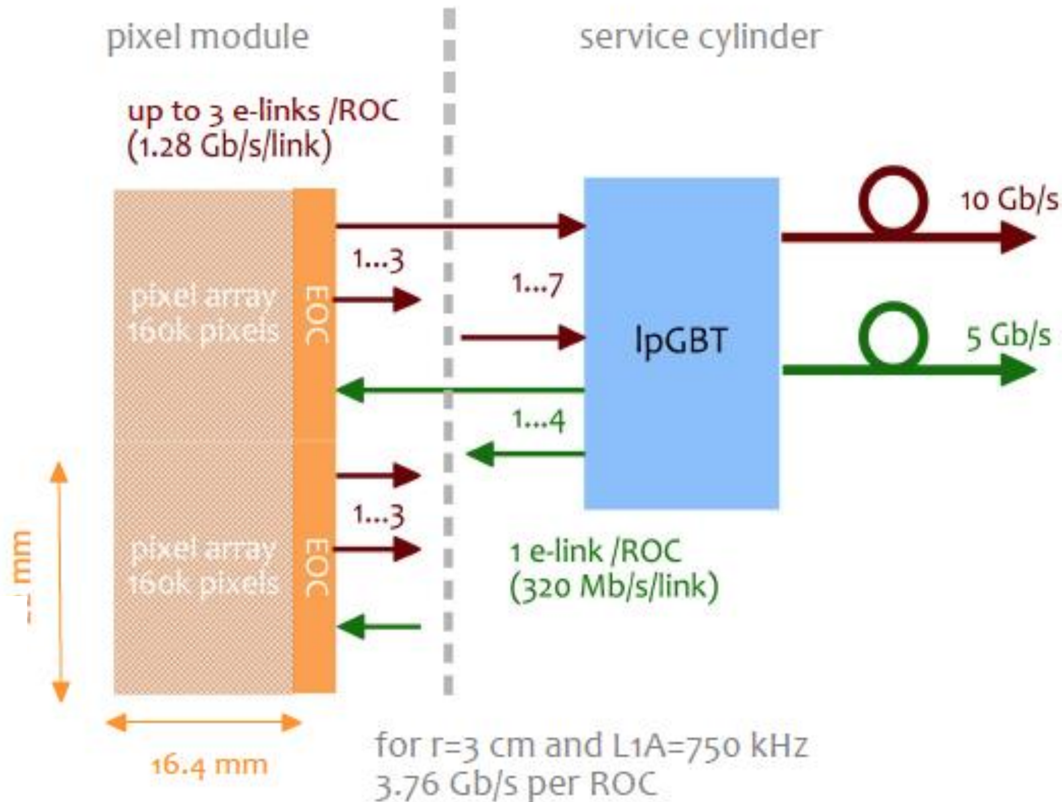


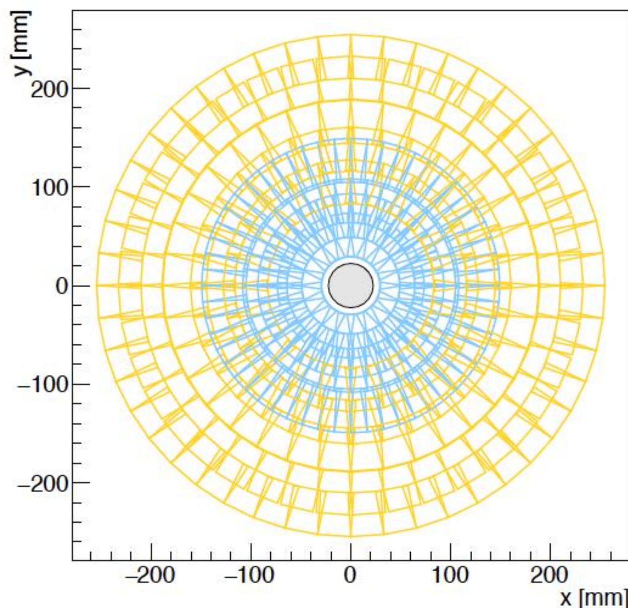
Fig. 8. Layout of 50 μm × 50 μm pixel cells surrounded by larger cells to be compatible with the PSI46dig readout chip.

Pixel Modules and readout

No opto-electronic device able to withstand the radiation environment of the inner layers.

Solution: “remote” lpGBT placed on the pixel service cylinder and connected to the module (readout and control signals) via e-links cables





A module is defined by matching input specs of lpGBT with the output rate of the ROCs.

Minimal number of module types e.g. 2x1 or 2x2 ROCs/module with typical size of a ROC 2x2 cm^2.

Possibly small/large pixels in different layers/discs.

E.Migliore

Pixel Phase II Powering Baseline

Required power: ~20 kW for 4.5m^2

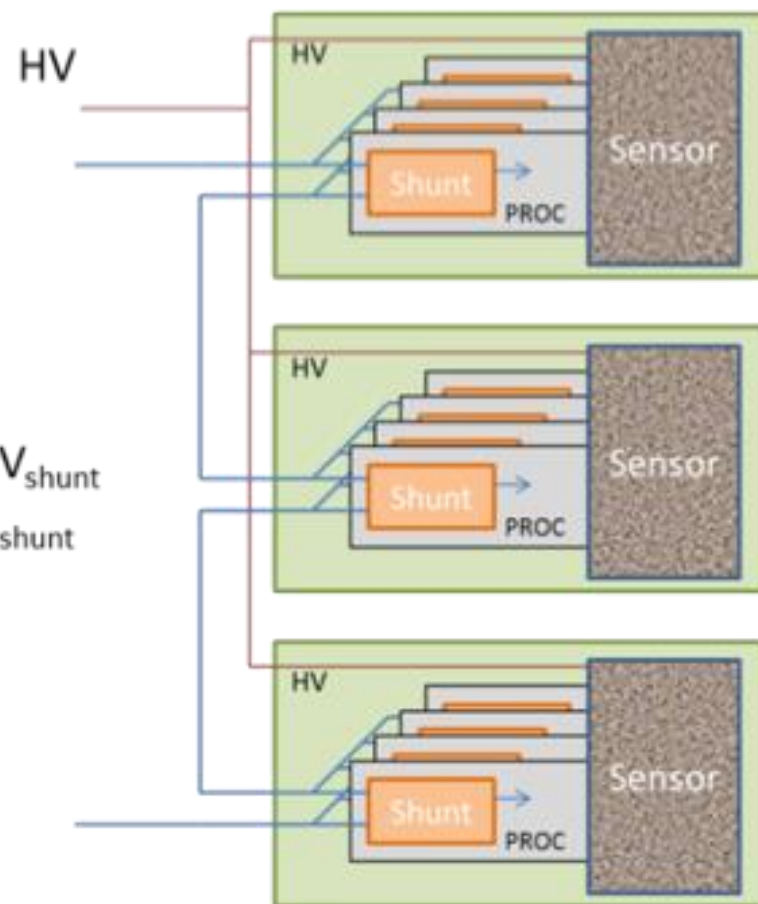
Traditional powering schemes (phase-0: direct from PS, phase-I: DC-DC converter) cannot be used due to material and space issues and radiation → investigate serial powering across modules

Serial powering: current driven and intrinsically low mass; not very efficient and failure modes needs to be carefully evaluated

Start with setup based on ATLAS FEI4 to gain experience on system test

Shunt-LDO circuit is Integrated in the ROC itself

- Developed for FEI4 chip family, being ported in RD53
- provides regulated voltage, shunts the current not taken by load



E.Migliore

HL-LHC

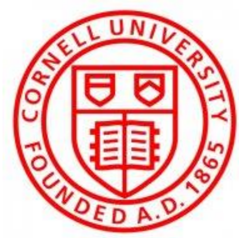
Summary

- HL-LHC poses high demands on pixel detector
  - Radiation hardness →thin sensors with radiation hard design
  - Efficient and precise tracking at high rates →small pixel pitches
  - Radiation tolerant, fine pitch, low noise readout chips→RD53
  - Fast links
- R&D programs to develop thin, fine pitch sensors and address pixel design issues
  - Planar: HPK submission, INFN/FBK (together with ATLAS),
  - 3D: INFN/FBK (together with ATLAS), CNM
- Fine pitch bump bonding challenging and a major cost driver
- Mechanics and services non-trivial- many more forward disks
- TDR due next year!

Resources, Thank you!

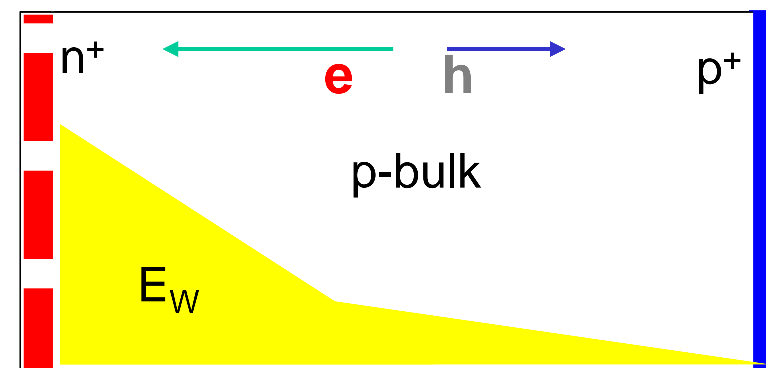
- Georg Steinbrueck
- Marco Meschini et al
- Gervasio Gomez, Ivan Vila
- Joe Conway, Charlie Strohman

Backup Material



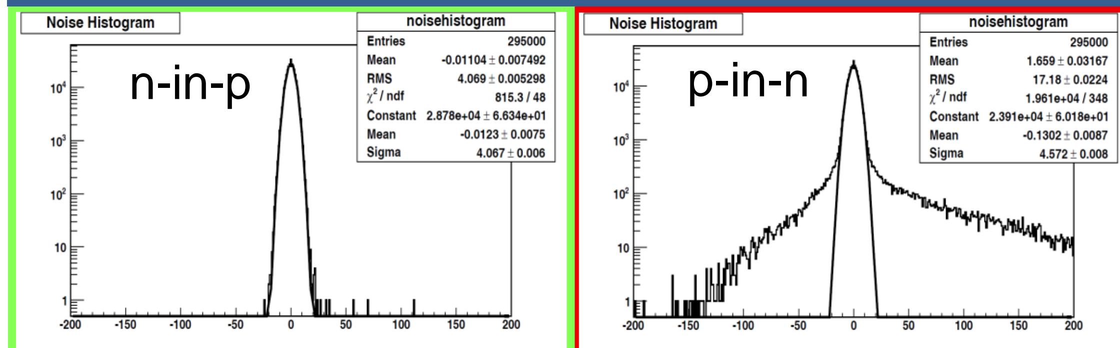
n-in-p versus n-in-n

- n-in-p single sided process
  - More vendors, cost effective
- Thin sensors: especially costly for double sided n-in-n
- n-side readout preferred
  - Electrons: Higher mobility than holes, higher lifetime → Advantage to collect electrons at high weighting field (E_W)
  - Excess noise observed in p-in-n strip sensors for Φ>1E15 cm^{-2}
  - T-CAD simulations confirm that p-in-n sensors have the tendency to exhibit high electric fields at the strips due to positive oxide charges (likely curable by careful design)



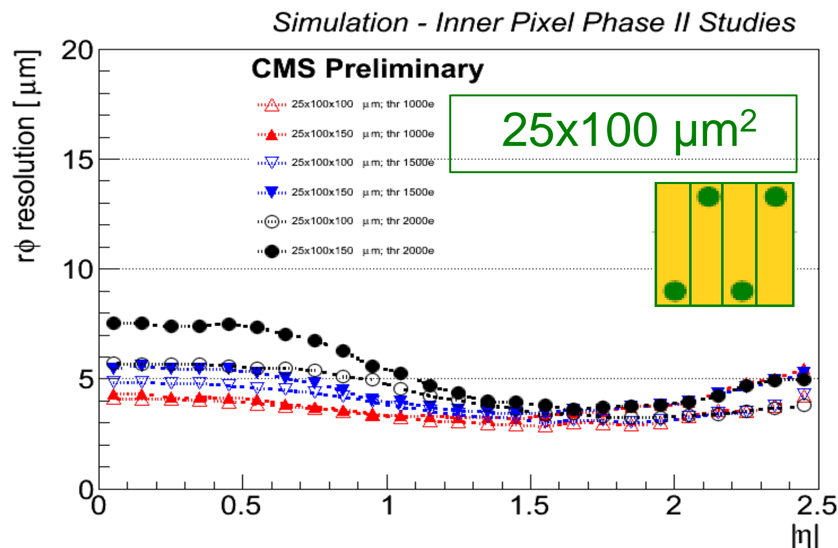
Charge collection: Illustration

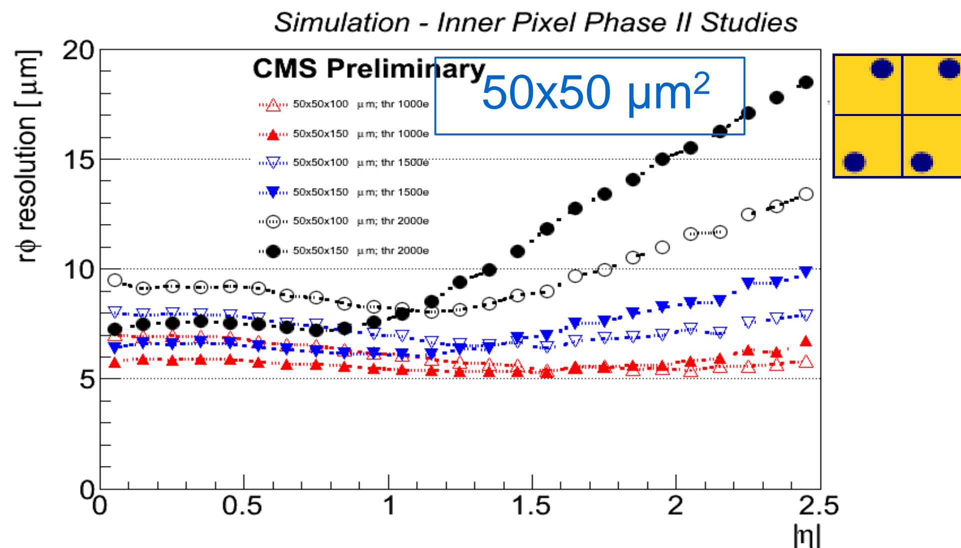
Noise histograms in 80 μm pitch strip sensor



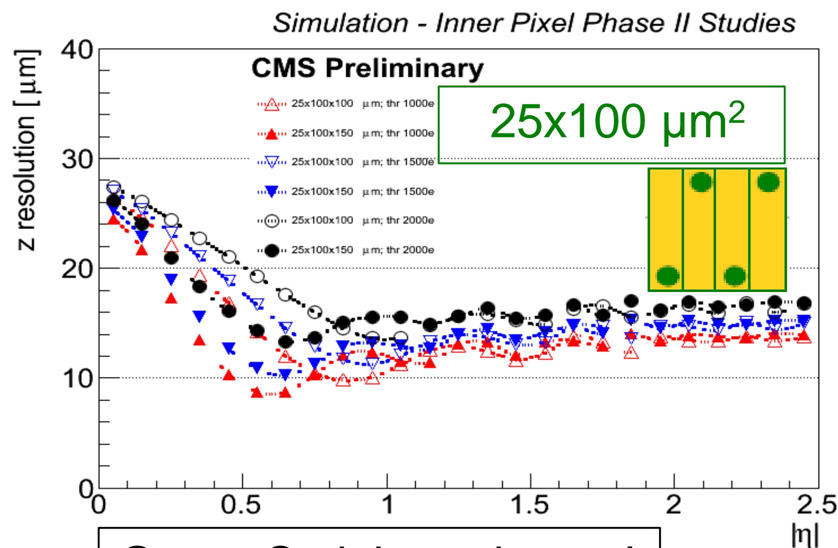
Georg Steinbrueck, et al

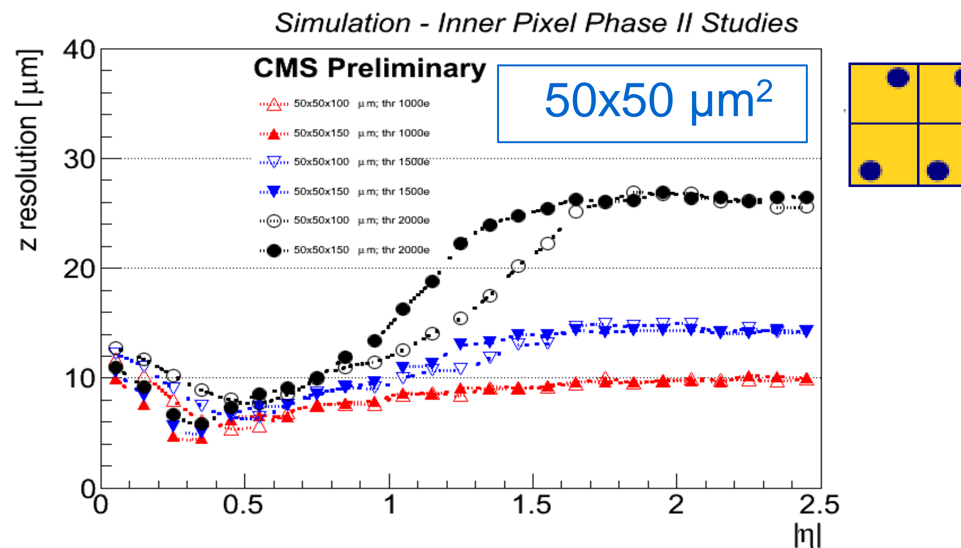
Pixel size





thickness open=100 μm/full=150 μm threshold 1000e/1500e/2000e





Georg Steinbrueck, et al

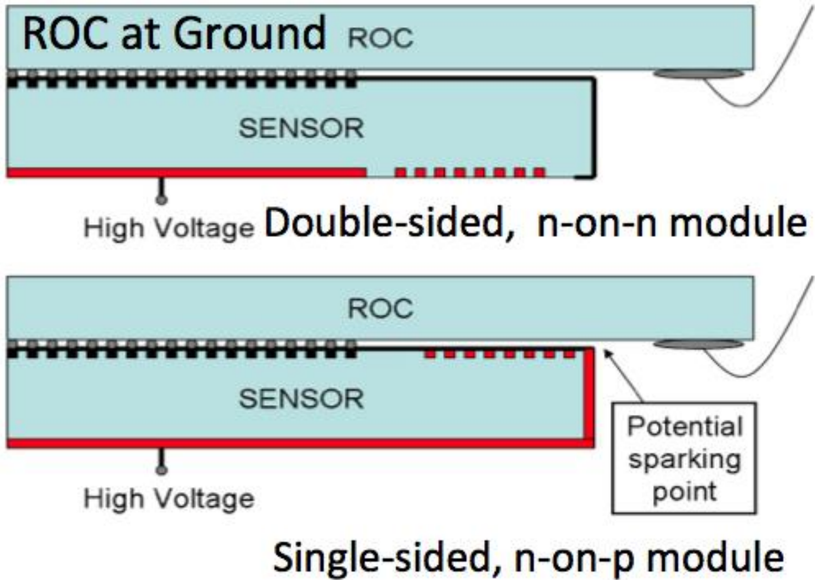
Sparking

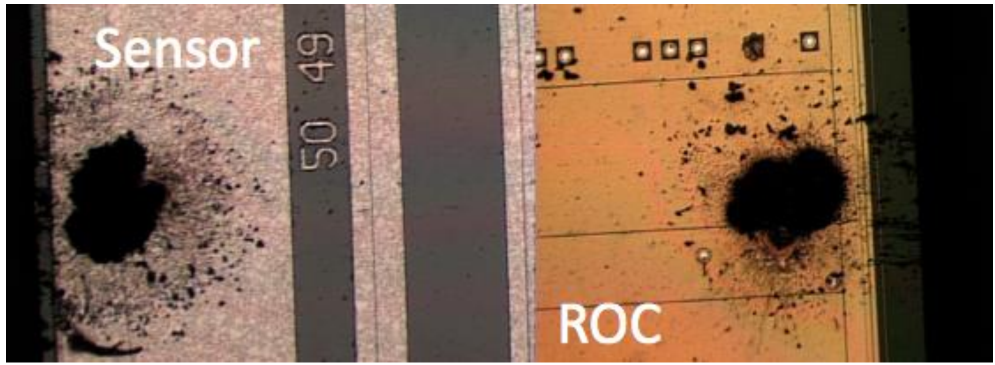
Planar n-in-p sensors

- CMS R&D sensor submission underway to determine rad hardness, optimal design
- Plus: low cost, good reliability. Minus: sparking problem, warping?

Planar n-in-n sensors

- Same (double-sided) technology as used in CMS phase 0 and 1, but need to thin.
- Higher cost, fewer vendors.





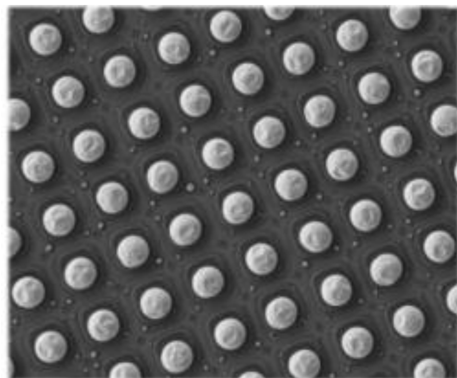
Bump bonding

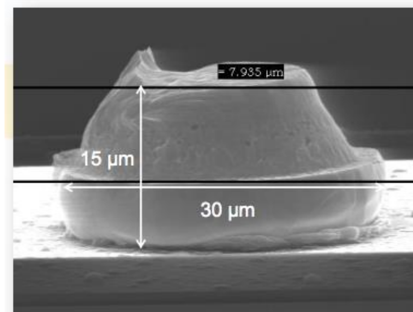
Bump-Bonding (interconnection of sensors and ROC):

Standard industry processes include under-bump metallization, deposition of solder balls, indium bumps, or similar, then flip-chip assembly

Special considerations for HL-LHC pixel sensors:

- Thinner sensors (150 μm) challenging to handle.
- Small feature size (depending on design, e.g. 10 μm^2 passivation opening).
- employ sparking protection, e.g. higher bump-bonds, underfill with high di-electric strength, parylene coating of modules, and investigate radiation hardness of spark protectant





SEM picture of gold stud bump
(with gold wire of Ø = 15 µm)