ATLAS Track-Trigger information

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ON BEHALF OF ATLAS
Introduction

The increase in luminosity during the HL-LHC phase will come at the price of a much higher pileup
- The pileup level is expected to jump from 40 to 140-200 collisions per bunch crossing
- ATLAS was designed for a pileup of 20 collisions per bunch crossing, big improvements are required

The relevance of the tracker information will grow dramatically
- Tracks based corrections will be fundamental in many areas, as MET and jet measurements
- Tracker quality will be challenged by the density of the particles within the events

The use of tracks can be a crucial tool to improve trigger selections and effectively control rates
- Large data reduction in the data acquisition system is in fact required
- Need to keep thresholds in many selections at the same level of Run II, despite the much larger pileup
  - Increasing the thresholds will help curbing the rates, at the price of efficiency lose in many decay modes (e.g. Higgs related measurements)
  - Inner tracker based confirmation and isolation will be fundamental for many single lepton selections
- Extremely challenging task due to the number of channels involved and the short latency
ATLAS Inner Detector Upgrade

The ATLAS inner detector will be completely redesigned in Phase II

- The current Pixel+Strips+TRT tracking volume will be replaced by all silicon tracker
- The detector will have 5 pixel layers and 4 pair of strip layers
  - An average of 13 measures in the barrel
- Total coverage and final details on the layout still under discussion
  - Coverage up to $\eta=4$ favored

New Tracker (ITk) designed to sustain the total dose expected during the HL-LHC period

- Performance are expected to be at the level of Run-I or Run-II, despite the extremely larger pileup
- Allowing to maintain high efficiency on all the relevant channels
Trigger architecture during HL-LHC

Scoping document TDAQ architecture during Phase II will have 2 fast hardware steps

- **Level-0** will have a maximum output rate at 1 MHz, using information from calorimeter and moon systems
  - Extremely reduced latency budget: ~10 µs
- **Level-1** can add the ITk information, maximum output rate 400 KHz
  - Latency budget for full decision ~60 µs

Further data reduction in the **Event Filter**

- Maximum expected output rate 10 KHz

The architecture expects **2 track finding systems** that should add computing power for real time tracking

- **L1Track**, able to perform regional tracking at 1 MHz
- **FTK++**, able to perform full event tracking at ~100 KHz

In case a single HW level architecture regional hardware tracking still required for fast event rejection
Prequel: ATLAS Fast TracKer

FTK is designed as coprocessor dedicated to track reconstruction at high rate and short latency

- It is able to provide **full track reconstruction at 100 KHz** with an average latency ~**100 µs**
  - Efficiency around 93% for all tracks above 1 GeV, |η|<2.5
  - Computational load subdivided in towers able to work in parallel, designed around Associative Memory (AM) chips and FPGAs
  - Custom boards using VME and ATCA standards

Track reconstruction implemented in a pipelined algorithm

- AM chips can perform pattern matching the ID data to a dictionary of pre-calculated patterns: **8192 chips**, storing **1 billion** patterns
  - Pattern recognition uses 8 silicon layer (3 pixel + 5 strips)
  - Linearized track fitting performed in 2 consecutive stages
    - 1st fit based on 8 layers, final fit uses 12 layers (4 pixel + 8 strips)

Commissioning ongoing: **first tracks expected within 2016, first full detector coverage in 2017**
FTK performance plots

![Efficiency vs. $p_T$](image1)

![Number of FTK Vertices](image2)

![Fake rate](image3)

![Normalized Entries](image4)
Pattern recognition using AM chips

The AM chip is a custom VLSI chip able to store sequences of numbers, “super-strips” (SS)
- SS represents a cluster position in a given detector element
- A sequence SSs, the pattern, represents a course resolution trajectory for a track

Match between the incoming data and the patterns is performed while data are loaded
- The list of matching “roads” is returned when the comparison ends
  - The combinatorics problem is automatically solved by the chip
- Further computing focuses only on the hits belonging to roads
  - Track fitting performed using FPGAs

Important to have chips able to store larger pattern bank and fast links
- Larger bank size allows better selections
- AM chip variable matching precision allows effective pattern bank compression

\[ p_i = \sum_j C_{ij} \cdot x_j + q_i \]
ATLAS L1 Track Processor

Use of tracks during the Level-1 decision should allow to keep thresholds reasonably low
- Single muon and electron selection should allow $p_T > 20$ GeV
- Double-lepton selections at $p_T > 10$ GeV
- Low $E_T$ threshold should also be available for multi-jet (e.g. 4 jet trigger)

To achieve these goals ATLAS L1Track performance should be:
- Reconstruct tracks with $p_T$ above 4 GeV within the RoI
- Efficiency above 90% and resolution similar to offline tracking
- Allow 5x rejection power for single leptons, with $z_0$ of a few mm resolution to reject objects from multiple interactions

L1Track design in ATLAS exploits AM for pattern recognition (like FTK)
- Track parameters extracted using a linearized algorithm implemented in FPGAs
- Performance, in particular latency, requires more advanced solutions and components

ECFA 2016 - Aix-Les-Bains 06/10/2016

CERN-LHCC-2012-022
L1Track expected performance

Different configuration of layers and SS sizes have been tested
◦ Possible to achieve the efficiency goal (~99%) with limited latency (few µs)

Using strip-only or strip+1 pixel configuration both satisfy the main criteria
◦ Number of patterns required about 1 billion
◦ Number of fired roads and fits within the given latency
◦ 8 layers pattern matching with a single linearized fit step

Both solution fulfill the efficiency and resolution requirements
◦ Using the outermost pixel layer improves track parameter resolutions, particularly $z_0$

<table>
<thead>
<tr>
<th>Detector layers</th>
<th>single muon</th>
<th>min. bias</th>
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<tbody>
<tr>
<td></td>
<td>$\varepsilon_{\text{pattern}}$</td>
<td>$\varepsilon_{\text{fit}}$</td>
</tr>
<tr>
<td>Strip layers only</td>
<td>99.4%</td>
<td>99.5%</td>
</tr>
<tr>
<td>Strip + 1 pixel layer</td>
<td>99.5%</td>
<td>99.7%</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Detector layers</th>
<th>$q/p_T$ [e/GeV]</th>
<th>$\phi$ [rad]</th>
<th>$\eta$</th>
<th>$d_0$ [mm]</th>
<th>$z_0$ [mm]</th>
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</thead>
<tbody>
<tr>
<td>Strip layers only</td>
<td>0.003</td>
<td>0.001</td>
<td>0.002</td>
<td>0.3</td>
<td>1.7</td>
</tr>
<tr>
<td>Strip + 1 pixel layer</td>
<td>0.003</td>
<td>0.001</td>
<td>0.001</td>
<td>0.2</td>
<td>0.3</td>
</tr>
</tbody>
</table>
Level 1 Track Latency study

Study on the latency has been performed to verify the possibility to read all data from the detector

- Available budget to retrieve data is estimated as 6 μs
- Track reconstruction estimated to be a few μs

Emulations have been performed to verify the latency required to read 99% of data from the ABC130 chips

The Regional Read-out Request (R3) mechanism implemented in the ABC130 allows to ship data to the processor with the required time

L1Track requests have priority over the normal data requests

- This will allow the L1Track system to avoid truncation

w/ R3 prioritization
Impact on the trigger

Test on single muon and electron trigger performed

- Using strips only configuration, similar results are expected from the alternatives
- Simulation studies on a trigger tower seeded by a Level-0 object

Trigger selection performed using pileup 200 samples

- Goal is to have a 5x reduction on minimum bias while retaining >90% efficiency on the object
- Different matching schemes have been tested

Goal can be achieved by the current track trigger architecture
FTK++ processor

FTK++ will work within the HLT network

- AM+FPGA processor technology guarantees extremely fast track reconstruction
- Full tracking at O(100) KHz for all tracks with $p_T>1$ GeV
- Large synergy with L1Track will guarantee reliability and cost optimization
- Number of patterns for the system ~8 billion, because of lower $p_T$ threshold (1 GeV)

The availability of resources explicitly devoted to tracking can bring a significant output in term of physics outcome of the experiment

Further studies on all approaches will be performed during the next years to perform the optimal technological choice
Associative Memory chip evolution

The **AM06 chips** is the key component for FTK and any similar future tracking processor:
- Uses **65 nm** TSMC technology, able to store **128k patterns** per chip
- Power consumption about **2.5 W per chip**, working at ~1.1 V
- Data through a 2 GB/s serial link, internal clock 100 MHz
- Next production batch arriving in January, currently produced about 1000

Phase-II processor will use **AM2020**
- Based on **28 nm** technology, reaching **512k pattern/chip**
- Internal clock will raise to **200 or 500 MHz**
- I/O speed can be increased having **multiple 2 GB/s input lines**
  - Each I/O line at 16 bit with 500 MHz is 4 GB/s: e.g. 8 input lines mean 64 GB/s

First 28 nm cell prototype ongoing on **AM07**
- New CAM architecture has been tested, close to the goal of power consumption per comparison
- Cells size is in line with the expected increase in the number of patterns, optimization of the power ongoing
- More prototyping will be performed during 2017
Track trigger processor boards evolution

Very preliminary idea on the possible HW for the future track trigger processors

With respect to the FTK structure a more streamlined system can be built

- A single mainboard, based on ATCA standard
- Based on the FTK Data Formatter board design, PulsarII
- Computation done in the daughter cards

A large mezzanine can perform both pattern matching and track fitting

- Balancing among AM and FPGA will be validated during the coming years
- With respect the FTK AMB a smaller number of chips per board is expected
- It will allow to reduce cooling and power distribution problems
Conclusions

To fully exploit the HL-LHC capabilities ATLAS is planning improvements in the tracking system

- A new all-silicon tracker will offer improved tracking capabilities, allowing to resolve the enormous particle density expected in the events

More use of tracks during at all stages of the analysis will allow to maintain sensitivity to many physics channels at the level on Run-I/II

- Use of tracks during the trigger decision requires enormous computing power
- Use of dedicated hardware can allow to fill the gap, allowing also to tailor the performance around the trigger requirements

Providing tracking info at Level-1 is particularly challenging given the high rate and limited latency

- Current studies show how a processor based on AM chips and FPGA will be able to achieve the goal
- Regional tracking with 99% efficiency for tracks above 4 GeV is expected to allow 5x rate reduction on single leptons

Dedicated HLT processor will allow to implement selection closer to offline analysis

- Possibility to use custom hardware is also

FTK run will provide important information on the technology

Studies on future AM chips compatible with L1Track and FTK++ requirements is ongoing
Backup
| Item          | Offline $p_T$ Threshold [GeV] | Offline $||$ | L0 Rate [kHz] | L1 Rate [kHz] | EF Rate [kHz] |
|--------------|-------------------------------|-------------|---------------|---------------|---------------|
| isolated Single $e$ | 22              | $< 2.5$    | 200           | 40            | 2.20          |
| forward $e$  | 35              | $2.4 - 4.0$ | 40            | 8             | 0.23          |
| single $\gamma$ | 120             | $< 2.4$    | 66            | 33            | 0.27          |
| single $\mu$ | 20              | $< 2.4$    | 40            | 40            | 2.20          |
| di-$\gamma$ | 25              | $< 2.4$    | 8             | 4             | 0.18          |
| di-$e$       | 15              | $< 2.5$    | 90            | 10            | 0.08          |
| di-$\mu$     | 11              | $< 2.4$    | 20            | 20            | 0.25          |
| $e - \mu$    | 15              | $< 2.4$    | 65            | 10            | 0.08          |
| single $\tau$ | 150             | $< 2.5$    | 20            | 10            | 0.13          |
| di-$\tau$       | 40,30          | $< 2.5$    | 200           | 30            | 0.08          |
| single jet    | 180             | $< 3.2$    | 60            | 30            | 0.60*         |
| fat jet       | 375             | $< 3.2$    | 35            | 20            | 0.35*         |
| four-jet      | 75              | $< 3.2$    | 50            | 25            | 0.50*         |
| $H_T$         | 500             | $< 3.2$    | 60            | 30            | 0.60*         |
| $E_{T}^{\text{miss}}$ | 200             | $< 4.9$    | 50            | 25            | 0.50*         |
| jet + $E_{T}^{\text{miss}}$ | 140,125       | $< 4.9$    | 60            | 30            | 0.30*         |
| forward jet** | 180             | 3.2 - 4.9  | 30            | 15            | 0.30*         |
| Total         |                  |            | $\sim 1000$  | $\sim 400$   | $\sim 10$    |
AM based system challenges

Various constraints need to be met:
- Good efficiency, to avoid drop interesting information
- Satisfy the limit in the data transmission and computational load among different components
  - The number of hits that can be processed, the combinations that can be considered are limited

Finding an optimal working point is difficult:
- Many parameters, with not linear relations
- Algorithms need to remain simple (computing complexity is limited)
- Better version of existing algorithms can be necessary

Two main ingredients to allow the current system:
- Variable resolution feature in the pattern matching, using a “don’t care feature“ in the new AM chip (later)
- Two stage fitting scheme to obtain a better balance between the computing elements
AM optimization and DC bits

Exploring the use of AM chips various aspects need to be taken into account
- Number and position of the layers used during the pattern recognition stage
- Precision of patterns during the pattern matching

Pattern matching resolution is the most crucial
- Low resolution patterns allow smaller pattern bank size (less chips, less cost), but the probability of random coincidences grows
- High resolution increases the filtering power at the price of a much larger banks

The use of DC solves the problem of balancing the match precision
- DC allows to merge similar patterns in favored configurations (less patterns) maintaining high-resolution and rejection power where convenient
- The feature has been included in the newer version of the AM chips

Pattern in AM chip w/o the DC
3 low-resolution patterns
7 high-resolution patterns
Empty areas are a source of fakes

Pattern in AM chip w/ the DC
DC set

A. Annovi et al. http://dx.doi.org/10.1109/ANIMMA.2011.6172856
FTK Algorithms pipeline

FTK has a custom clustering algorithm, running on FPGAs.

Data are geometrically distributed to the processing units and compared to existing track patterns.

Pattern matching limited to 8 layers: 3 pixels + 5 SCTs. Hits compared at reduced resolution.

FTK has a custom clustering algorithm, running on FPGAs. Data are geometrically distributed to the processing units and compared to existing track patterns. Pattern matching limited to 8 layers: 3 pixels + 5 SCTs. Hits compared at reduced resolution.

Full hit precision restored in good roads. Fits reduced to scalar products.

Good 8-layer tracks are extrapolated to additional layers, improving the fit.

\[ p_i = \sum_j C_{ij} \cdot x_j + q_i \]

\[ \chi^2 = \sum_i \left( \sum_j A_{ij} \cdot x_j + k_i \right)^2 \]
FTK Pipeline Bandwidth Summary

- **ROD → DF/IM**: 2 Gbps/link, 380 links, 32 boards
- **DF → DF**: ~25 Gbps between shelves, 40 Gbps within the shelf
- **AUX → SSB**: 6.4x4 Gbps, 32 boards
- **DF → AUX**: 6.4 Gbps, 128 boards
- **AUX → AMB**: 12 Gbps
- **AMB → AUX**: 16 Gbps
- **SSB → FLIC**: 32 Gbps total
- **FLIC → ROS**: 32 Gbps total, 2 boards
FTK performance and commissioning

FTK system based on 9 flavor of electronic cards using VME and ATCA standards

Commissioning is currently ongoing
- First tracks reconstructed by the processor expected during this year
- First installation step expects to have ¼ of the final hardware
  - Full detector coverage will be finalized during 2017
- Amount of hardware will grow during the following years according the needs
  - We can proceed with continuous commissioning
  - Complete production for many of the boards

Trigger chain using FTK in preparation
- Track efficiency is expected to be ~93%
- Possible to implement beam-spot determination, b-tagging, tau-tagging, JVT, MET corrections ...