ALICE TPC Upgrade

Front End Card (Revision 0)

Requirements, Functionality, and Implementation

(Draft E, 29 April 2016)

1. Introduction

The Front End Readout Cards (FECs) are designed to provide digitization of data from the chambers of the ALICE TPC Upgrade. A total of 3600 FECs must be produced to instrument the TPC and provide 10% spares. The specifications and requirements of the FEC are discussed in the ALICE TPC Upgrade TDR and have been presented in DOE Project Reviews. They are collected in Table 1 below. Note that many of the specifications are ultimately specifications for the ALICE SAMPA ASIC. The SAMPA is a 32 channel radiation tolerant custom ASIC that provides a charge-sensitive preamp, shaper, digitizer, and transmitter. The first FEC prototype is named "Revision 0." It uses the "MPW2" prototype version of the SAMPA.

Table 1: FEC Specifications

Number of channels	160
Signal polarity	negative
Dynamic range	30x MIP
Noise (in lab, at 18.5 pF)	600e
Conversion gain	20 mV/fC
Peaking time	160 ns
ADC linear range	100 fC
ADC number of bits	10
ADC sampling rate	5 MHz
Power consumption	< 35 mW/ch
Radiation tolerance	up to 5.6 krad integrated dose
Connector	match TPC backplane

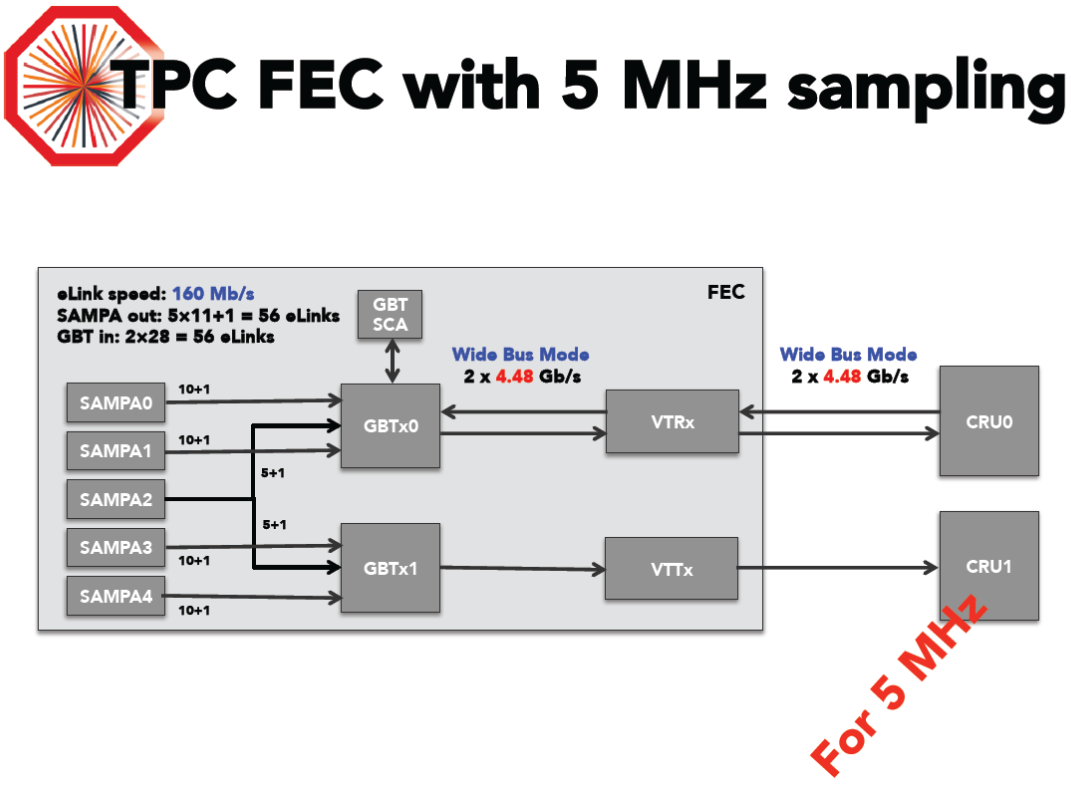

Figure 1: Block diagram of the Rev. 0 FEC

2. General Description and readout concept

The FEC contains 160 channels of charge-sensitive preamplifier/ shapers followed by 10-bit, 5 Msample/s analog-to-digital converters provided by the SAMPA ASICs. The output digital data from each SAMPA ASIC is transmitted as input to one of two GBTx ASICs which then send the data to the ALICE CRU (Control Readout Unit) via optical links provided by the VTRx /VTTx. The basic functional block diagram is shown in Fig. 1. The data digitized at 5 MHz is sent from the 5 SAMPAs to the 2 GBTx ASICS on 160 MHz elinks. There are a total of 56 such elinks per FEC, as indicated in Fig. 1.

The corresponding schematic diagram is separately provided as document **TPC-A_Rev0.pdf**.

3. SAMPA Implementation

a. Power

The SAMPA layout is currently implemented with three discrete grounds and three discrete power supplies. Each SAMPA has its own set of three regulators. The analog supplies are connected together with the exception of the reference which is powered from a separate

regulator due to potential noise issues. The digital supplies have also been combined into a single regulator. We plan to go to a single ground in future versions if possible. Also we will likely share regulators to reduce cost.

b. Front-End configuration

The preamplifier/shaper configuration pins (polarity, shaping, etc.) have been connected to switches for this version which will ensure that all modes are available in case of a failure of any single mode on the MPW2 ASIC. These pins will be hardwired in future versions.

c. JTAG

JTAG is connected for each individual ASIC as slave mode. This ensures testability in case of an ASIC failure. These will be setup as a chain with the GBT-SCA as master in future versions.

d. Clock Configuration

This is connected to switches for the MPW2. These will be hardwired in future versions.

4. GBTx Implementation

a. Power

The two GBTx devices share 1.5V and 2.5V regulators. Grounds are common.

b. JTAG

JTAG for the GBTx is set up so that each of the two GBTx are slaves with the GBT-SCA being the master. This is the preferred configuration of these devices.

c. Clock and data

The clocks for the SAMPAs are supplied by GBTx0. Each SAMPA has its own clock. Data lines from the SAMPAs are connected as shown in Fig. 1. SAMPA0 and 1 are connected to GBTx0; SAMPA3 and 4 are connected to GBTx1. SAMPA2 sends data to GBTx0 and GBTx1.

5. GBT-SCA Implementation

a. Power

Power for the GBT-SCA is supplied by the same 1.5V regulator used for the GBTx. The ground is also common.

b. I^2C bus

The GBT-SCA supplies configuration for all parts through the I^2C bus. Each SAMPA and GBTx has its own clock and data lines so that a single ASIC failure will not inhibit the testing of the parts.

c. Temperature monitoring

Five RTDs are being used to monitor temperature across the board. The GBT-SCA is designed to implement a two-wire RTD measurement. We will reduce the number of RTDs in future versions or utilize a solid-state temperature device since the RTDs are relatively expensive.

6. FEC Control

SAMPA regulators on/off are presently controlled by the GPIO of the GBT-SCA. Additionally, SAMPA pin control through GBT frames (reset, trigger, etc.) are implemented through the GBTx.

7. FEC monitoring

Presently there are only two voltage monitoring sections. The first is the RSSI on the VTRx. RSSI (Received Signal Strength Indicator) monitors the inbound signal strength from the fibers. The second section is the temperature-measuring RTDs. There are several ADC inputs left on the GBT-SCA so that supply voltages can be monitored. Some discussion would be good here regarding the information desired.

8. Estimated power consumption

a. GBTx - ~1.1W
b. GBT-SCA - ~0.1W plus digital.
c. SAMPA - ~1W
d. VTRx – 0.75W
e. VTTx – 1W
f. **TOTAL ASIC – (5*1)+(2*1.1)+1.85 = 9W**

NOTE: This does not include regulator differential which depends upon supply voltage. **Estimated total approximately 16W.**

9. Power up procedure of a full sector

a. Power on, CRU clock present on VTTRx
b. GBTx0-3 power on as slaves
c. GBT-SCA powers on as I^2C master but unconfigured
d. GBTx0
    1. *Use XOSC mode and an I^2C controller to deliver data to GBTx0.*
    2. *Fuse program GBTx0*
e. Allow GBTx0 to lock to CRU clock
f. Use I^2C controller or CRU to configure GBT-SCA.
g. Have GTB-SCA or CRU configure the remaining GBTx1-3.

10. Known Future Changes

There is a list of likely future changes. The changes include:

a. Removal or change to less-expensive temperature measurement devices.
b. Addition of EPROM for board ID.
c. Increased us of board voltage monitors depending upon requirements.
d. Removal of regulators from SAMPAs.

e. Change of grounding to SAMPAs.
f. Removal of individual JTAG interfaces.

11. Known Schematic Errors

a. Input clock/signal unused terminations need to be added on aux GBT-SCA lines.