Opto-Board Prototyping Plan

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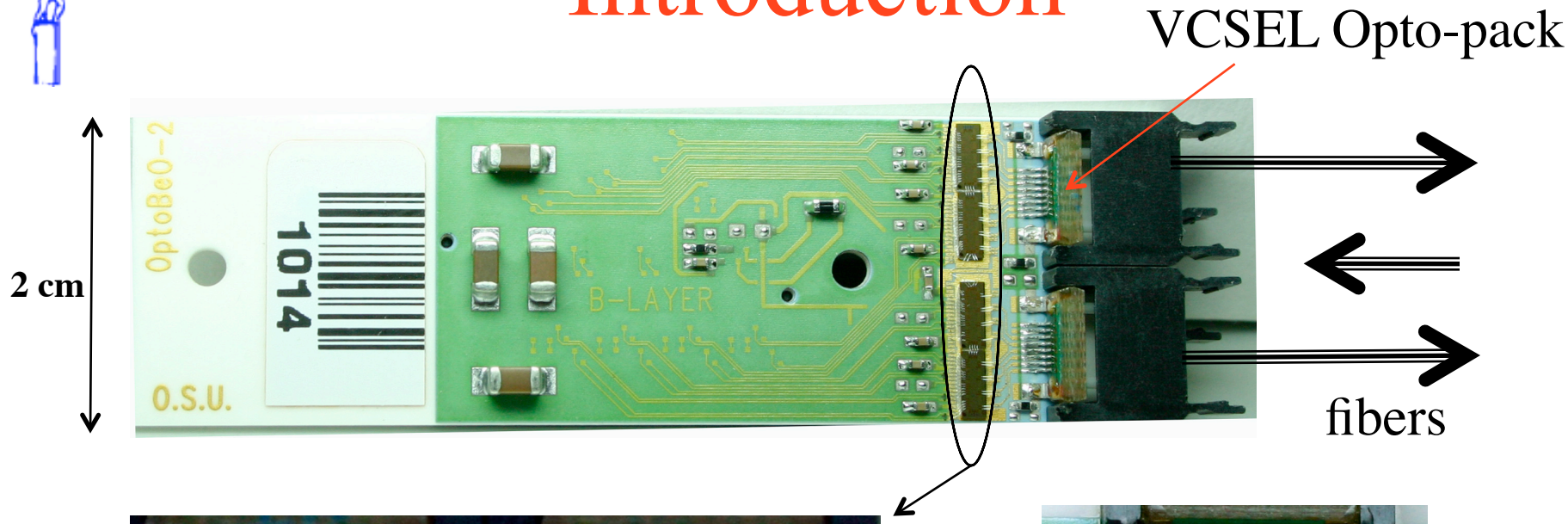
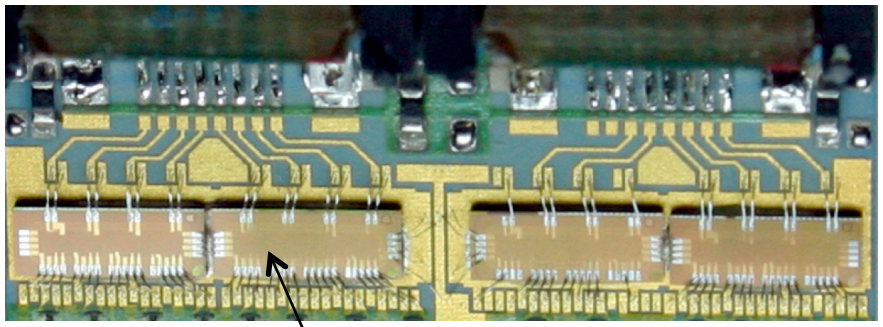
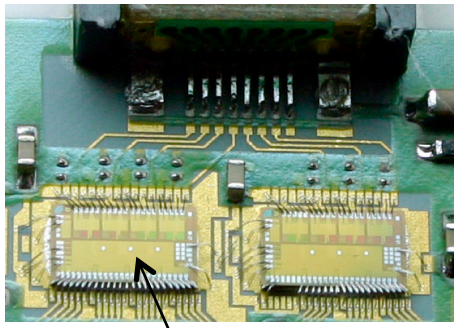
Outline

- Introduction
- Plan
- What if…
- Summary

Introduction





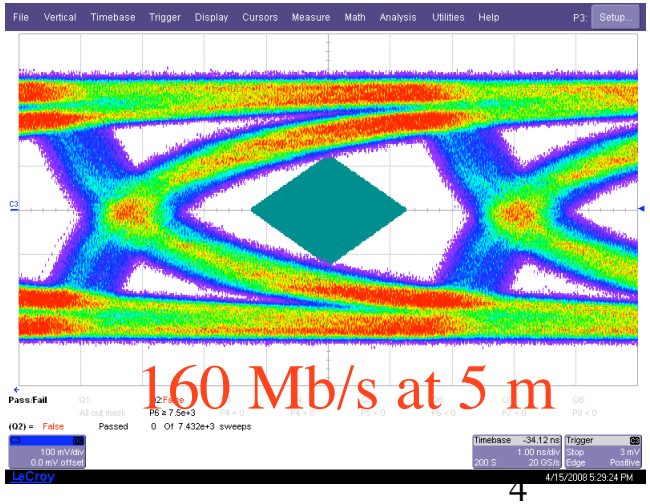


VCSEL Driver Chip (VDC)

PIN Receiver (DORIC)

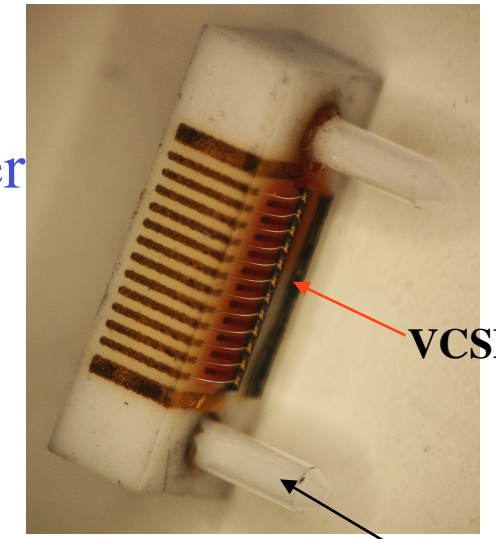
Near-Term Plan

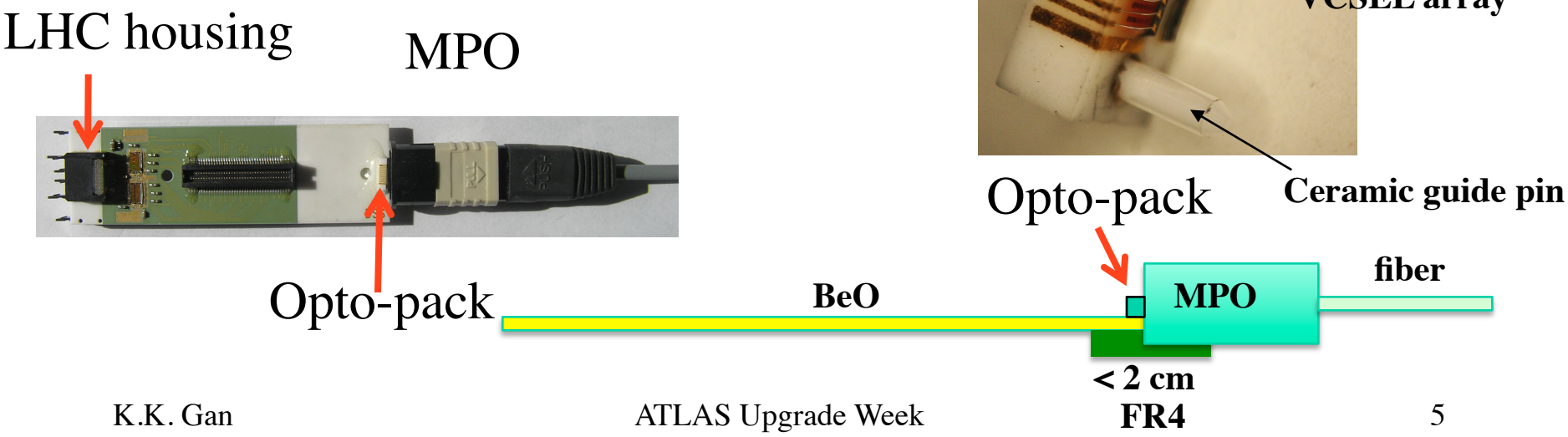
- opto-board has been fabricated:
  - ✔ two BeO opto-packs with AOC 5 Gb/s VCSEL array
  - ✘ one PCB opto-pack with Taiwan PIN array
  - will operate DORIC as it is (40 MHz)
    - will study decode clock/data after 4-6 meters of type0 cable
    - will measure bit error rate
  - will operate VDC at 160 Mb/s
    - receive LVDS signal after 4-6 meters of type0 cable
    - will study optical signal
  - report the result in June IBL meeting



Plan in Autumn

- prototype opto-board in FR-4:
  - use a smaller connector
    - current 80-pin JAE connector supports two VCSEL arrays
  - optimize for BeO opto-pack
  - allow for mounting of MPO connector
  - ⇨ new opto-board will be wider but shorter





VCSEL/PIN Arrays

- propose to use AOC 5 Gb/s VCSEL/Optowell PIN arrays
  - arrays are fabricated in 4 and 12 channels
  - ✘ S-link bandwidth is 8 x (4 x 40 Mb/s)
  - ⇨ can only use 8 of the 12 channels in an array
    otherwise we could build 1/3 less opto-boards!

Clock Multiplier

- Two clock multipliers (4 x 160 MHz and 16 x 4 MHz) in 130 nm layout were submitted in March 2008
  - ✔ no significant degradation observed after irradiation
  - ✘ take μs to recover from SEU in PIN coupled to DORIC
    - observation confirmed with simulation
  - ✘ need power cycling after chip latched up with an SEU
    - effect not reproduced in simulation but discovered a fault in implementing SEU tolerance circuitry

Alternatives…

- if there are problems uncovered in the next few months
  - ⇨ alternative design:
    - DORIC operating at 80 MHz
      - ⇨ no significant degradation observed in irradiated 130 nm prototype chip
    - VDC operating at 160 Mb/s
      - ⇨ irradiated 130 nm prototype chip is working
    - build a more robust opto-links:
      - implement redundancy to bypass broken PIN/VCSEL
      - individual control of VCSEL currents

Summary

- first feasibility test by summer
- first prototype by early 2010
- alternative (and better) design available…