ATLAS/CMS/LCD
RD53 collaboration:

Pixel readout integrated circuits for extreme rate and radiation

3rd LHCC status report

May 25 2016

RD53 SPs: Jorgen Christiansen, CMS & Maurice Garcia-Sciveres, ATLAS on behalf of RD53
Reminder RD53

- Focussed R&D program to develop pixel chips for ATLAS/CMS phase 2 upgrades and LCD vertex
- Extremely challenging requirements for HL-LHC:
  - Small pixels: 50x50um$^2$ (25x100um$^2$) and larger pixels
  - Large chips: ~2cm x 2cm (~1 billion transistors)
  - Hit rates: 3 GHz/cm$^2$
  - Radiation: 1Grad, 2 10$^{16}$ neu/cm$^2$ over 10 years (unprecedented)
  - Trigger: 1MHz, 10us (~100x buffering and readout)
  - Low power - Low mass systems
- Baseline technology: 65nm CMOS
- Full scale demonstrator pixel chip in 2016.
- 19 collaborating institutes and many Guests
  - Bari, Bergamo-Pavia, Bonn, CERN, CPPM, Fermilab, LBNL, LPNHE Paris, Milano, NIKHEF, New Mexico, Padova, Perugia, Pisa, Prague IP/FNSPE-CTU, RAL, Seville, Torino, UC Santa Cruz. (PSI has withdrawn as very busy with phase 1 pixel upgrade)
  - 150 on collaboration Email list,
  - 80 on RD53 NDA list (65nm TSMC technology access),
  - 77 on RD53 guests list (ATLAS/CMS people involved in phase 2 pixel but not on chip design)
  - 55 on serial power list (ATLAS/CMS people interested/working on serial powering)
Internal organization

- Before: R&D in working groups:
  - Radiation effects and rad hard design
  - Analog: Low power/noise/area analog front-ends
  - IP blocks: ADC, DAC, PLL, Modified digital library, etc.
  - Simulation and architecture: Simulation, Optimization, Verification, 
  - IO: IO interface
- Collaboration meetings across WGs
- Now (from 1/1 2016): Focussed on large scale demonstrator
  - Project structure for RD53A demonstrator
    - Bring everything together to make working large scale chip
    - Radiation WG (still a critical issue)
Radiation effects

- Radiation test and qualification of 65nm technology: 1Grad and $2 \times 10^{16}$ neu/cm²
  - Radiation tests with X-rays, Cobalt source and 3Mev protons
- Significant radiation damage above ~100Mrad (only critical for pixels)
  - New radiation effects made it difficult to reach clear conclusions
- Two major “effects”
  - Radiation damage (transconductance) during radiation depends on: Device type, L, W, Bias, Temperature
  - Annealing effects depends on: Temperature, Time, Bias, Device type, L, W, Received dose
    - Partial recovery (transconductance) or getting worse ($V_t$ shift)
  - (Low dose rate effect)
- Realistic to stand 500Mrad with conservative design approach
  - Cold detector: -20 to -10 °C, Not getting hotter than room temperature while powered
  - Analog: Appropriately designed (large transistors) will only have small radiation degradation
    - Confirmed with multiple RD53 prototypes
  - Digital: Suffers significant speed degradation as using small transistors
    - High density logic in pixel array will have significant (200-400%) speed degradation.
      - Only needs 40MHz operation frequency.
      - High density digital library for pixel array (small modifications of TSMC lib)
    - High speed circuits to be designed with large transistors (dedicated digital library)
    - Leakage is not a serious problem in 65nm.
    - Verification with dedicated digital radiation test chip (DRAD)
  - Inner barrel layer to be replaced after 5 years
- 200/500Mrad simulation models extensively used for circuit simulation and optimization
- Full scale pixel chip demonstrator will determine if 1Grad can be accomplished
A few radiation effects plots

**NMOS**

- $L=1000$, $W=1000$
- $L=1000\text{n}, W=120\text{n}$
- $L=60\text{n}, W=1000\text{n}$

**PMOS**

- Radiation Induced Narrow Channel Effect: RINCE (known)
- Radiation Induced Short Channel Effect: RISCE (new)
- Detrimental annealing effect (new)

- PMOS, $L=60\text{n}, W=600\text{n}$
(bad) Annealing

- Significant $V_t$ shift can develop with annealing depending on Temperature, Time, Bias, Device type, $L$, $W$, Received dose,
  - Foundry specific problem?
- Latest's news: Indication that detrimental effect can be “avoided”/delayed by keeping cold
  - -20°C for 10 years
  - Room temp for few months (if unbiased more?)

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### Graphs:

- **Graph 1:** Comparison of annealing effects at different biases and temperatures.
  - 0V bias
  - Diode 1.2V bias

- **Graph 2:** Activation energy extraction vs. time for various temperatures.
  - 100°C
  - 60°C
  - 40°C
  - 20°C
  - -20°C

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Changing technology?

- **High density required in small pixels for hit storage during trigger latency**
  - 130nm technology not sufficient density
- **Other 65nm technologies will now be tested for radiation damage**
  - One technology has been seen to have similar radiation damage, but most likely less detrimental annealing (but not any more available)
  - Others could be better or worse (unpredictable)
- **Sub 65nm**
  - Not yet radiation tested to these high levels
  - Significantly increased cost and complexity
- **We would be “alone” as no other detectors needs to change technology**
  - Technology access, design kit, support, radiation testing, IPs, shared runs, etc.
- **RD53 stays with current 65nm technology for large scale demonstrator**
  - Major design efforts invested in this
  - Appears viable for 500Mrad when taking appropriate precautions
  - If we are forced to change technology it will take ~1 year to remap design, IPs, FEs, libraries plus extensive radiation testing program will be needed.

**Bad combination “avoidance”:**
- >200Mrad (inner layer),
  - Replace inner layer(s) after 5 years (5% surface)
- Radiation at High/room temperature:
  - Pixel will run cold (-10 -20°C)
- Small PMOS: High density digital
  - Only needs to run 40MHz
- Analog and Fast Digital circuits:
  - Dedicated designs with large transistors
- High/room temperature anneal
  - Pixel runs cold
  - No bias/power when not cooled

Needs to confirm that this “avoidance strategy” is sufficient and reliable
DRAD chip

- Dedicated test chip to measure delay degradation and power consumption of digital logic
  - RD53, MPA, LPGBT
- Test structures with different types of gates: NAND, NOR, buffers, flip-flop, latch
- SEU test structure
- 9 different libraries: 7-18 track
  - Small, Mid, Large transistors
  - Low Vt, normal Vt, High Vt
  - Linear, enclosed
- Submitted March. 2016
- Return: End May
- Radiation test campaign during summer

Some gates (e.g. 4NOR) more affected than others

Simulated delay degradation (room temp. radiation)
Analog FEs

- Low power/noise/area analog pixel Front-Ends
- ~50% pixel area for analog
- Analog front-end specifications defined
  - Capacitance, threshold, noise, power, dispersion, etc.
- Evaluation of alternative FE architectures
  - 3 implementations of TOT FEs
    - 2 slow (40MHz counting) TOT
    - 1 fast (200MHz counting) TOT
  - 1 Non linear fast digitizing FE
- 3 FEs prototyped and extensively tested
  - Limited radiation effects
IPs

- Building blocks required to build full pixel chip
  - Large diversity of different IP blocks developed
    - ADCs, DACs, sensors (temp, current, radiation), Bandgap references, analog buffers, specialized storage cells, PLL, serializers, differential inputs/outputs, shunt-LDO, Power on reset, differential drivers/receivers, etc.
  - Specs and data sheets defined
  - IPs prototyped and tested.

- Large design effort
Simulation/verification

- Simulation and verification framework for pixel chip
  - Based on system Verilog and UVM (industry standard for ASIC design and verification)
  - Available on repository and being used by several groups
    - Reference model
    - Basic/generic pixel chip
    - Detailed RTL/gate level implementations
    - Integration with ROOT to import hits from detector simulations and for monitoring and analysing results.
  - Simulation of alternative architectures with Monte Carlo data and/or internally generated hits
    - Performance characterization of different architectures
  - Verification of small scale prototypes
  - Power profiling under different conditions (hits, trigger)

- Plans
  - Inclusion of SEU simulation/verification
  - Detailed verification of demonstrator chip
Pixel array prototypes

- **FE65-P2: 64 x 64 pixels**
  - 2 x 2 pixel region (evolution from FEI4)
  - Low rate readout
  - Double Analog / Digital isolation
  - 4b-ToT with slow (40MHz) FE

- **CHIPIX65: 64 x 64 pixels**
  - 4 x 4 Pixel Region
  - Single Analog / Digital isolation
  - 5b-ToT with slow and fast FEs
  - Includes multiple RD53 IP-blocks
  - Status: Submission June 2016

- **RD53A: 400 x 400(200) pixels**
  - Status: Under design
FE65-P2 test results

3.9 µA/pixel
4.6 µA/pixel

Vth1 = 30
PrmpVbpf = 50
Vff = 24

Before radiation

ENC

Threshold

only 0.2% s-curves failing
untuned!

After 350Mrd
RD53A

- **Demonstrator chip:**
  - Full size chip: ~2cm x 1(2)cm, small pixels (50x50um²), Large pixels, Very high hit and trigger rates, Radiation and SEU tolerance, Effective in-time threshold: 1200e-, Low power, Serial powering, Functional in test beams, etc.
  - Specification document agreed with CMS and ATLAS phase 2 pixel communities.
    - Pixel sensors compatible with this chip being prepared in both ATLAS and CMS
  - Engineering run ~1M$ (we better get this right!)
    - Shared run with other project(s) (CMS MPA)
    - Demonstrator will be ~1/2 size, but designed as being full size
    - Starting to collect required funds (500k$)

- **Converge all activities in RD53 and WGs on this vital goal/milestone**

- **Schedule:**
  - Up-scaling small demonstrator: Now
  - First version of near final chip: Q3 2016
  - Final version: Q4 2016
  - (plus some months for extensive verifications)

- **Core design team: ~10 and increasing**
  - Weekly design meetings since the beginning of the year.
  - Regular 1-2 days getting together
  - Defined project structure and responsibilities
  - Groups: INFN, Bonn, LBNL, Marseilles, NIKHEF, CERN
# RD53A Project Structure

## RD53A Chip: Jorgen, Maurice
- Specifications
- Documentation
- General organization

## Test System: TBD (Bonn, CERN, Pisa, ?)
- Requirements, specifications
- Hardware, Firmware, Software
- Chip test/characterization: wafer level, chip level, beam tests
- Radiation testing

## RD53A Chip Integration/Verification: Flavio, Deputy: Tomasz

### Floorplan: Flavio, Dario
- Pixel array, Bump pad
- EOC
- Power distribution
- Bias distribution
- Analog/digital isolation
- Integration/verification

### Analog FEs (3/4) with biasing: Luigi, Valerio, Ennio, Abder, IP designers
- Specification/performance
- Interface (common)
- Analog isolation
- Digital/timing model
- Abstract
- Verification of block: function, radiation, matching, etc.
- Shared database
- Integration in design flow
- Distribution of global analog signals
- Verification of integration

### Monitoring: Francesco, Mohsine, IP designers
- Specification/performance
- Interface
- Analog isolation
- Digital/timing model
- Abstract
- Verification of block: function, radiation, matching, etc.
- Shared database
- Integration in design flow
- Verification of integration

### Digital: Tomasz
- **Simulation Framework: Elia, Sara, Rebecca**
  - Framework
  - Hit generation/Import MC
  - Reference model / score board
  - Monitoring/verification tools
  - Generic behavioural pixel chip
  - SEU injection
- **Architecture: Elia, Sara, Andrea, Luca,**
  - Evaluation – choice: Performance, Power, Area
  - Simulation/optimization
  - Functional verification
  - SEU immunity
- **Pixel array/pixel regions: Sara, Andrea**
  - Latency buffer
  - Core/column bus
- **Readout/control interface: Roberto, Paris**
  - Data format/protocol
  - Rate estimation / Compression
  - Implementation
- **Configuration: Roberto, Luca, Mohsine**
  - External/internal interface
  - Implementation
- **Implementation: Dario, Luca, Andrea, Luigi, Francesco, Sara,**
  - Script based to “quickly” incorporate architecture/RTL changes
  - RTL - Synthesis
  - Functional verification
  - SEU verification
  - P&R
  - FE/IP integration
  - Clock tree synthesis
  - Timing verification
  - Power verification
  - Physical verification
  - Final chip submission

### Digital lib.: Dario, Sandeep, Mohsine
- Customized rad tool library
- Liberty files (function, timing, etc.)
- Characterized for radiation
- Custom cells (Memory, Latch, RICE)
- Integration with P&R
- Radiation tolerance
- Integration in design kit

### Power: Michael, Sara, Flavio
- Shunt-LDO integration
- On-chip power distribution
- Optimization for serial powering
- System level power aspects
- Power Verification

### IO PAD frame: Hans
- Wirebonding pads, ESD, SLVS, Serial readout, Shunt-LDO, analog test
  - Input/output

### Testing/Yield optim.: Sandeep, Luca ?
- Testability
- Scan path
- BIST
- Redundancy
- Bump-bonding test/verification

### Support and services:
- Tools, design kit: Wojciech, Sandeep
- Clissoft repository: Elia, Dario, Sandeep, Wojciech
- Radiation effects and models: Mohsine
RD53A status

**On-going:**
- Architecture simulations and optimization using Monte Carlo hit data from experiments.
- Global floor plan: Upscaled small demonstrator
- Shared repositories: IPs, FEs, RTL code, Simulation, full design
- Optimization of design flow & tools for very large complex design
- Integration of FEs (4) with biasing and required adaptions
- Integration of monitoring: ADC, Temp sensor, voltages, currents, etc.
- Integration of serial powering
  - Distributed power dissipation, power profiling, decoupling, system simulations
- Integration of IO pad frame
- Digital: RTL coding and technology mapping
  - Pixel array: Optimization (power, size, radiation tolerance)
  - EOC: Command decoder, chip configuration, readout data formatting, data compression
  - Synthesis and timing optimization/verification with radiation effects
  - Verification framework

**To come:**
- SEU optimisation and verification
- Final integration
- Extensive Analog and digital verification
- DRC verification
- Submission

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**Metrics**

<table>
<thead>
<tr>
<th></th>
<th>4x4 centralized buffer architecture</th>
<th>2x2 distributed buffer architecture</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hit loss due to dead time (%)</td>
<td>2.44 - 0.59</td>
<td>0.58 - 2.67</td>
</tr>
<tr>
<td>Hit loss due to buffer overflow (%)</td>
<td>14 locations: 0.46</td>
<td>7 locations: 0.06 - 0.07</td>
</tr>
<tr>
<td>Hit loss due to limited ToTs (%)</td>
<td>0.29** (6 ToTs max)</td>
<td>-</td>
</tr>
<tr>
<td>Total loss (%)</td>
<td>3.19 (14 loc.)</td>
<td>1.8-3.24 (7 loc.)</td>
</tr>
<tr>
<td>Pixel region area*** (digital, post synthesis, pre-PDK) (um²/pixel)</td>
<td>664 (14 loc.)</td>
<td>0.60-2.71 (9 loc.)</td>
</tr>
<tr>
<td>Power consumption (average, post-PDK) (mW/pixel)</td>
<td>coming soon</td>
<td>4.932 (typical) 6.223 (worst)</td>
</tr>
</tbody>
</table>

* Centralized architecture features 6 ToTs. ** To be repeated with MC edges of barrel data. *** No TDC in either architecture

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**Power profiling**

- Time resolution: 1ns, 25ns, 100ns, 1 µs, 10 µs (zoom on shorter simulation window)
- Delay corner considered: RD53A typ
- Activity conditions: with hits (3 GHz/cm² hit rate) and triggers (1 MHz rate)

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**400x400 pixels power**

<table>
<thead>
<tr>
<th></th>
<th>Typ</th>
<th>Worst</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog array</td>
<td>0.96W</td>
<td>1.6W</td>
</tr>
<tr>
<td>Digital array</td>
<td>0.77W</td>
<td>0.99W</td>
</tr>
<tr>
<td>EOC</td>
<td>0.2W</td>
<td>0.3W</td>
</tr>
<tr>
<td>IO</td>
<td>0.2W</td>
<td>0.3W</td>
</tr>
<tr>
<td>Shunt-LDO</td>
<td>0.5W (25%)</td>
<td>1W (30%)</td>
</tr>
<tr>
<td>Total</td>
<td>~3W</td>
<td>~4W</td>
</tr>
</tbody>
</table>
Many groups and people working on a focussed R&D effort to implement very high rate pixel chip for extreme radiation.

Large number of circuits, building blocks and small pixel arrays have been successfully prototyped and tested in 65nm technology.

Improved understanding of the initially “mysterious” radiation effects seen at extreme radiation levels above 100Mrad:

- Many circuits and devices radiation tested
- 500Mrad appears as realistic goal
- Test of full pixel chip will determine if 1Grad is feasible when cold

Focussed on submitting full scale demonstrator chip:

- Building blocks available and tested
- Extensive experience gained with small pixel array prototypes
- Defined design team with weekly meetings
- Submission: ~End 2016
Backup slides
More information

- RD53 collaboration meetings: https://indico.cern.ch/category/5036/
- ACES: https://indico.cern.ch/event/468486
  - RD53 + ATLAS and CMS phase 2 pixel upgrades
- Radiation seminar: https://indico.cern.ch/event/442426/
- Conferences/workshops
- Coming conferences/workshops
  - Pixel, Vertex, TWEPP, IWORD, FE workshop
Top level WG

- Architecture and floor-plan for large pixel chip
  - Digital sea with analog islands floorplan
    - Distribution of power and global signals
    - Analog – Digital isolation
  - Digital “on-top” design flow
  - Pixels – Pixel regions – Pixel cores – End of column
  - Implementation of small 64x64 pixel demonstrator in 65nm (submission end of this month)
    - Re-optimized “FEI4” for small pixels, higher hit and trigger rates.

- Plans
  - Refinement of pixel chip (digital) architecture
    - Using simulation framework
  - Integration of full pixel chip demonstrator

RD53A

Pixel chip: ~2cm² = ~160k pixels of 50x50um²
Phase 2 pixel challenges

- ATLAS and CMS phase 2 pixel upgrades very challenging
  - Very high particle rates: 500MHz/cm²
    - Hit rates: 2-3 GHz/cm² (factor 16 higher than current pixel detectors)
  - Smaller pixels: ¼ - ½ (25 – 50 um x 100um)
    - Increased resolution
    - Improved two track separation (jets)
  - Participation in first/second level trigger?
    A. 40MHz extracted clusters (outer layers)?
    B. Region of interest readout for second level trigger?
  - Increased readout rates: 100kHz -> 1MHz
  - Low mass -> Low power

Very similar requirements (and uncertainties) for ATLAS & CMS

- Unprecedented hostile radiation: 1Grad, 2 $10^{16}$ Neu/cm²
  - Hybrid pixel detector with separate readout chip and sensor.
  - Phase2 pixel will get in 1 year what we now get in 10 years

- Pixel sensor(s) not yet determined
  - Planar, 3D, Diamond, HV CMOS, ...
  - Possibility of using different sensors in different layers
  - Final sensor decision may come relatively late.

- Very complex, high rate and radiation hard pixel readout chips required
Radiation effects

Thick Shallow Trench Isolation Oxide (~ 300 nm); radiation-induced charge-buildup may turn on lateral parasitic transistors and affect electric field in the channel.

Doping profile along STI sidewall is critical; doping increases with CMOS scaling, decreases in I/O devices.

Increasing sidewall doping makes a device less sensitive to radiation (more difficult to form parasitic leakage paths).

Charge buildup in gate oxide and interface states affects $V_t$.

Spencer dielectrics may be radiation-sensitive.

Birds beak parasitic device.
### Pixel chip generations

<table>
<thead>
<tr>
<th>Generation</th>
<th>Current FEI3, PSI46</th>
<th>Phase 1 FEI4, PSI46DIG</th>
<th>Phase 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel size</td>
<td>100x150um² (CMS) 50x400um² (ATLAS)</td>
<td>100x150um² (CMS) 50x250um² (ATLAS)</td>
<td>25x100um² ?</td>
</tr>
<tr>
<td>Sensor</td>
<td>2D, ~300um</td>
<td>2D+3D (ATLAS) 2D (CMS)</td>
<td>2D, 3D, Diamond, MAPS ?</td>
</tr>
<tr>
<td>Chip size</td>
<td>7.5x10.5mm² (ATLAS) 8x10mm² (CMS)</td>
<td>20x20mm² (ATLAS) 8x10mm² (CMS)</td>
<td>&gt; 20 x 20mm²</td>
</tr>
<tr>
<td>Transistors</td>
<td>1.3M (CMS) 3.5M (ATLAS)</td>
<td>87M (ATLAS)</td>
<td>~1G</td>
</tr>
<tr>
<td>Hit rate</td>
<td>100MHz/cm²</td>
<td>400MHz/cm²</td>
<td>2(3) GHz/cm²</td>
</tr>
<tr>
<td>Hit memory per chip</td>
<td>0.1Mb</td>
<td>1Mb</td>
<td>~16Mb</td>
</tr>
<tr>
<td>Trigger rate</td>
<td>100kHz</td>
<td>100KHz</td>
<td>200kHz - 1MHz</td>
</tr>
<tr>
<td>Trigger latency</td>
<td>2.5us (ATLAS) 3.2us (CMS)</td>
<td>2.5us (ATLAS) 3.2us (CMS)</td>
<td>6 - 20us</td>
</tr>
<tr>
<td>Readout rate</td>
<td>40Mb/s</td>
<td>320Mb/s</td>
<td>1-4Gb/s</td>
</tr>
<tr>
<td>Radiation</td>
<td>100Mrad</td>
<td>200Mrad</td>
<td>1Grad</td>
</tr>
<tr>
<td>Technology</td>
<td>250nm</td>
<td>130nm (ATLAS) 250 nm (CMS)</td>
<td>65nm</td>
</tr>
<tr>
<td>Architecture</td>
<td>Digital (ATLAS) Analog (CMS)</td>
<td>Digital (ATLAS) Analog (CMS)</td>
<td>Digital</td>
</tr>
<tr>
<td>Buffer location</td>
<td>EOC</td>
<td>Pixel (ATLAS) EOC (CMS)</td>
<td>Pixel</td>
</tr>
<tr>
<td>Power</td>
<td>~1/4 W/cm²</td>
<td>~1/4 W/cm²</td>
<td>½ - 1 W/cm²</td>
</tr>
</tbody>
</table>
### Working groups

<table>
<thead>
<tr>
<th>WG</th>
<th>Domain</th>
</tr>
</thead>
<tbody>
<tr>
<td>WG1</td>
<td>Radiation test/qualification</td>
</tr>
<tr>
<td></td>
<td>Coordinate test and qualification of 65nm for 1Grad TID and $10^{16}$ neu/cm$^2$</td>
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<tr>
<td></td>
<td>Radiation tests and reports.</td>
</tr>
<tr>
<td></td>
<td>Transistor simulation models after radiation degradation</td>
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<tr>
<td></td>
<td>Expertise on radiation effects in 65nm</td>
</tr>
<tr>
<td>WG2</td>
<td>Top level</td>
</tr>
<tr>
<td></td>
<td>Design Methodology/tools for large complex pixel chip</td>
</tr>
<tr>
<td></td>
<td>Integration of analog in large digital design</td>
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<tr>
<td></td>
<td>Design and verification methodology for very large chips.</td>
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<td></td>
<td>Design methodology for low power design/synthesis.</td>
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<td></td>
<td>Clock distribution and optimization.</td>
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<tr>
<td>WG3</td>
<td>Simulation/verification framework</td>
</tr>
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<td></td>
<td>System Verilog simulation and Verification framework</td>
</tr>
<tr>
<td></td>
<td>Optimization of global architecture/pixel regions/pixel cells</td>
</tr>
<tr>
<td>WG4</td>
<td>I/O + (Standard cell)</td>
</tr>
<tr>
<td></td>
<td>Development of rad hard IO cells (and standard cells if required)</td>
</tr>
<tr>
<td></td>
<td>Standardized interfaces: Control, Readout, etc.</td>
</tr>
<tr>
<td>WG5</td>
<td>Analog design / analog front-end</td>
</tr>
<tr>
<td></td>
<td>Define detailed requirements to analog front-end and digitization</td>
</tr>
<tr>
<td></td>
<td>Evaluate different analog design approaches for very high radiation environment.</td>
</tr>
<tr>
<td></td>
<td>Develop analog front-ends</td>
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<tr>
<td>WG6</td>
<td>IP blocks</td>
</tr>
<tr>
<td></td>
<td>Definition of required building blocks: RAM, PLL, references, ADC, DAC, power conversion, LDO,</td>
</tr>
<tr>
<td></td>
<td>Distribute design work among institutes</td>
</tr>
<tr>
<td></td>
<td>Implementation, test, verification, documentation</td>
</tr>
</tbody>
</table>
RD53 collaboration

- 20 Institutes (Seville has joined)
  - Bari, Bergamo-Pavia, Bonn, CERN, CPPM, Fermilab, LBNL, LPNHE Paris, Milano, NIKHEF, New Mexico, Padova, Perugia, Pisa, Prague IP/FNSPE-CTU, PSI, RAL, Seville, Torino, UC Santa Cruz.
- 140 on collaboration Email list
  - ~70 actively contributing
  - 2015 FTE: ~23
- 50 on RD53 guests email list
- Spokes persons: Maurice Garcia-Sciveres, LBNL (ATLAS), Jorgen Christiansen, CERN (CMS)
- IB chair: Lino Demaria, Torino
- WG conveners: Marlon Barbero, Roberto Beccherle, Jorgen Christiansen, Maurice Garcia-Sciveres, Tomasz Hemperek, Valerio Re
- 2 year terms coming up to renewal within 3 months

- MOU defined and signed (few exceptions)
- RD53 collaboration meetings: 2 times per year
- RD53 management meetings: Monthly
- WG meetings: Monthly – bi-monthly

<table>
<thead>
<tr>
<th>Activity</th>
<th>FTE 2015</th>
</tr>
</thead>
<tbody>
<tr>
<td>Radiation</td>
<td>4</td>
</tr>
<tr>
<td>Analog</td>
<td>3</td>
</tr>
<tr>
<td>IP</td>
<td>7</td>
</tr>
<tr>
<td>Simulation</td>
<td>3</td>
</tr>
<tr>
<td>Top</td>
<td>3</td>
</tr>
<tr>
<td>IO</td>
<td>1</td>
</tr>
<tr>
<td>Organization</td>
<td>2</td>
</tr>
<tr>
<td>Total</td>
<td>~23</td>
</tr>
</tbody>
</table>
Radiation effects (PMOS)

Requires an extended seminar to explain all this.
### Power Consumption

<table>
<thead>
<tr>
<th>400x400 pixels power</th>
<th>Typ</th>
<th>Worst</th>
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</thead>
<tbody>
<tr>
<td>Analog array</td>
<td>0.96W</td>
<td>1.6W</td>
</tr>
<tr>
<td>Digital array</td>
<td>0.77W</td>
<td>0.99W</td>
</tr>
<tr>
<td>EOC</td>
<td>0.2W</td>
<td>0.3W</td>
</tr>
<tr>
<td>IO</td>
<td>0.2W</td>
<td>0.3W</td>
</tr>
<tr>
<td>Shunt-LDO</td>
<td>0.5W (25%)</td>
<td>1W (30%)</td>
</tr>
<tr>
<td>Total</td>
<td>~3W</td>
<td>~4W</td>
</tr>
</tbody>
</table>