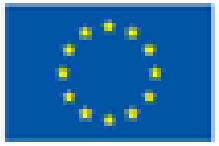

Topical Workshop on Beam Loss Monitors (15-16/09/2016)

THE NEW BEAM LOSS MONITORING SYSTEM FOR CERN'S INJECTOR COMPLEX

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Introduction

This project has undertaken the task to develop up-to-date Beam Loss Monitoring System for the Injectors.

Mainly,

- Build a generic, highly configurable and high-performing system
- Acquisition part to accept several detector types
- Use reprogrammable parts to target all injectors' requirements

Team members (past and present):

BI-BL: M. Alsdorf, C. Arcola, B. Dehning, C. Hajdu, M. Kwiatkowski, O. Malnasi-Csizmadia, W. Vigano, C. Zamantzas

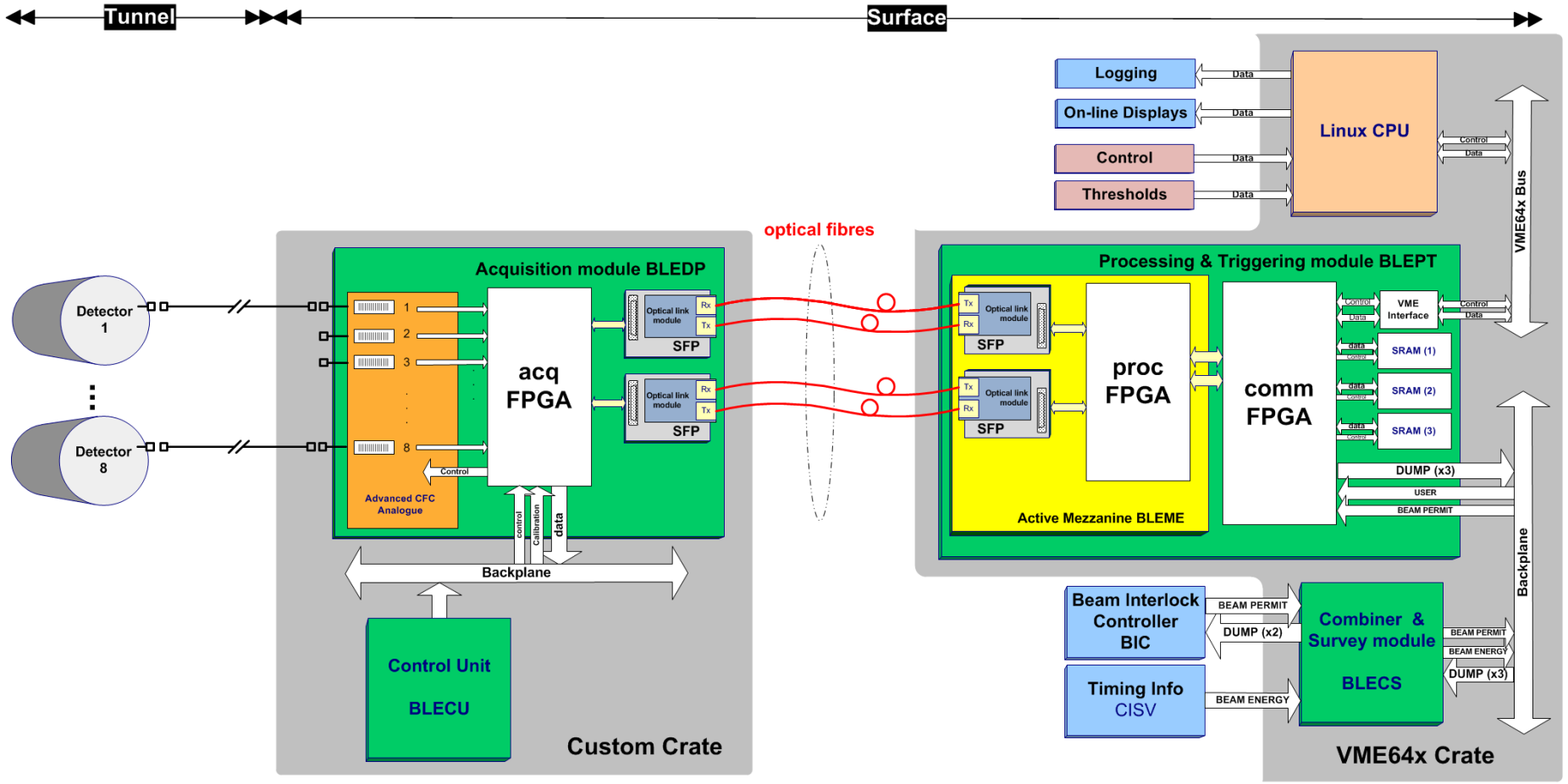
and support from: E. Effinger, J. Emery, G. Venturini, E. Nebot Del Busto

BI-SW: E. Angelogiannopoulos, S. Jackson, L. Jensen, B. Kolad

Outline

- Specifications
  - Dynamic range, Measurements, Supervision, Interlocking
- System overview
  - Architecture, Cabling
- Electronics
- Examples of the installations in LINAC4, PSB and PS
- Summary

System Architecture



SPECIFICATIONS

Acquisition & Processing

Is timing/synchronisation at the acquisition and/or processing level necessary?

- **Synchronisation** is **required** with the **start of the cycle** to
  - Perform calculation of integration periods and
  - Schedule comparisons with their corresponding threshold values
  - Record high frequency observation data
  - Schedule the data readout and publish by the CPU

- **Synchronisation** is **achieved** by
  - Use the 'Start of Cycle', 'Beam In' and 'Beam Out' events received through the timing system.
  - Dedicated timing card with broadcast in the backplane.
  - Sync is done at the processing level (i.e. 2 samples jitter between cards).

Integration Periods

Continuously the processing electronics calculate 4 **integration period values** for each channel:

- **2 μs**, **400 μs**, **1 ms** and **1.2 s** (machine basic period)
  - Implemented as moving sum windows in the hardware
  - Calculation is refreshed at acquisition frequency
- Compare with predefined thresholds
  - **Machine protection** with hardware implementation comparisons on each refresh
  - **Limit radiation levels** with software implementation comparisons at end of cycle
  - ➢ See also next slide.
- Calculate for each channel the maximum values recorded on each integration period during the cycle
  - Published for the online displays and
  - Send to the long-term logging

Threshold Comparisons

Hardware implementation part:

- All calculated **integration period values**, i.e from **2 μs** to **1.2 s**, will be constantly checked against their threshold values:
  - 4 threshold values, one for each of the integration periods.
  - Comparisons happen at the refresh period – that is, every 2 μs
  - In the case the measured values exceed those the beam permit signal will be removed for **all users**
  - The **blocked** beam permit signal will be **latched** until an operator acknowledges.
- The **threshold values** will be need to be set **unique per channel:**
  - Each card will process 8 channels

Software implementation part:

- All maximum **integration period values** recorded on the cycle will be checked against a second set of threshold values. The outputs will be used for **repeated over threshold function**
  - Additional threshold values for the same integration periods will also be required.
  - In the case found to be over threshold repeatedly *n* times it will be required to block **that user's injections**.
  - The **blocked** beam permit signal will be **latched** until an operator acknowledges.
  - The repeat value *n* will be settable per monitor in the range of 1 to 16.
- The **threshold values** will need to be **unique per user and per channel:**
  - Each CPU will process 8 cards x 8 channels
  - The information of the current user has to be obtained from the telegram per cycle -> dedicated **timing card**
  - Memory for 32 users will be reserved.

Beam Permit Logic

- System [HW and/or SW] will **block** injections
  - i.e. "remove permit" if losses over threshold
- System [SW] will **remember** if the user is allowed to have beam
  - i.e. "give permit" if previous cycle for the user was ok (or previous interlocks were cleared)
- The Beam Interlock Controller will be configured in the "Non-latch" mode.
  - i.e. the system will need to follow timing and notify in advance.
- Aiming to keep system **latency** (from measurement to output) small
  - HW: The target for the fast integration periods is < 10 µs
  - SW: Block on next cycle
- Only data from the **current cycle** need to be considered.
  - Timing in the electronics essential (i.e. possible failure mode)

Ambient Radiation Measurement

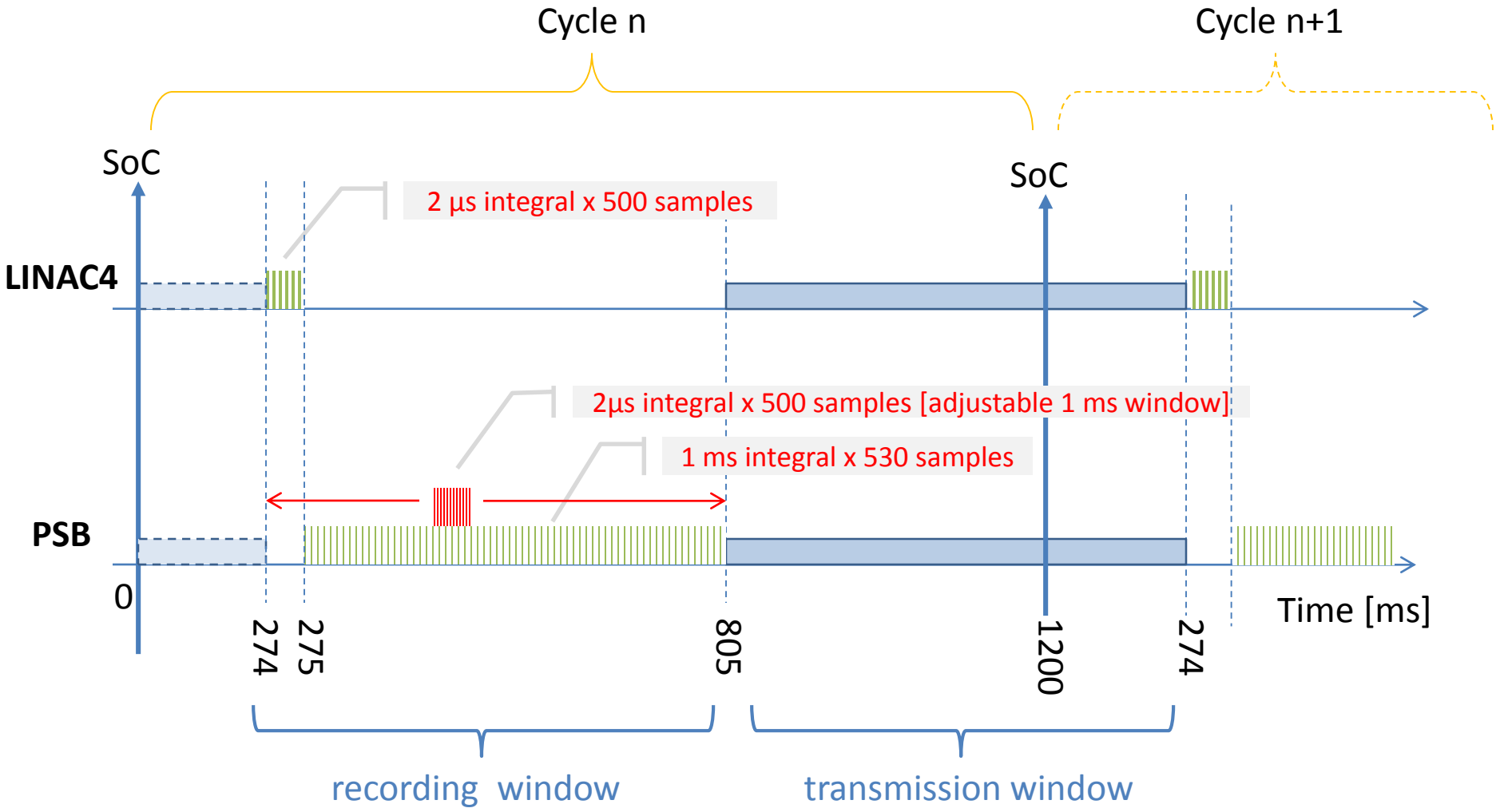
Calculate and log the ambient radiation measured at the end of each cycle

- Processing electronics will provide two values:
  - total accumulated in the cycle (already described) and
  - total accumulated with beam present
- Subtraction of the two values in CPU
- Additional timing events to be used for the recording
- Values will come together with number of samples used in the recording to allow accurate conversion to user-friendly units, i.e. Gy, Gy/s, …
- Publish values for the online displays and the long-term logging

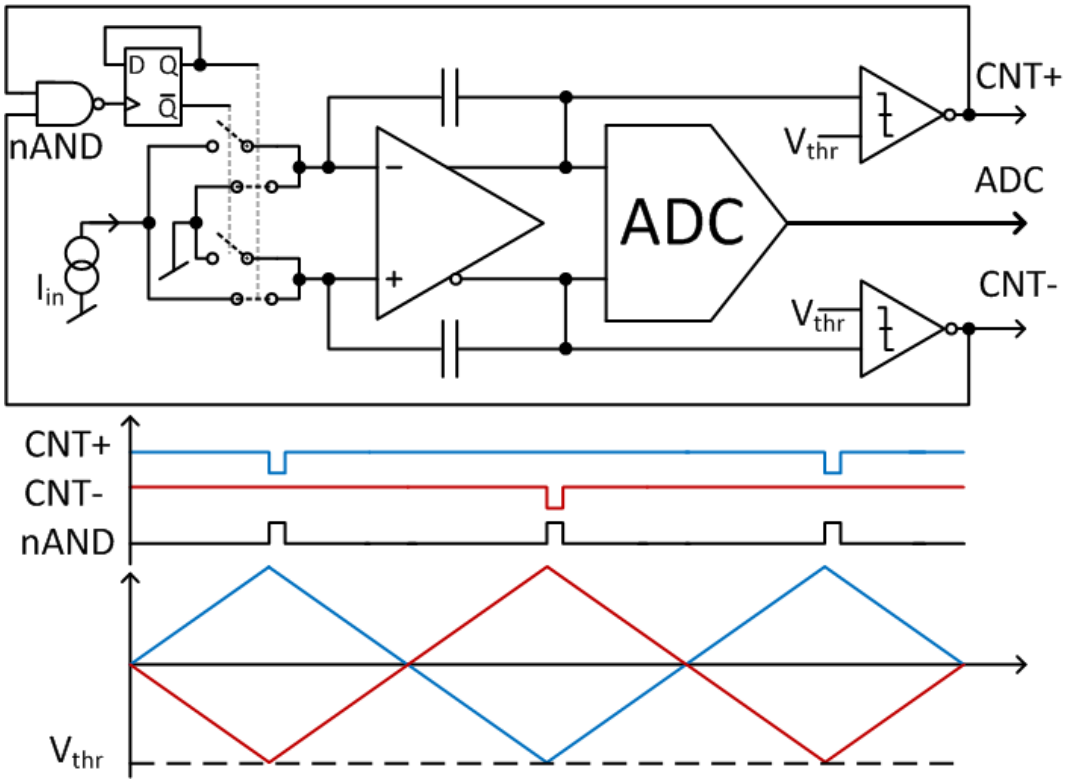
Evolution Over Time buffer

- Record detailed observation data
  - Publish on the online displays
  - Log on demand
- LINAC4:
  - 2 μs samples for 1 ms during beam presence
- PSB:
  - 1 ms samples for 600 ms during beam presence
  - 2 μs samples for 1 ms with adjustable start (aka Capture)
- Readout and transmission window by CPU during beam-out period

Evolution & Capture functions

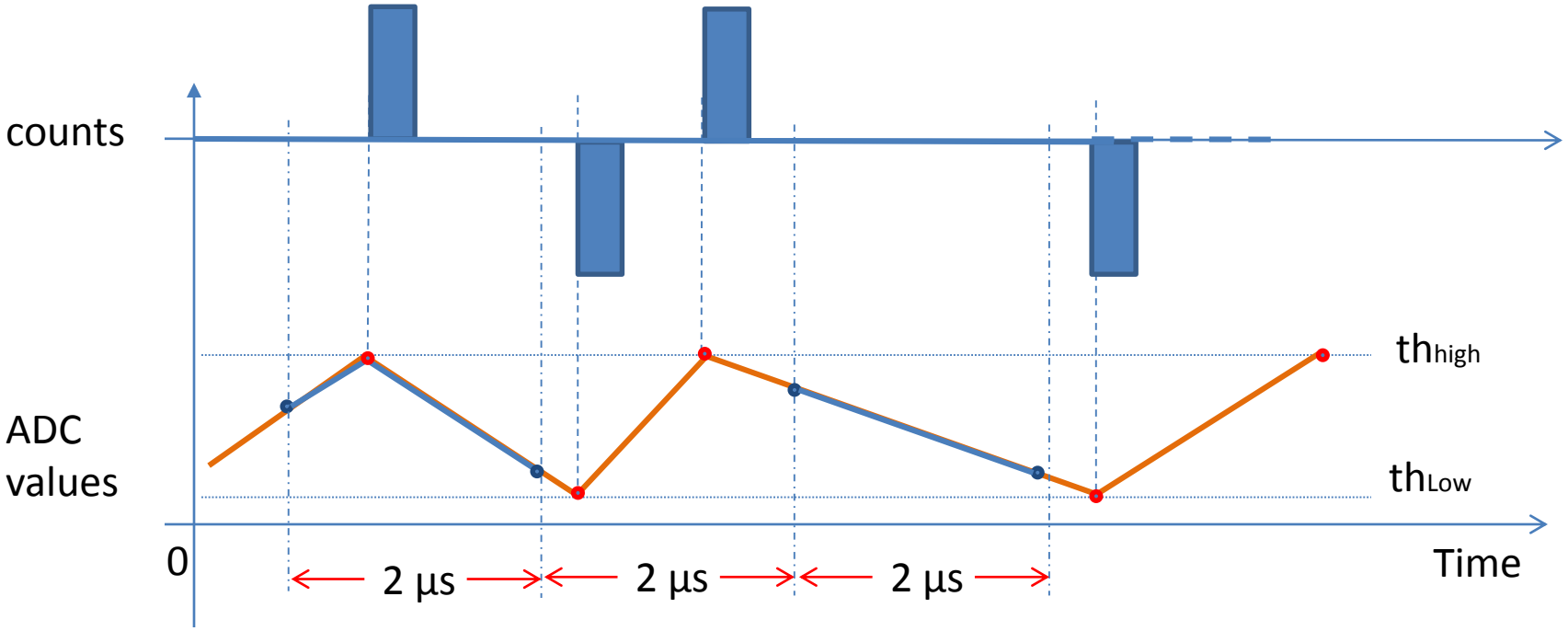


FDFC: Acquisition Principle



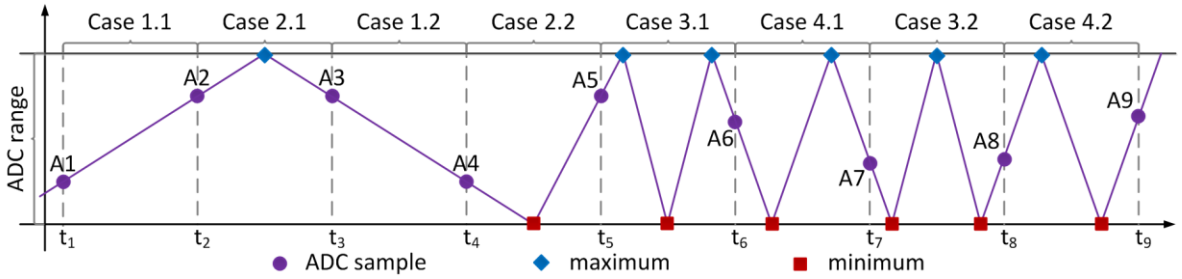
- A status signal selects in which branch of a fully deferential stage the input current is integrated.
- Two comparators check the deferential output voltage against a threshold, whenever is exceeded, the status signal changes to the complementary value (0 ! 1 or 1 ! 0) and the input current is integrated in the other branch.

FDFC: Data Pre-Processing



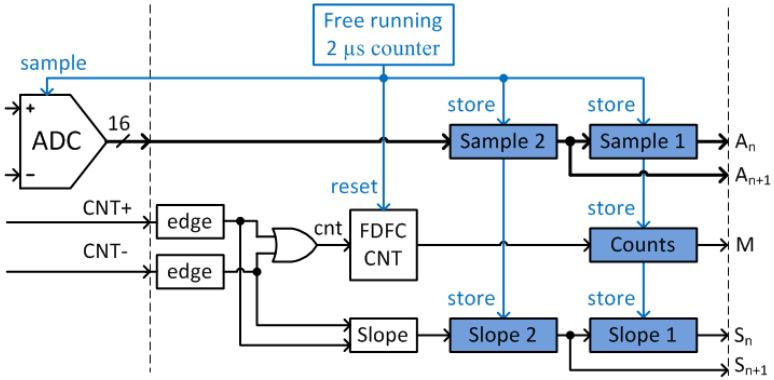
- The number of accumulated counts are combined with the ΔADC values to calculate the integrated loss over a 2 µs period.
- Most of the operations are handled by the FPGA. That is,
  - Defines start and stop of the acquisition period
  - Keeps a count of the number of pulses occurred in the acquisition period,
  - Clocks the ADC circuitries and makes differences of the recorded ADC values
  - Finally, processes the data and provides the 2 µs integral per channel

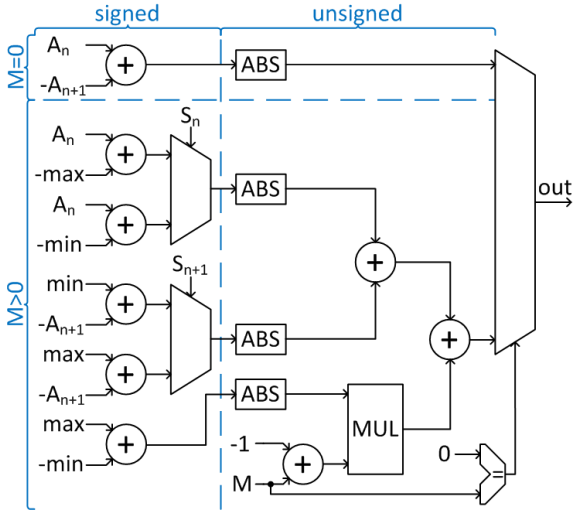
FDFC: Pre-Processing Algorithm



Case	Calculation
1.1	A_{n+1}-A_n
1.2	A_n-A_{n+1}
2.1	(max-A_n) + (max-A_{n+1})
2.2	(A_n-min) + (A_{n+1}-min)
3.1	(max-A_n) + (max-A_{n+1}) + (M-1) * (max-min)
3.2	(A_n-min) + (A_{n+1}-min) + (M-1) * (max-min)
4.1	(A_n-min) + (max-A_{n+1}) + (M-1) * (max-min)
4.2	(max-A_n) + (A_{n+1}-min) + (M-1) * (max-min)

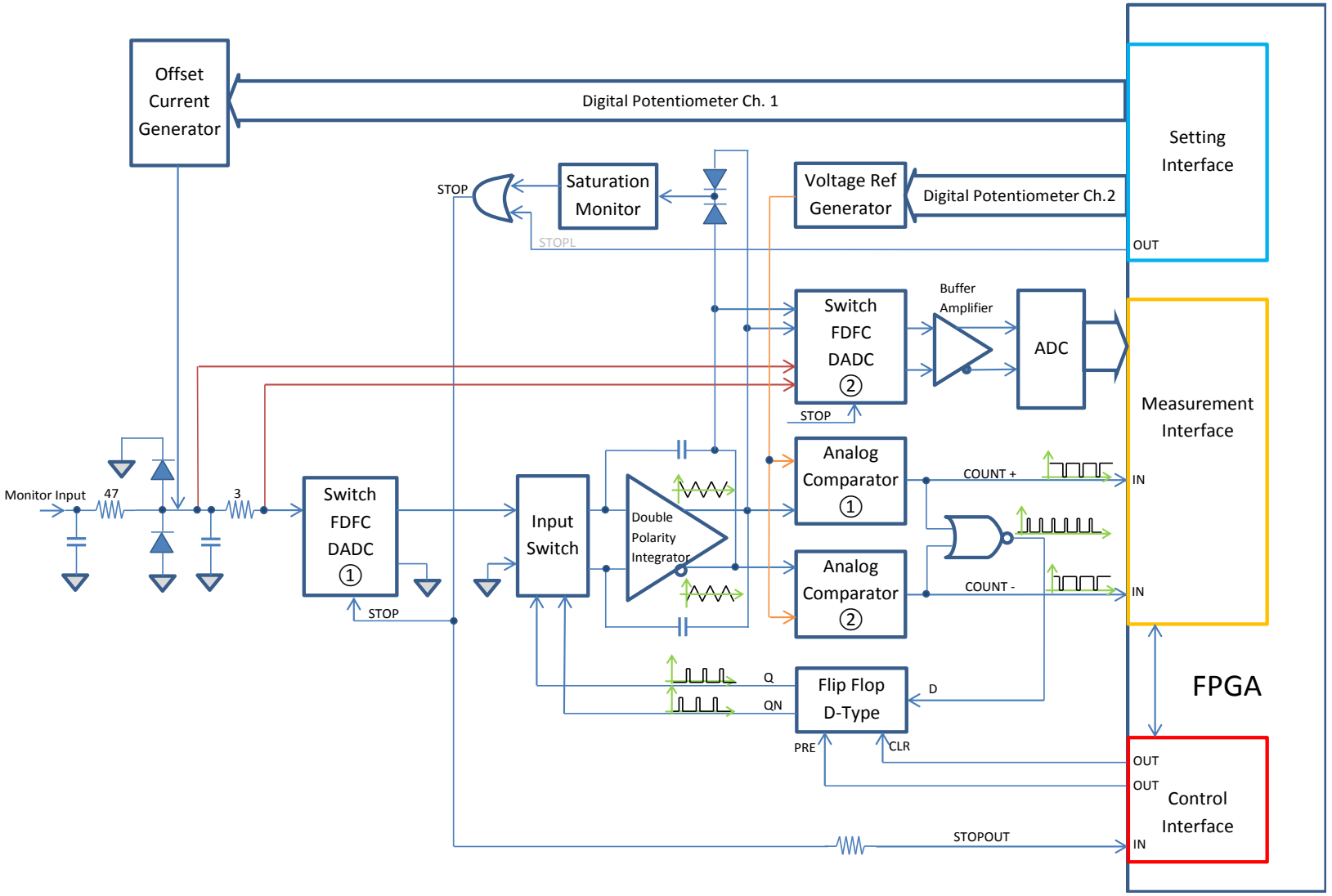
- In order to evaluate the integral between two samples the algorithm needs to cover eight cases.
- By tracking the slope and using the absolute value of the differences the realisation in the FPGA is significantly optimised.





- The above is for an ideal circuit. In reality an additional stage is introduced to compensate for component tolerances, switching delays, and other effects.

Acquisition channel Block Diagram

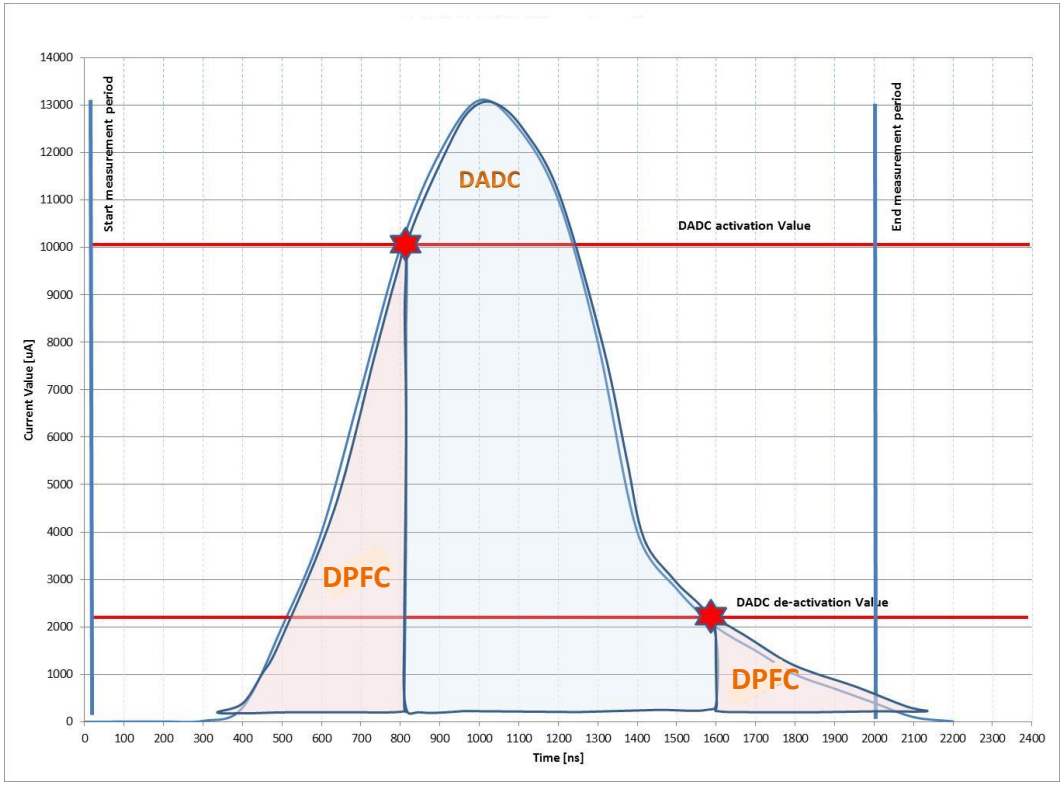


Acquisition principle (FDFC & DADC)

The input channel circuit is able to measure current input from 10pA to 200mA.

The measurement of the input current is performed by two techniques:

1) Dual Polarity Current to Frequency Converter (FDFC) operates in the range **10pA to 30mA**
2) Direct ADC acquisition (DADC) usable in the range **20.3µA to 200mA**



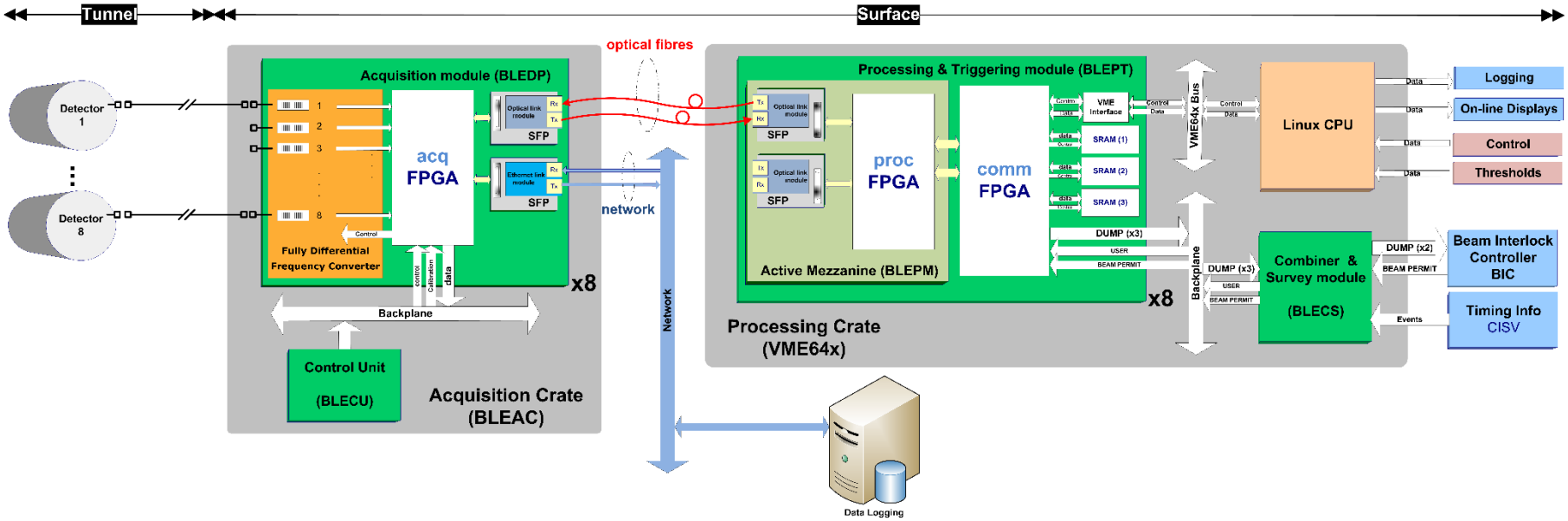
No gain change required:

The switch between the 2 ranges is managed by the *FPGA*.

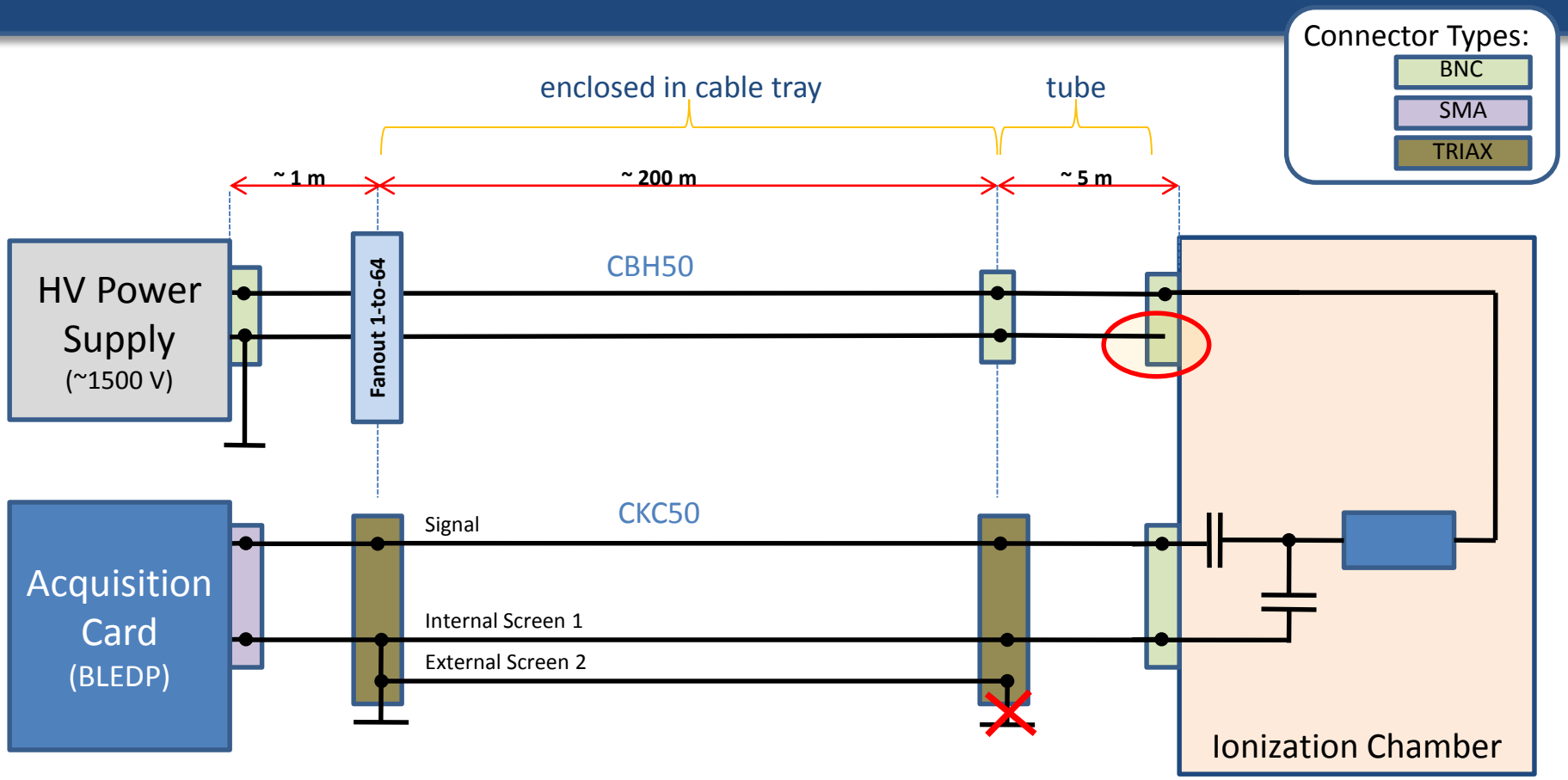
- If the maximum FDFC counts is reached, the FPGA switches the circuit to the DADC mode.
- When the value of the DADC falls below a threshold, the FPGA switches the circuit to the FDFC mode.
- The sum of all parts is calculated in the FPGA and transmitted as a 2 us sample.

SYSTEM OVERVIEW

System Architecture



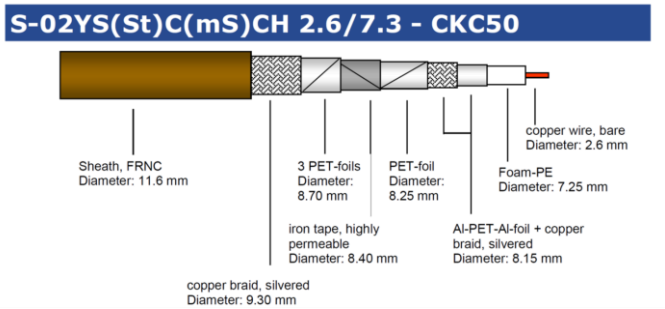
Cabling Overview



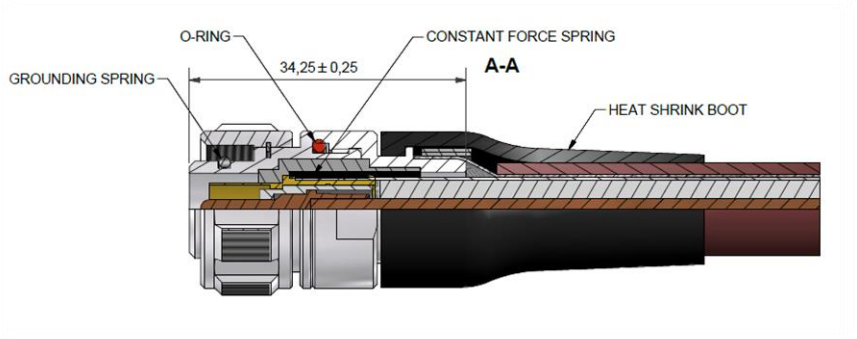
- Single HV cable to each detector using a fanout module.
- Screen of detector power cable is open on the IC side to assure there is **no ground loop**.
- Internal screen to **shield low frequency** noise (GND only on electronics side, IC is floating).
- External screen to **shield high frequency** noise (and atm not grounded at tunel side).

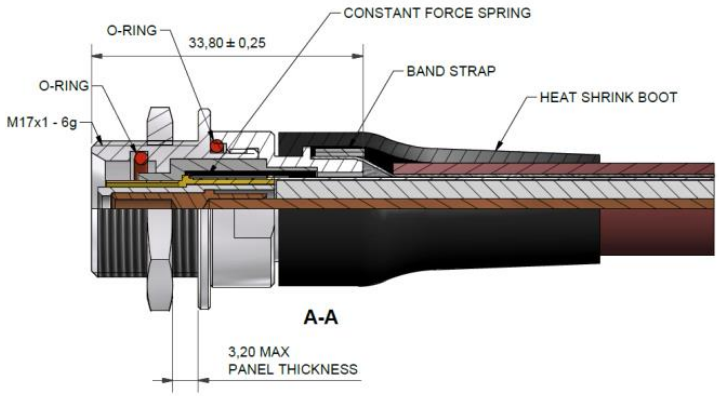
Cabling Overview

- HV cable: CBH50
- Signal cable: custom-made coaxial double shielded CKC50

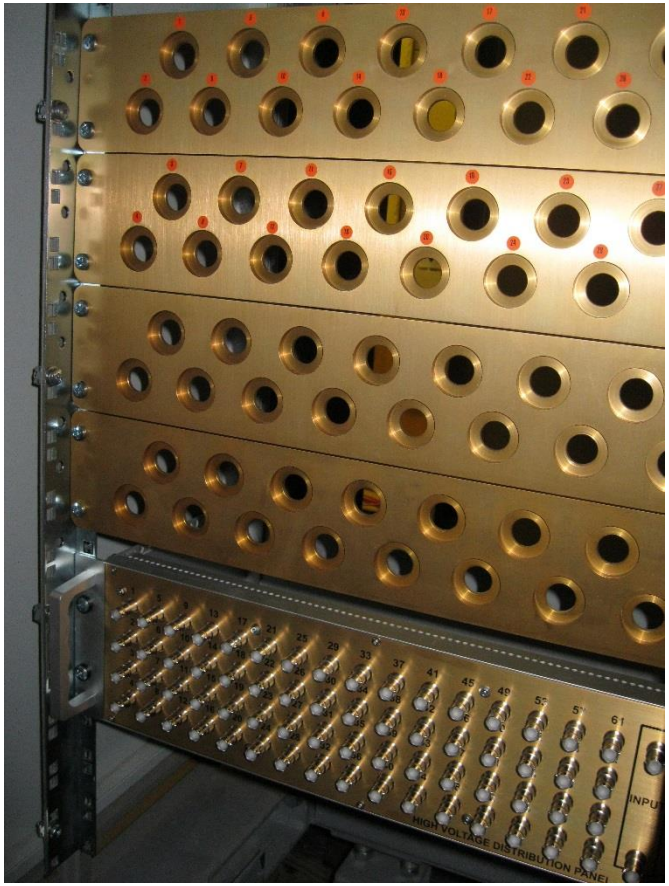


- Connectors/Plugs: custom-made triaxial





Cable Management



Signal Cable panel &
HV distribution

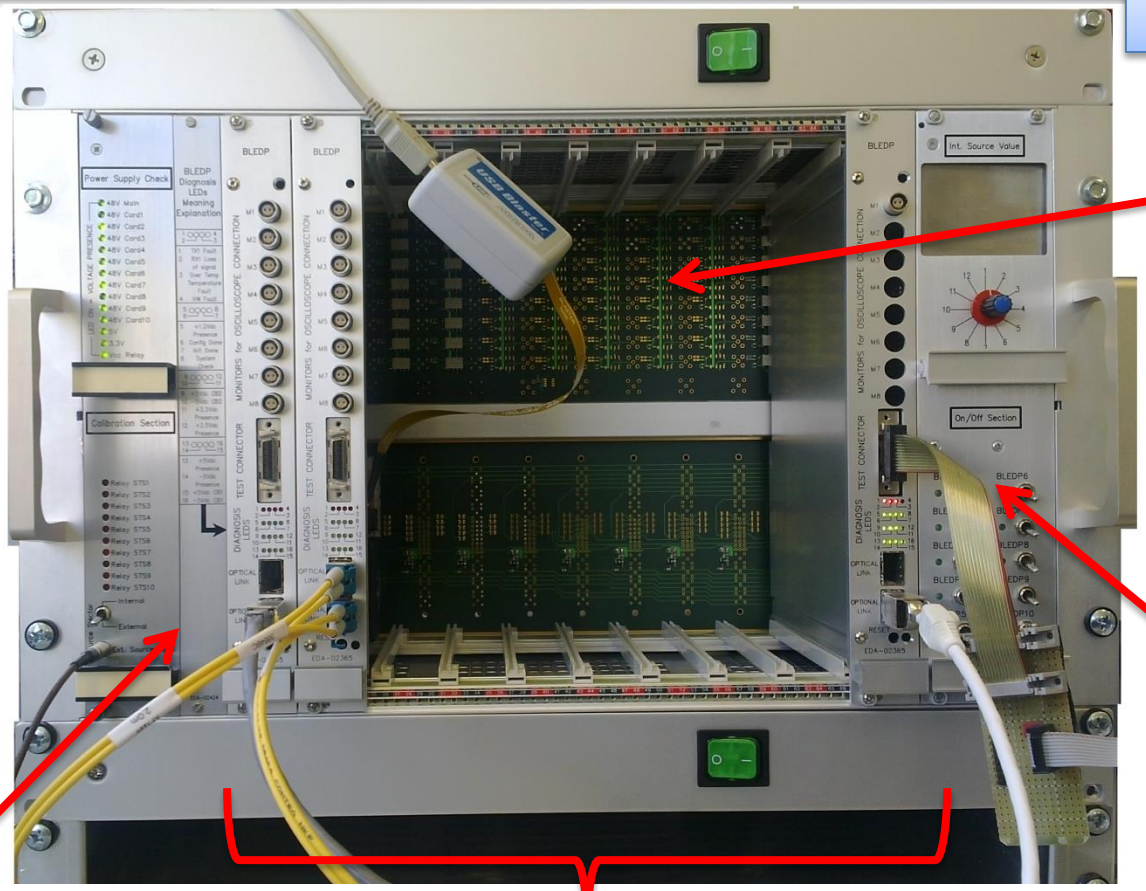
Signal Cables

HV Cables

ELECTRONICS

Acquisition Crate

Production completed



Custom Backplane
Support 64 connectors and relays for the input channels and distribute signals

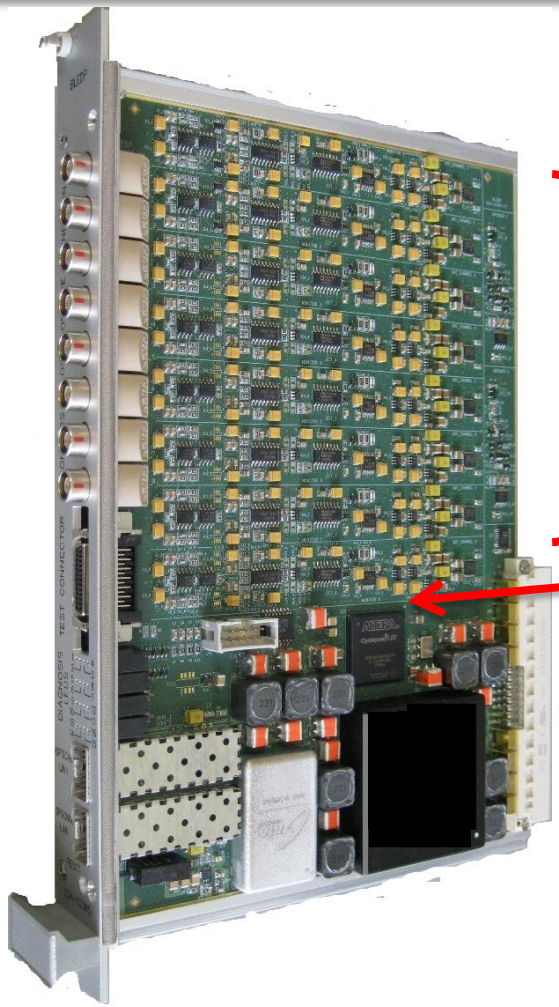
Control Unit
Later version w/ advanced remote functions

Main panel
- Ref. current Input
- LEDs
- Power switch

Acquisition module (BLEDP)
Up to 8 modules with 8 channel each

Acquisition module (BLEDP)

Currently in production



Acquisition
digitisation of 8 channels

FPGA
Altera Cyclone IV

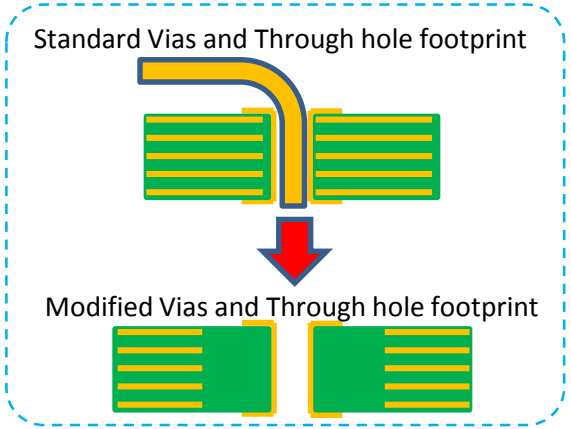
JTAG connection
Local programming and diagnostics

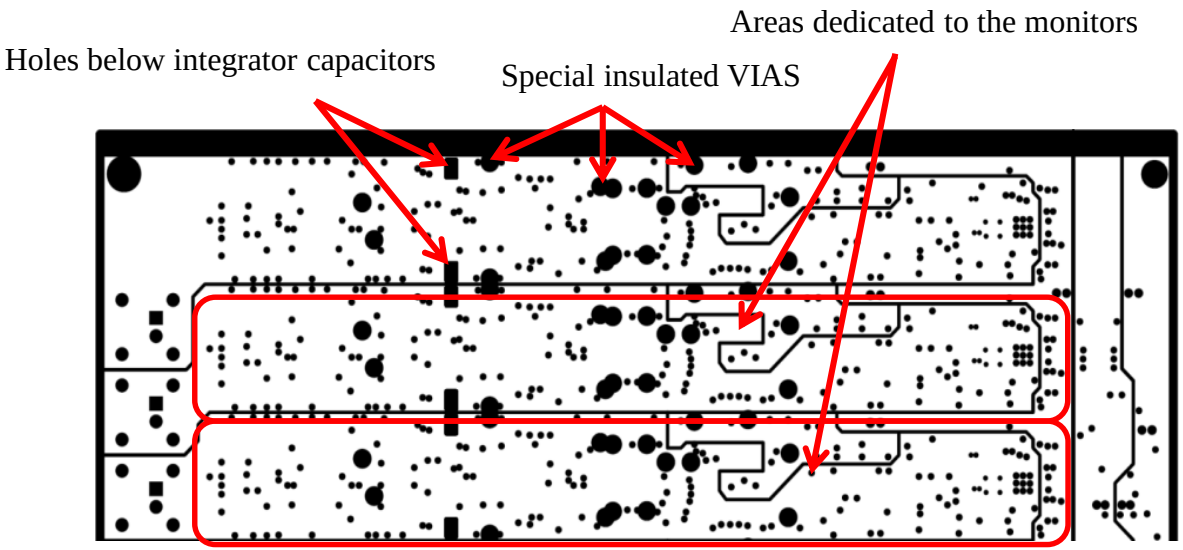
Backplane connection
Analogue inputs, power and control

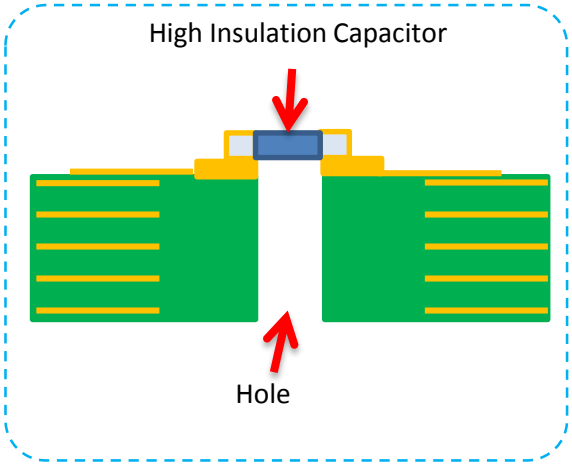
SFP connectors
Gigabit optical and/or Ethernet links

BLEDP Optimisation

- Improve the insulation between input lines and other signals e.g. power supplies.
- This has been done by:
  - creating special VIAS,
  - optimising routing paths and
  - creating holes below the integration capacitor.
  - several ground areas have been created.







Processing Electronics

- Processing Mezzanine
  - New design to match the acquisition modules
  - 2 SFP modules (gigabit Optical links and Ethernet)
  - Cyclone IV (150K logic elements) FPGA
- Carrier VME64x modules
  - Generic BI card, i.e. DAB64x
- VME crates with BI custom backplane
  - Broadcast of timing events to the modules
  - Daisy-chain of beam permit signals
  - Same as LHC system

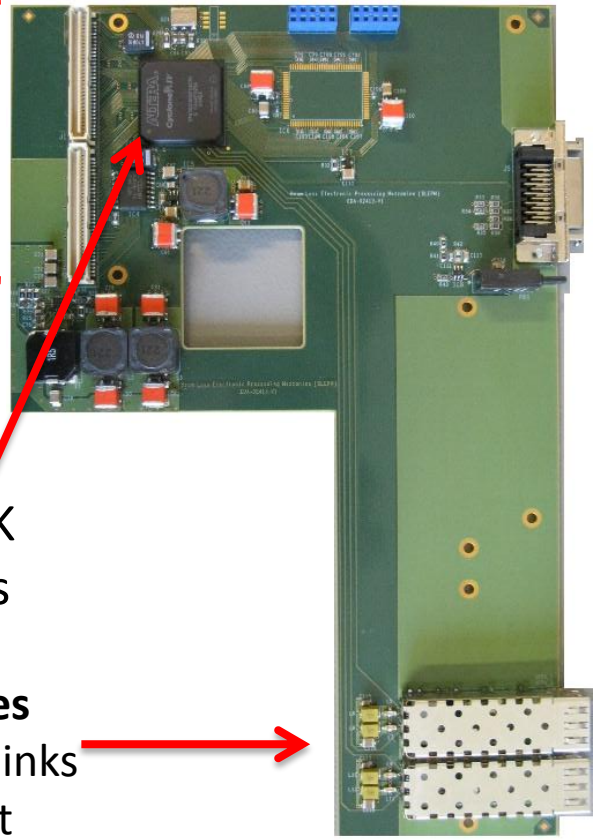
Processing & Threshold Comparator

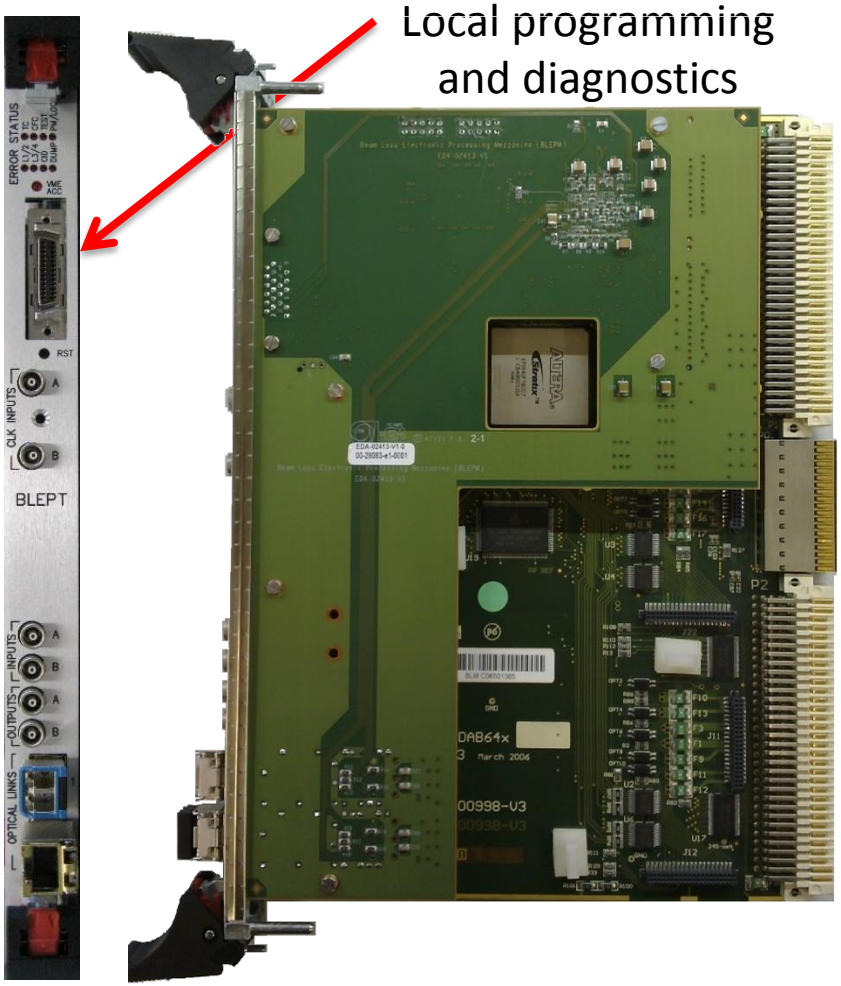
JTAG connection
Local programming and diagnostics

Connectors to the mainboard

FPGA
Cyclone IV 150K logic elements

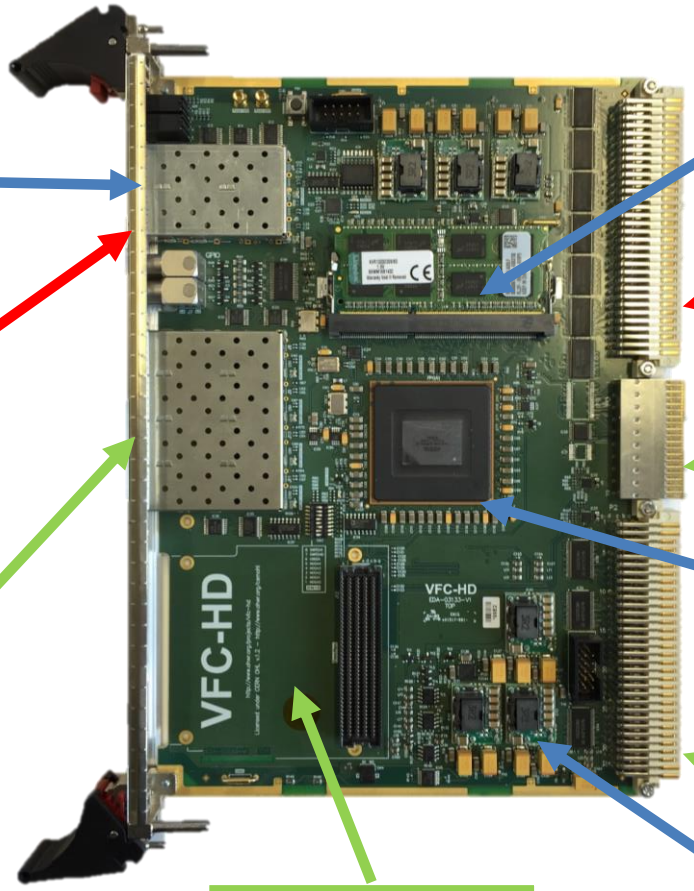
2 SFP modules
Gigabit Optical links and Ethernet





VFC-HD module

Next generation of generic CERN BI processing modules in production



Beam Synchronous Timing

Ethernet

4 SFP for fast connections to the Front-ends

DDR3

VME64x interface

P0 User defined connection

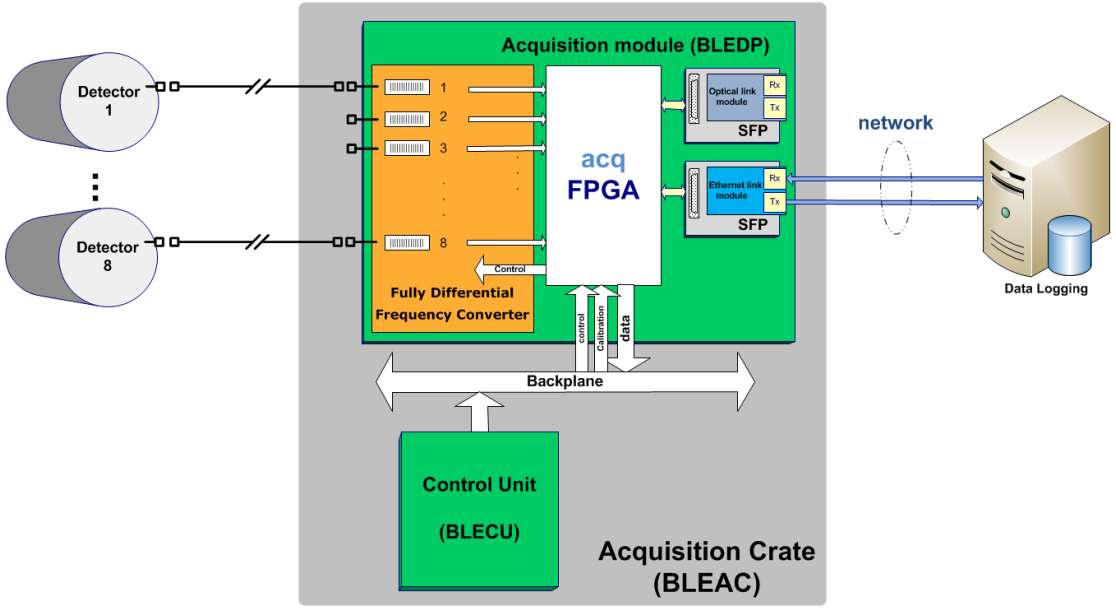
ARRIA V FPGA

Rear Transition Module connection

CERN Power Supplies

HPC-FMC slot

System for Verification



- Need to record all raw data
- Analyse data offline
- Debug & optimise pre-processing algorithm
- Characterise noise & analogue circuit.

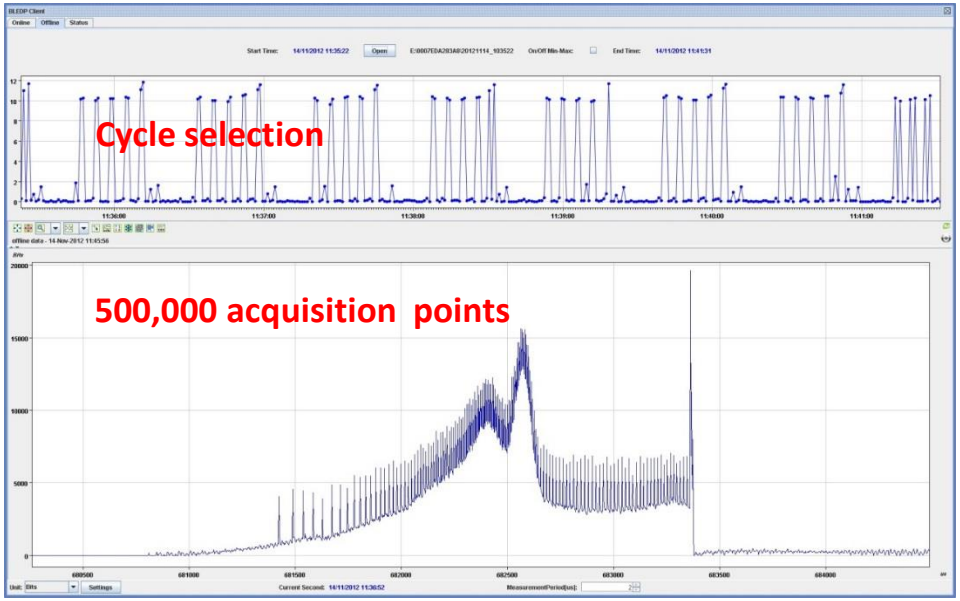
- Added a gigabit Ethernet module and connect to the network
- Developed TCP/IP and UDP stacks in the FPGA firmware -> NIOSII softcore
- Developed a server to be included in the FPGA -> compiled C++
  - accept commands, prepare data requested and transmit
- Developed client applications in Java, Python and C
  - send commands, store and display data

Stand-alone/Ethernet version

Front view

Rear view

- Ethernet-based version of the system
- Very powerful for
  - verification,
  - commissioning and
  - fine observations



INSTALLATION OVERVIEW

Pictures of the installation

Separated enclosed cable tray

Metallic cable tube for the last few meters

Fans on the rack top

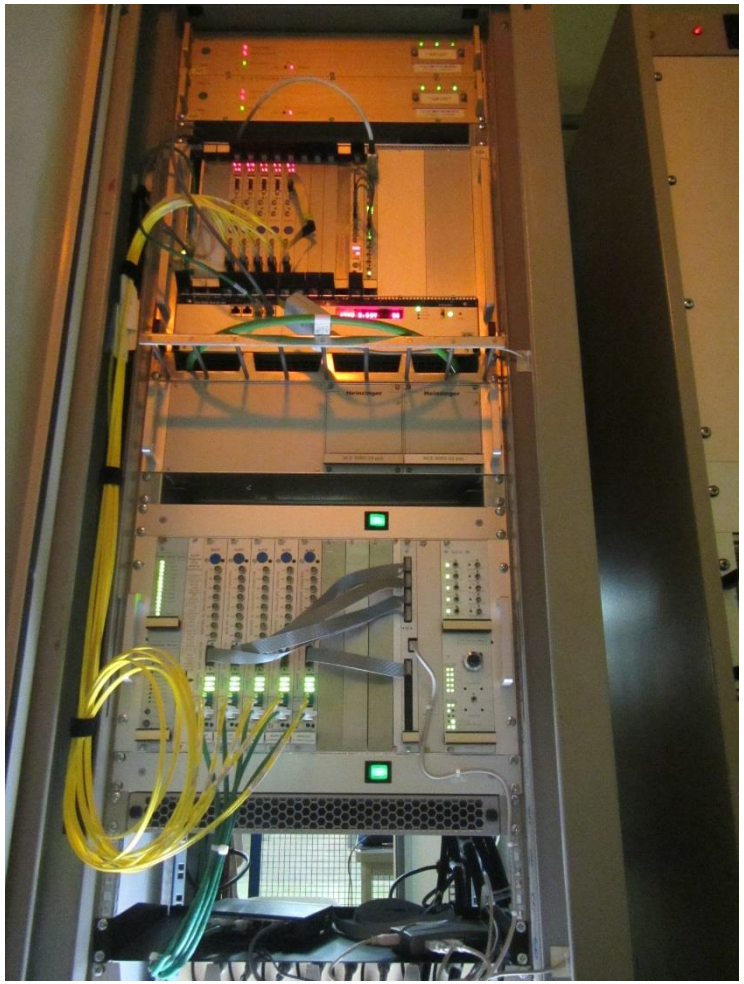
Enclosed and extended front for cables and fibres

Standard and Uninterrupted Power Supply connections

Rack includes:

- Acquisition crate
- Processing (VME) crate
- HV Power supply for the detectors
- User Interface to BIS (i.e. CIBU)

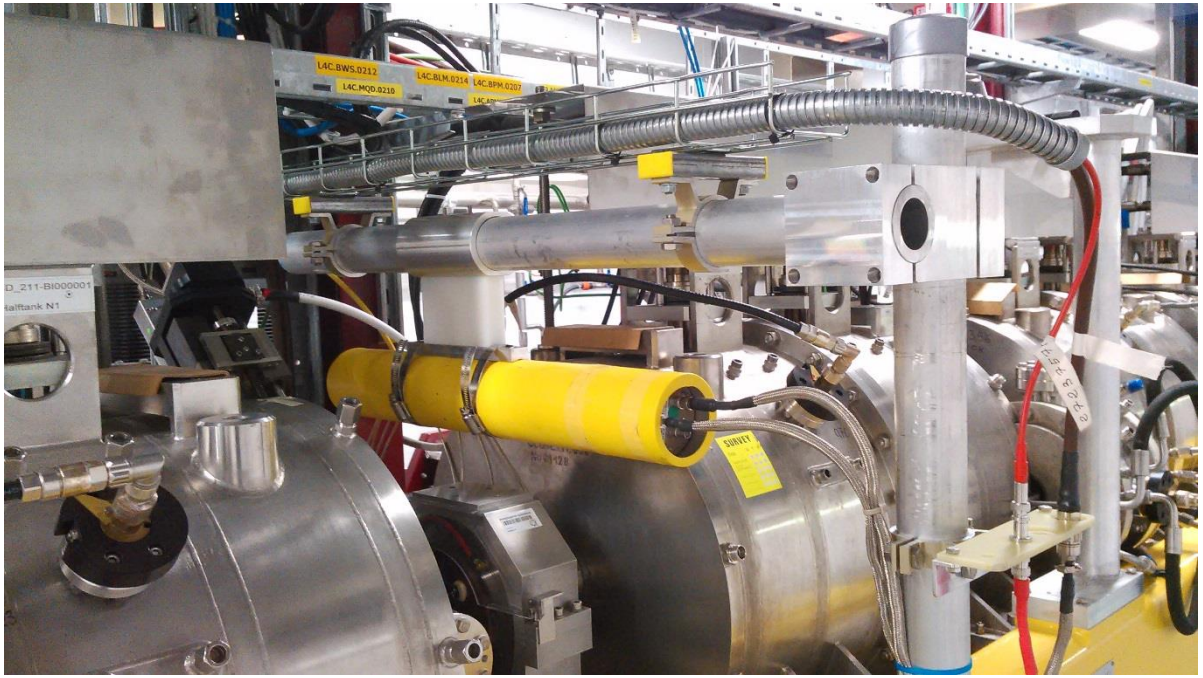
Rack Management



LINAC4: Info

- 11 ICs in the machine line and
- 14 ICs in the transfer line

LINAC4: Supports



Machine line

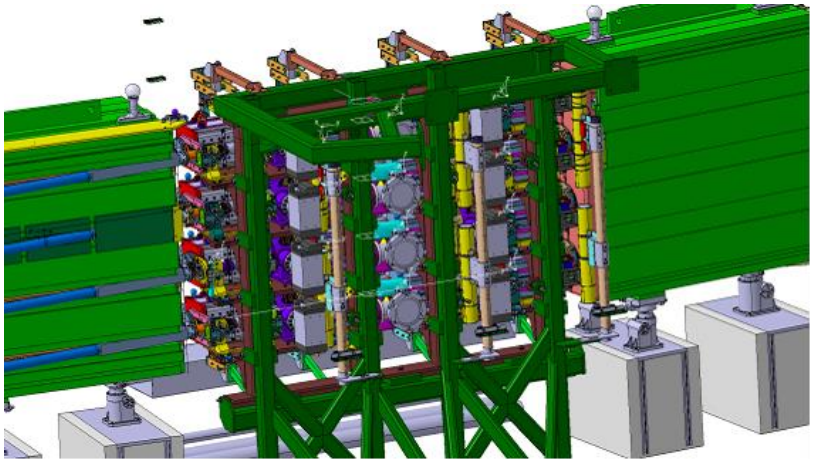
Dump and Transfer line

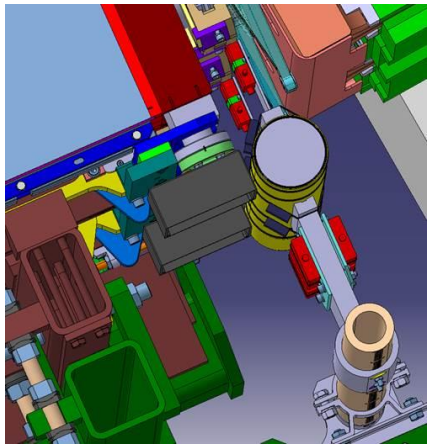
PSB: Info

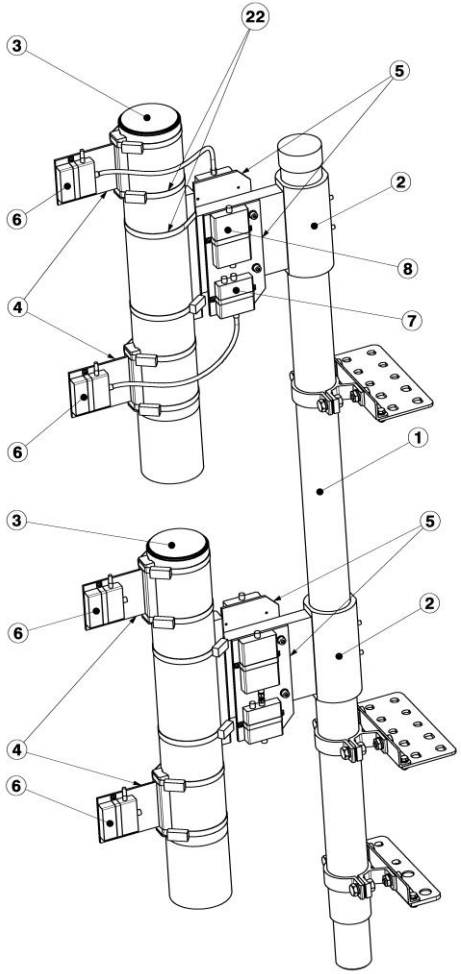
Machine/Area		Channels	Cables	Detector Type
PSB	Ring (L2 sections)	32	64	LHC-IC
	Ring (L3 sections)	32	64	FIC
	H- and BI lines	18	36	LHC-IC
	H-	8	40	Diamonds
	Extraction lines	28	56	LHC-IC

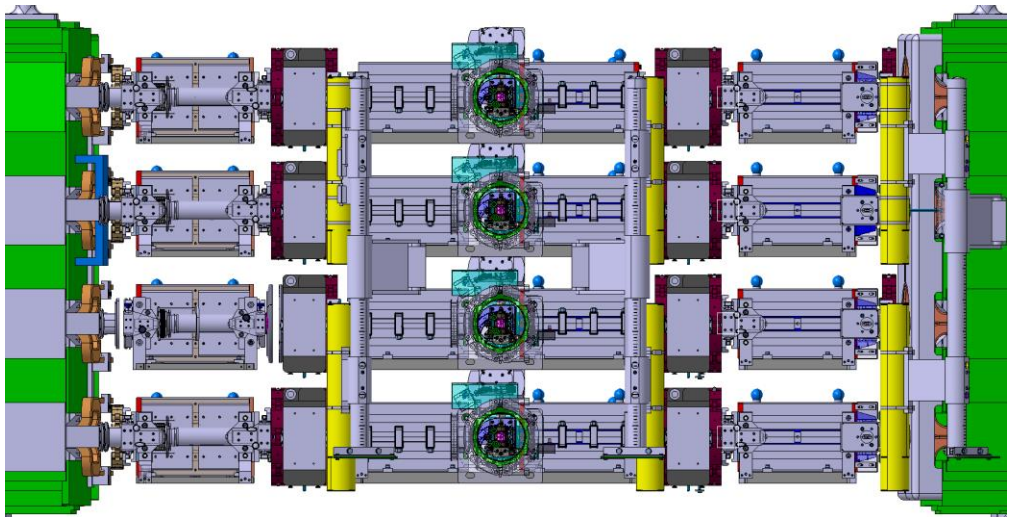
- Detectors:
  - 8 Diamonds with amplification and splitter stages
  - 32 Flat Ionisation Champers (FIC)
  - 72 LHC-type Ionisation Champers
- Cabling
  - Ring L2 sections complete
  - Remaining installation is planned for 2017
- Supports:
  - Common design for the H- detectors (ICs and Diamonds)
  - Transfer lines have not been considered yet

PSB Injection: IC & Diamond Support









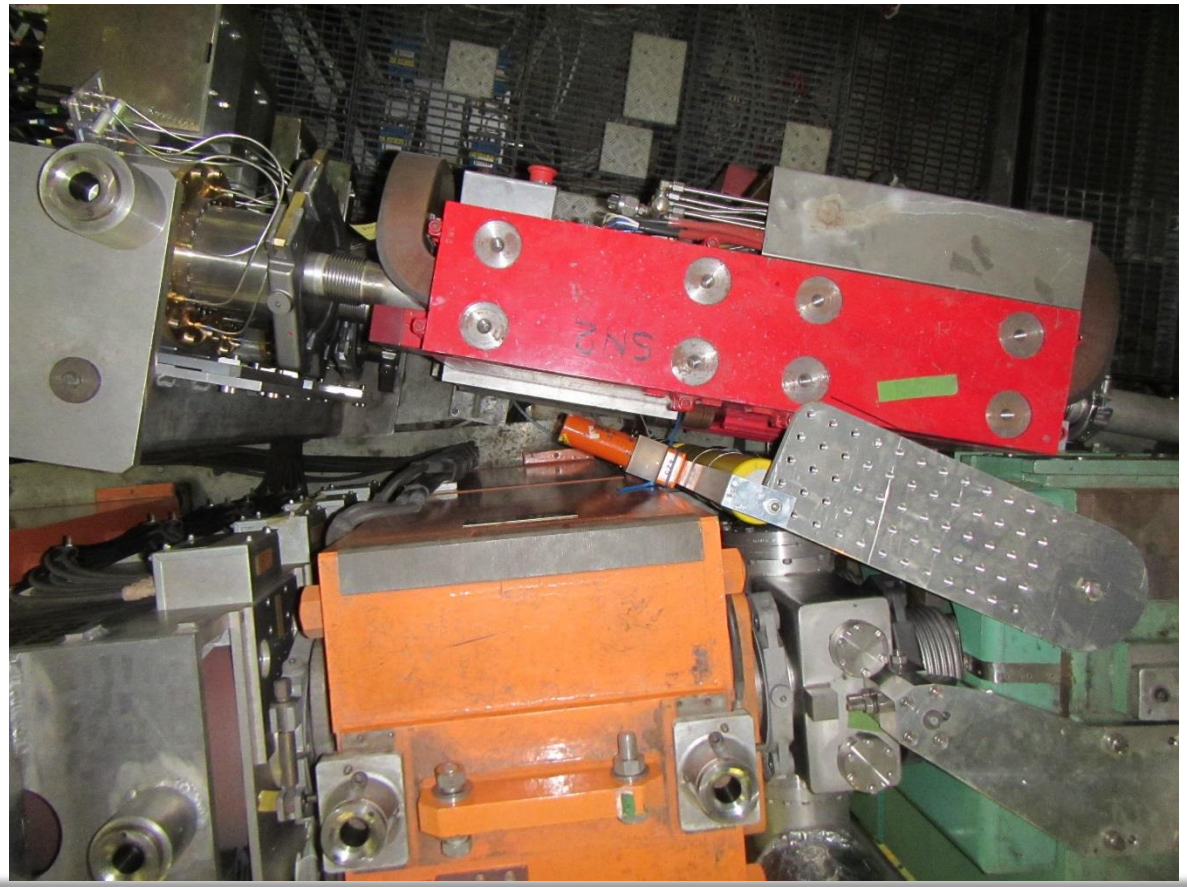
The new H^- charge-exchange injection system

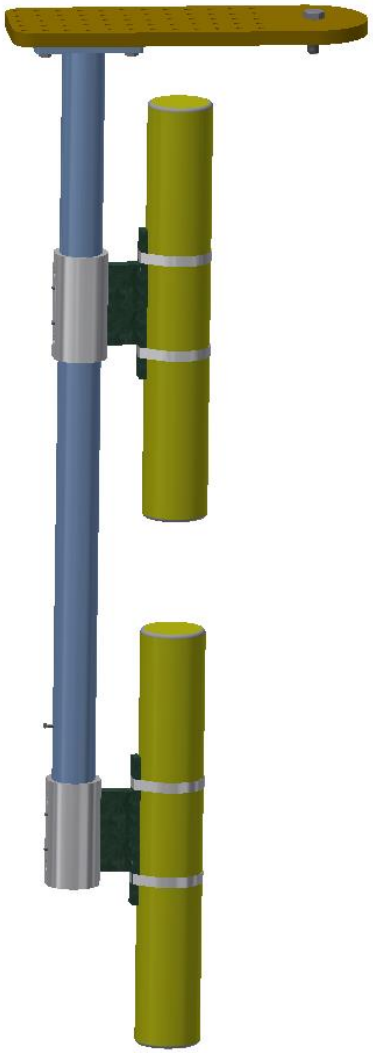
PSB Ring: IC Detector Support

- Very tight integration.
- Had to verify all locations; no interference / obstruction to other systems.

PSB Ring/Ejection: IC Custom support

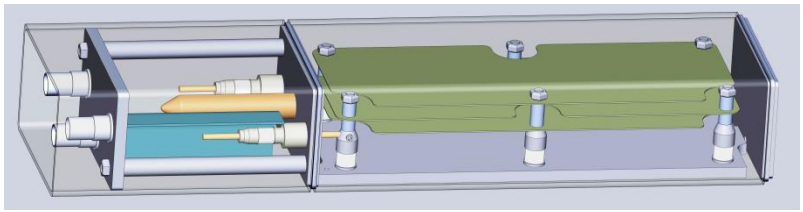
- No space to add the detector on the inside of the ring
- ACEMs mounted on the same plate

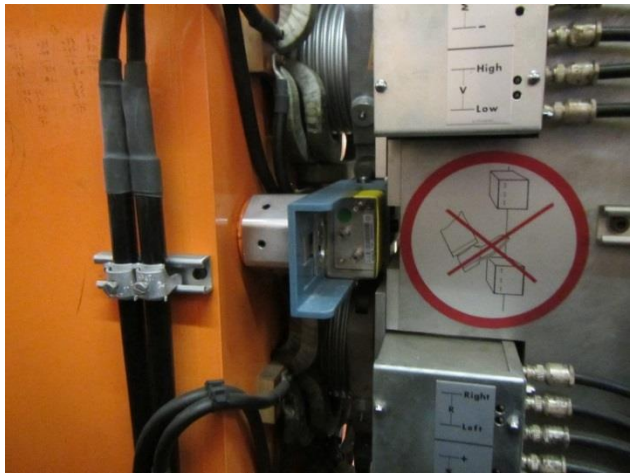




PSB Ring: FIC Detectors

- Rectangular detectors (FIC) placed between beam pipes
- Support mounts on the magnet
- Isolation tests performed



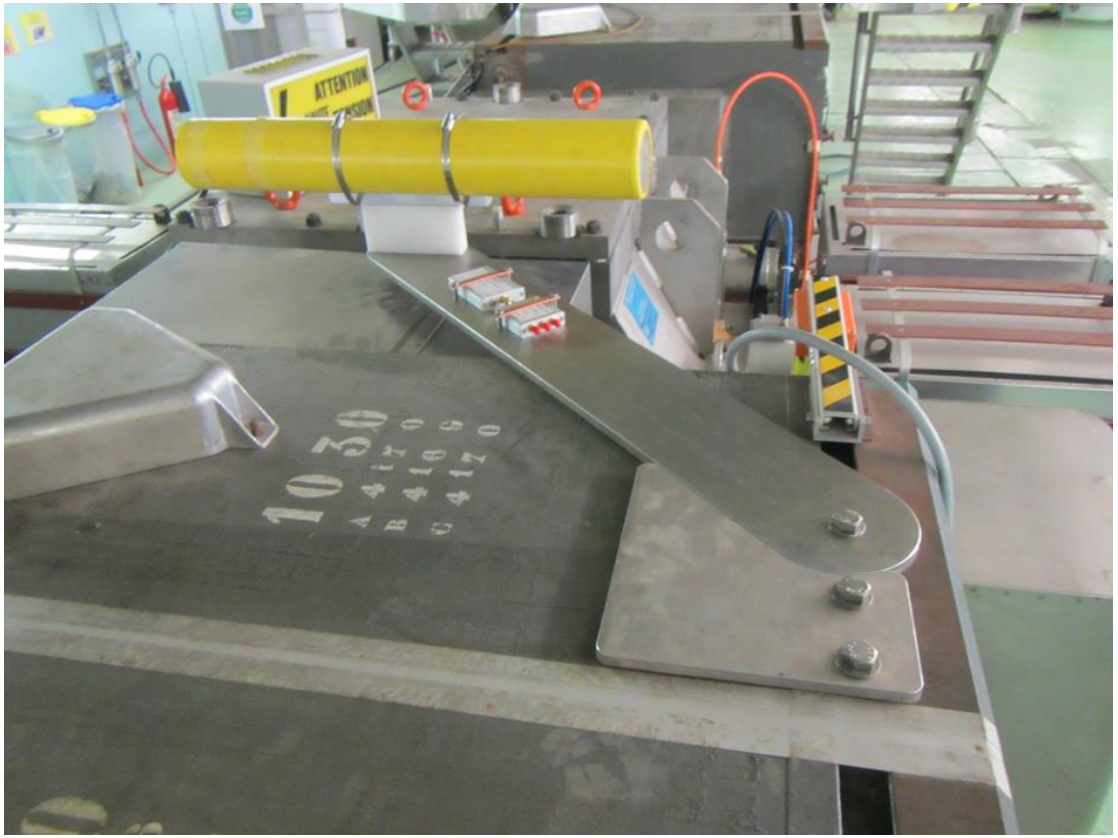


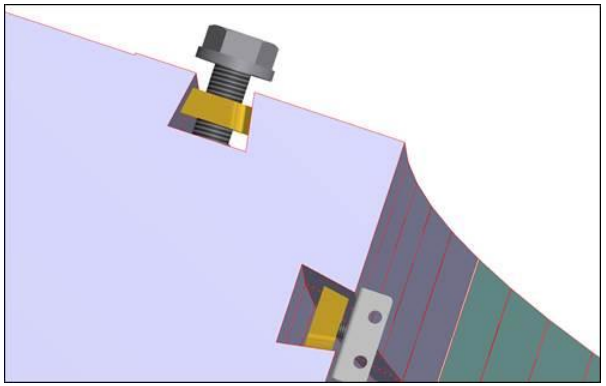
PS Info

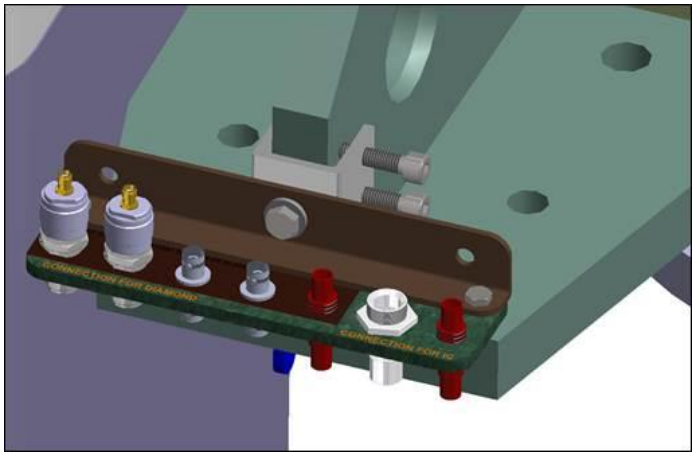
Machine/Area		Channels	Cables	Detector Type
PS	Ring	100	200	LHC-IC
	Ring (observation)	17	85	Diamond
	Transfer Lines	51	102	LHC-IC

- Detectors:
  - 17 Diamonds with amplification and splitter stages
  - 151 ICs are in production (delivery expected end 2016)
- Cabling installation is planned for 2017
- Supports:
  - Common design for the ring detectors (ICs and Diamonds)
  - Transfer lines have not been considered yet

PS Ring Support







- Common support for IC and Diamond

SUMMARY

Summarising

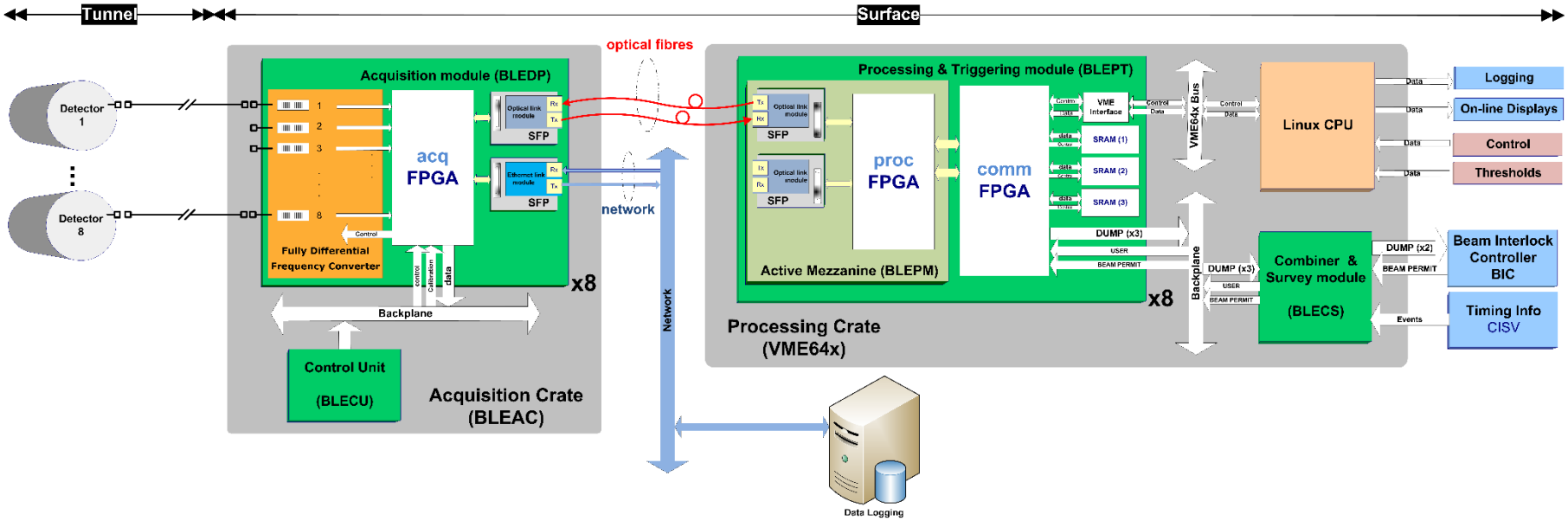
- Reliable tunnel installation
  - Monitors will be mostly Ionisation Chamber type
  - High immunity to EMI with special cables, connectors and enclosed cabletrays
  - Special attention given to grounding and isolation
- High performance acquisition electronics
  - Automatic range selection
  - Dynamic range = 10^{11}
  - In-system calibration mode (will have remote execution in the future)
- Modular processing electronics
  - High availability of resources (~350'000 Logic Elements)
  - Embedded bidirectional gigabit links
  - Additional gigabit Ethernet link (for dedicated measurements)
  - Future plan for upgrade using the new BI processing module
- Production and installation is expected to be completed mid. 2017
- Test-benches for verification, software development and measurements
- Beam measurements in October

THANK YOU

RESERVED SLIDES

Status of Development

System Overview

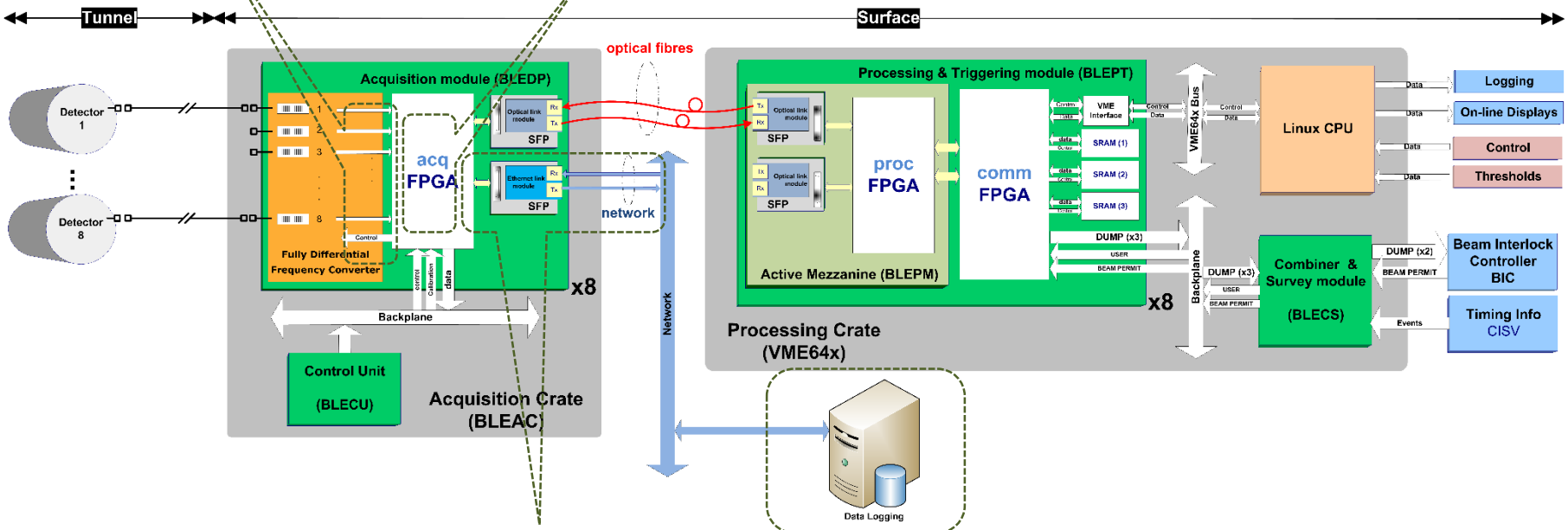


Status of Development

FPGA Development

Acquisition & Control
on-going

Data Pre-Processing
complete



Gigabit Ethernet Link
complete

Stand-alone Application
complete

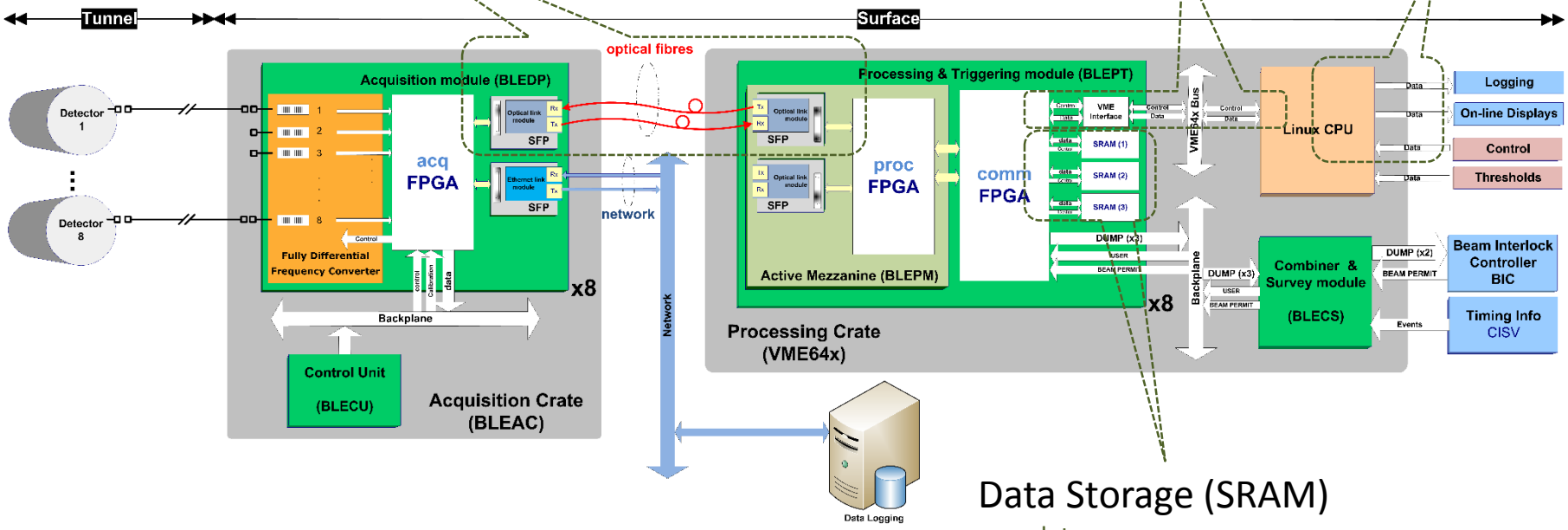
Status of Development

FPGA Development

Gigabit Optical Link
complete

VME Comm.
complete

FESA Class API
complete



Data Storage (SRAM)
complete

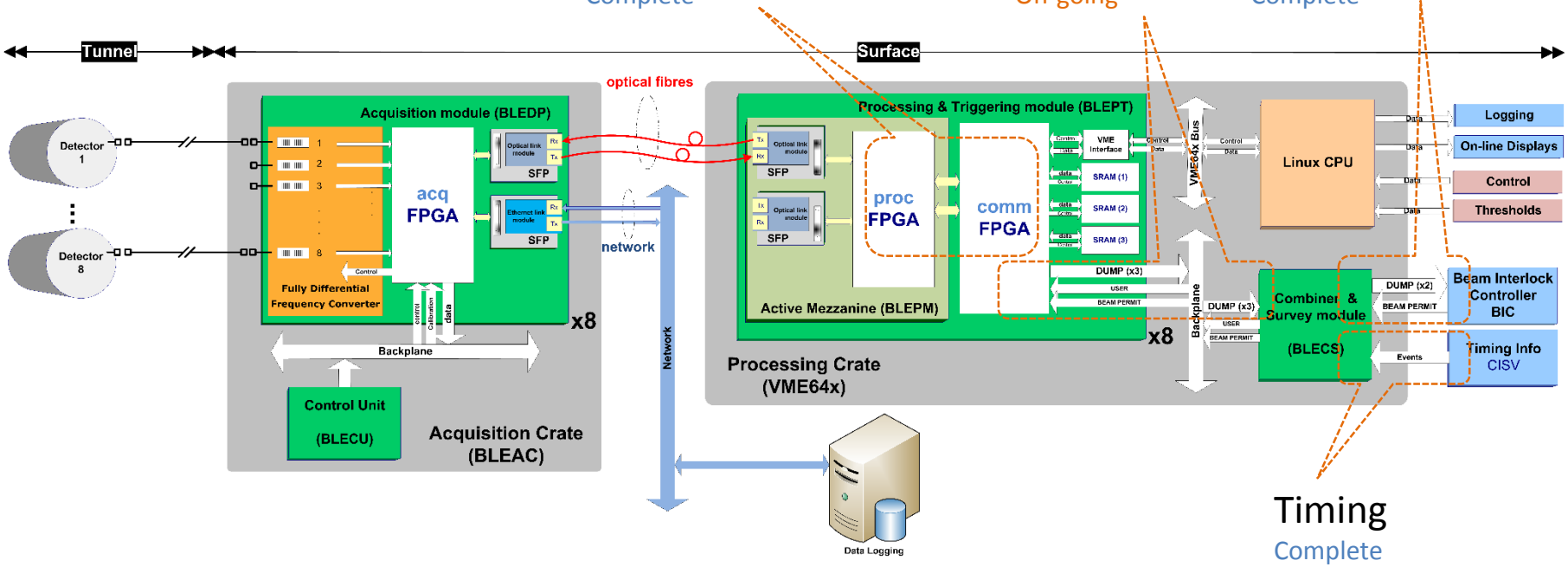
Status of Development

FPGA Development

Data Processing
Complete

Interlocks
On-going

CIBU Connection
Complete



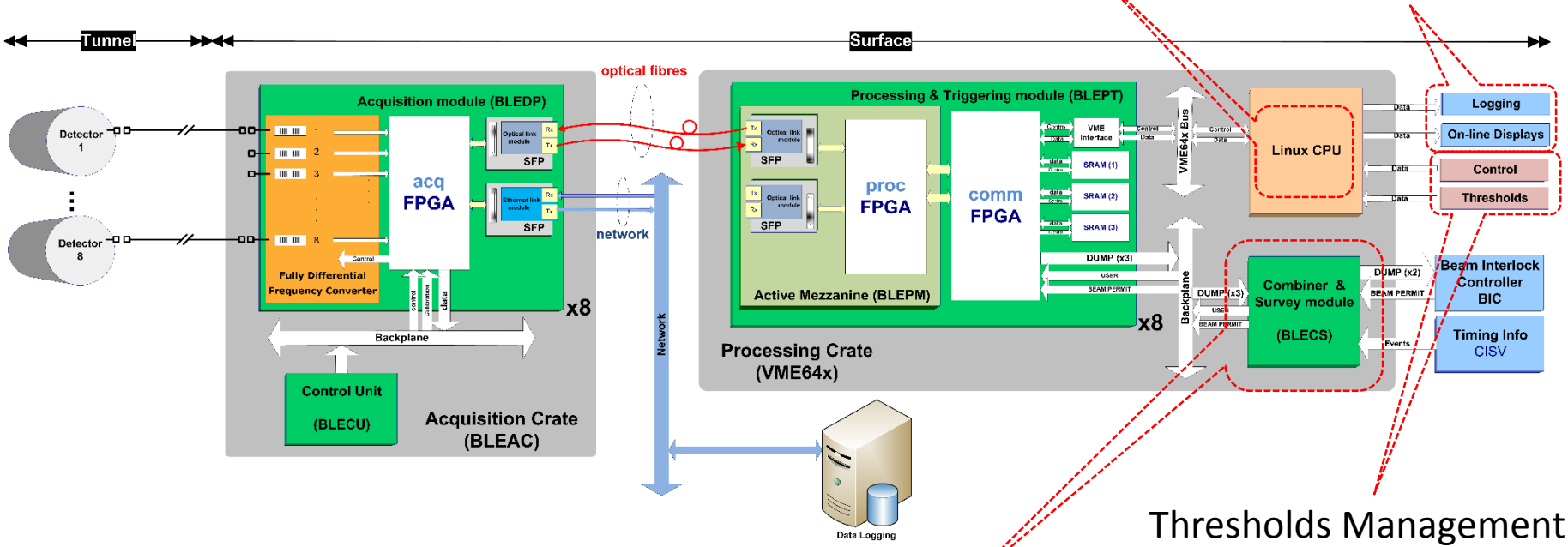
Timing
Complete

Status of Development

FPGA Development

FESA Server
complete

Logging Database
complete



Thresholds Management
Not Started

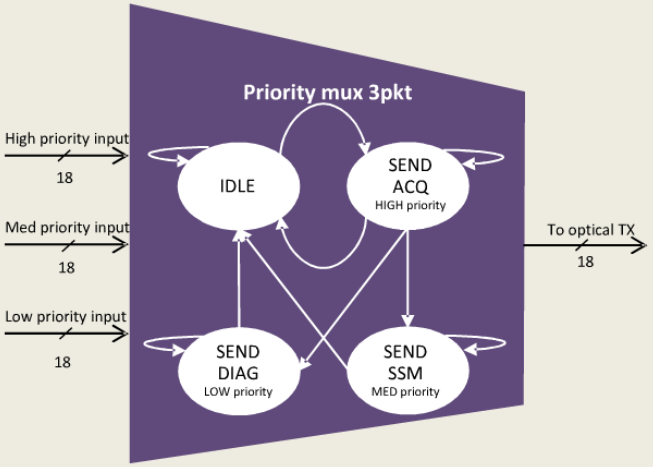
System Supervision
On-going

Priority Multiplexer

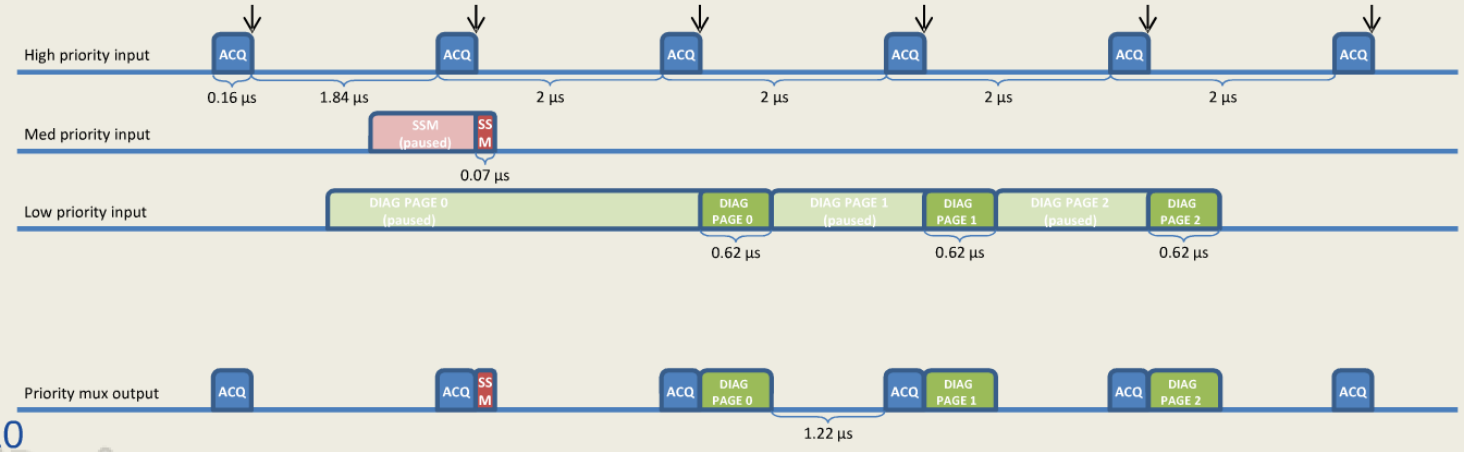
Inputs of the multiplexer:

- Acquisition packet 16 words
- SSM packet 7..9 words
- Diagnostic packet 62 words

priority



ACQ packet every **2 us**
Between two ACQ packets **only** one of the other type of packet allowed



Diagnostic Reader

	BLEDP	BLEPM	DAB64x
• Geographical address • Firmware version • Chid ID • Temperature	✓	✓	✓

• Humidity
• SFP 1-2
  • Serial number
  • Part number
  • Temperature / VCC
  • TX Power / RX Power
  • Warnings / TX Bias
	✓	✓	

• Current consumption • Power • Relays • DAC offset current • DAC analog threshold • Saturation condition counter • Direct acquisition counter	✓		
	35 interfaces 296 words	7 interfaces 108 words	4 interfaces 18 words

Diagnostic Data Example