Warm Interface Board

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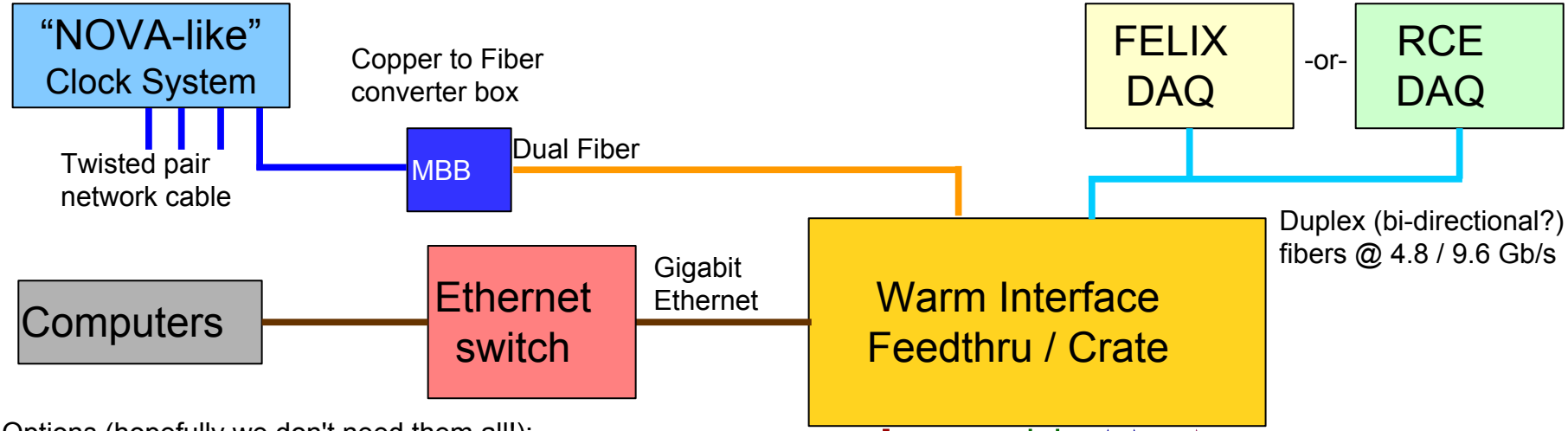
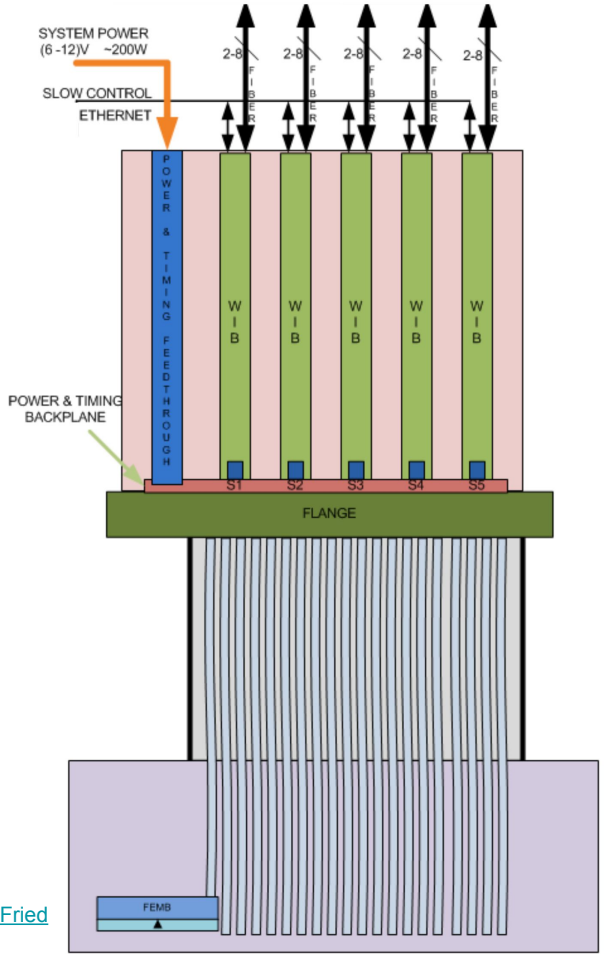
ProtoDUNE TPC Electronics Overview



Options (hopefully we don't need them all!):

- Clock / control inputs from:
  - Clock system
  - FELIX
  - RCE
- Slow controls interface via:
  - Ethernet (software, direct to WIB)
  - FELIX via DAQ fiber
  - RCE via DAQ fiber
- DC Power
  - All voltages regulated in WiB / cold
  - External regulators in power supplies

SBND Adapted Electronics



Power & Timing Backplane (PTB):

- Provides LV power distribution to WIBs
- Provides point-to-point timing between PTC and WIBs.
- Supports 5 WIBs

Power & Timing Card (PTC):

- Provides timing and control over front panel fibers.
- Front panel LV power input
- Power output over backplane

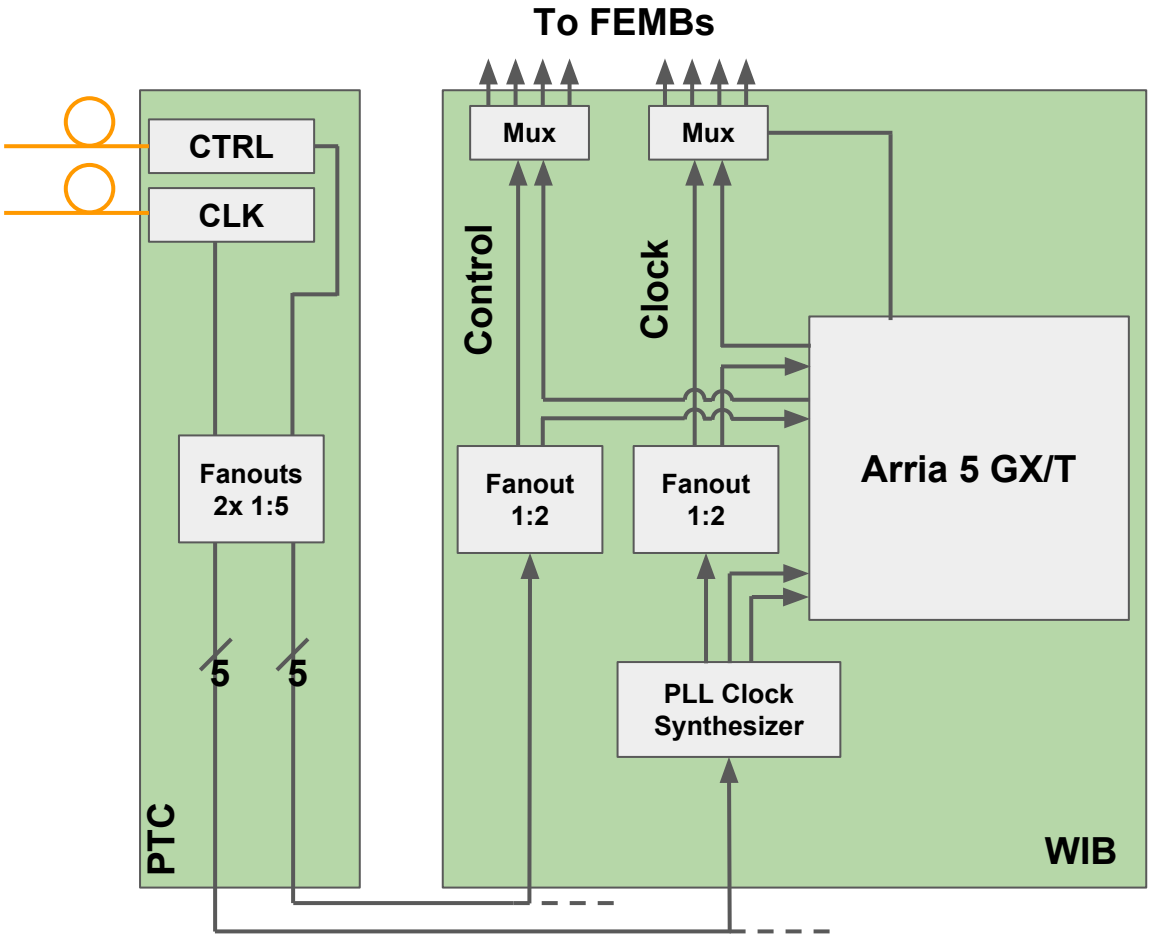
Warm Interface Board (WIB):

- Altera Arria V GX/GT FPGA
- Connects to up to four FEMB boards (16x 1.2Gbps links)
- DAQ Fibers out 4 at 2.5 - 10.3125Gbps.

- Local DC-DC converters for supplying cold power
- Possible front panel power to bypass DC-DC converters

- Configuration (slow control) interface via Gigabit Ethernet
- Debugging access to data via Gigabit Ethernet

WIB Timing and Control



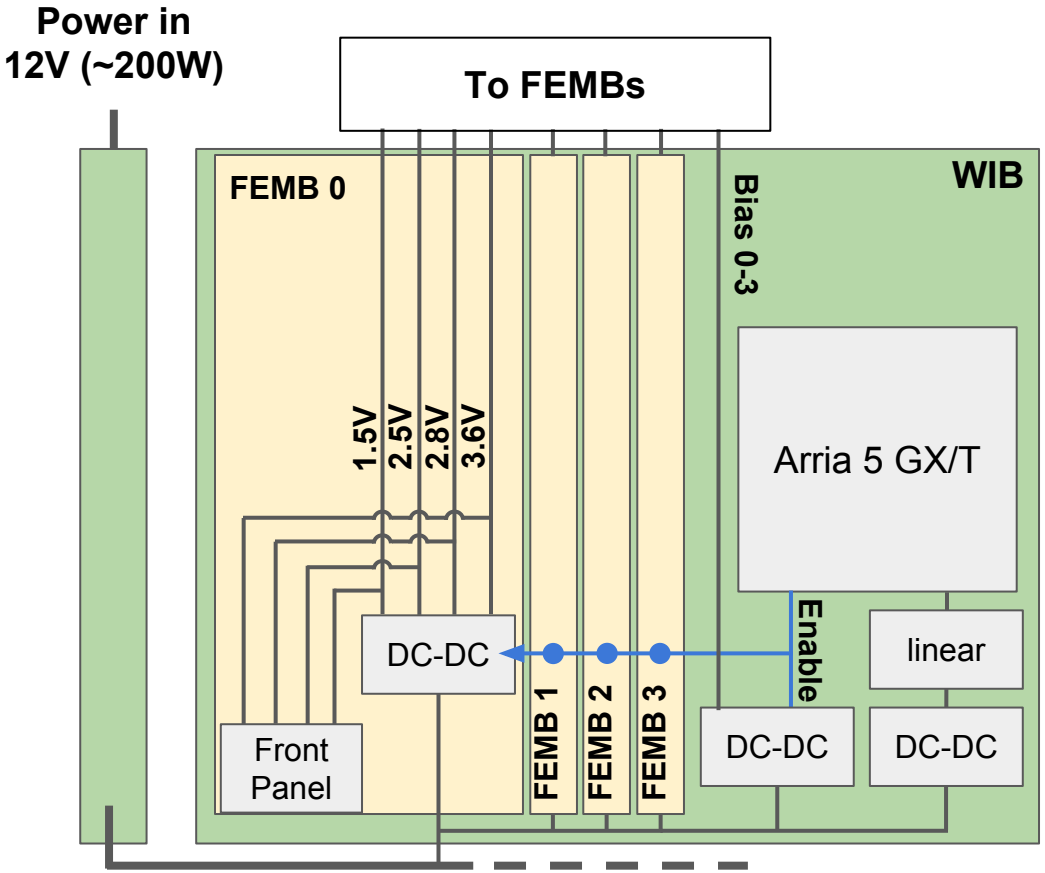
PTC ->WIB:

- Two fibers come in to the PTC, one clock (50Mhz), one control.
- Both are fanned out to each WIB via point-to-point backplane

On WIB:

- PTC clock used to synthesize clocks for the FPGA and the cold.
- Clock and control are fanned out and sent to the FPGA
- Clock and control source can be selected by mux
- Because the clock to the cold must go through a PLL, only the PTC's clock can be used.

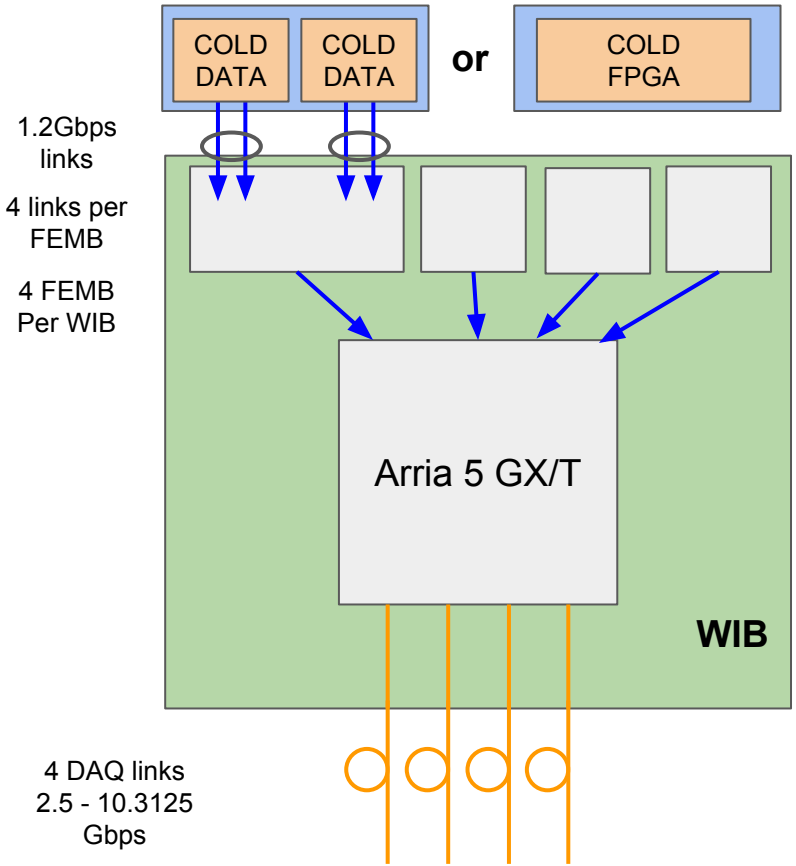
WIB Power



Power for cold:

- Each FEMB requires 1.5V,2.5V,2.8V, 3.6V, and a bias voltage.
- Primary power path:
  - External 12V is sent to the PTC which is then sent to a power bus on the backplane
  - Each WIB uses LTM4644 quad DC-DC converts to generate lower voltages for each FEMB
- Alternate power:
  - Front panel power connector
  - A connection for each power to be supplied by external supplies
  - Current design requires an upgraded connector

WIB DAQ links



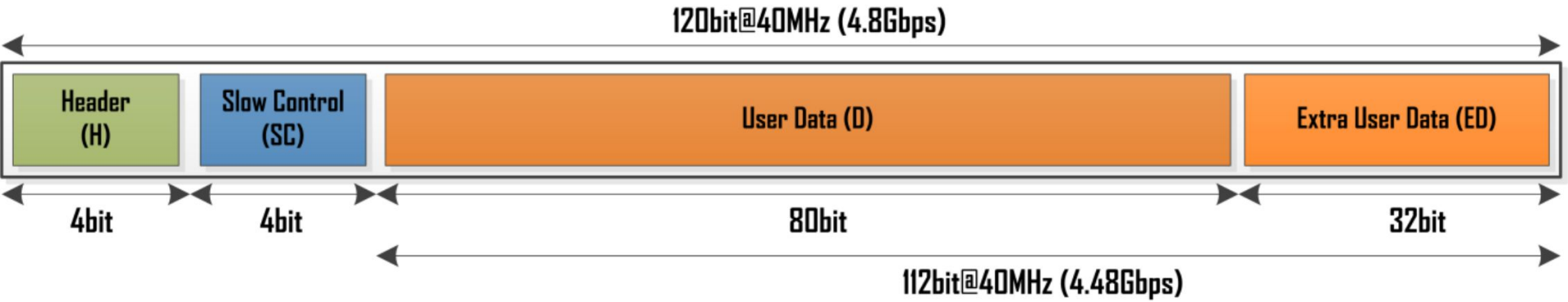
Front-end Motherboard (FEMB):

- proto-DUNE FEMB has one FPGA simulating two COLDDATA ASICs
- Each COLDDATA ASIC sends two 1.2Gbps LVDS streams.
- Each stream has 56 bytes per 500ns, so about 1.8Gbps of actual data per COLDDATA ASIC
- This gives about 3.6Gbps of data per FEMB

WIB:

- The WIB will combine the data from 4 FEMBs.
- The combined data will be sent out either a P-POD or a quad SFP.
- Depending on the FPGA installed, the links can range from 2.5 to 10.3125Gbps
- These links will speak to the FELIX and/or RCE systems.

FELIX GBT DAQ Link Thoughts



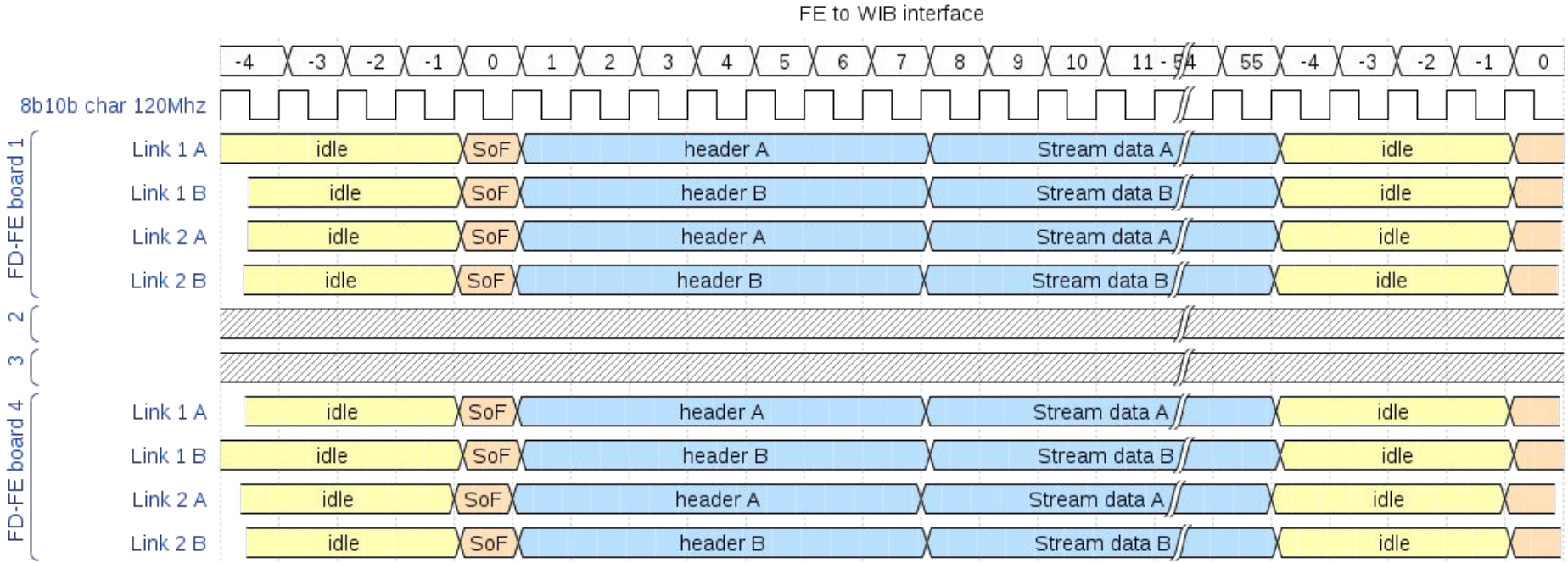
GBT wide mode @ 4.8Gbps

- In wide-mode, we get 112 bits (14 bytes) per 120bit frame. (4.48Gbps of user data)
- In each convert period, we then get 20 14byte frames.
- Since each COLDDATA ASIC sends 112 bytes per convert, we can send a full FE in 16 frames with 2 frames of header and two frames of IDLE.
- This is nice since we have a 1:1 link between Cold FE modules and links to FELIX

Backup

FE data flow

Each FE has two cold data ASICs, each with two 1.2(8)Gbps links.
Every 500ns, a convert signal begins a 56 word long data packet on each ASIC link pairs (112bytes)



The Warm Interface Board (WIB) is needed to convert cold data links to warm data links.
Warm data links would be higher speed with multiple cold links combined.

FE data format (over two links)

-	Link B								Link A								notes
-	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	bits
1	K28.5								K28.5								Start of frame
2	Checksum B[7..0]								Checksum A[7..0]								
3	Checksum B[15..8]								Checksum A[15..8]								
4	Time Stamp																
5	Errors																
6	Reserved																
7	S4				S3				S2				S1				Header bits
8	S8				S7				S6				S5				Header bits
9	S1 [19:12]								S1 [11:04]								Stream 1
10	S1 [35:28]								S1 [27:20]								
11	S1 [51:44]								S1 [43:36]								
12	S1 [67:60]								S1 [59:52]								
13	S1 [83:76]								S1 [75:68]								
14	S1 [99:92]								S1 [91:84]								
15	S2 [19:12]								S2 [11:04]								Stream 2
16	S2 [35:28]								S2 [27:20]								
17	S2 [51:44]								S2 [43:36]								
18	S2 [67:60]								S2 [59:52]								
19	S2 [83:76]								S2 [75:68]								
20	S2 [99:92]								S2 [91:84]								
21	S3 [19:12]								S3 [11:04]								Stream 3
22	S3 [35:28]								S3 [27:20]								
23	S3 [51:44]								S3 [43:36]								
24	S3 [67:60]								S3 [59:52]								
25	S3 [83:76]								S3 [75:68]								
26	S3 [99:92]								S3 [91:84]								
27	S4 [19:12]								S4 [11:04]								Stream 4
28	S4 [35:28]								S4 [27:20]								
29	S4 [51:44]								S4 [43:36]								
30	S4 [67:60]								S4 [59:52]								
31	S4 [83:76]								S4 [75:68]								
32	S4 [99:92]								S4 [91:84]								
33	S5 [19:12]								S5 [11:04]								Stream 5
34	S5 [35:28]								S5 [27:20]								
35	S5 [51:44]								S5 [43:36]								
36	S5 [67:60]								S5 [59:52]								
37	S5 [83:76]								S5 [75:68]								
38	S5 [99:92]								S5 [91:84]								
39	S6 [19:12]								S6 [11:04]								Stream 6
40	S6 [35:28]								S6 [27:20]								
41	S6 [51:44]								S6 [43:36]								
42	S6 [67:60]								S6 [59:52]								
43	S6 [83:76]								S6 [75:68]								
44	S6 [99:92]								S6 [91:84]								
45	S7 [19:12]								S7 [11:04]								Stream 7
46	S7 [35:28]								S7 [27:20]								
47	S7 [51:44]								S7 [43:36]								
48	S7 [67:60]								S7 [59:52]								
49	S7 [83:76]								S7 [75:68]								
50	S7 [99:92]								S7 [91:84]								
51	S8 [19:12]								S8 [11:04]								Stream 8
52	S8 [35:28]								S8 [27:20]								
53	S8 [51:44]								S8 [43:36]								
54	S8 [67:60]								S8 [59:52]								
55	S8 [83:76]								S8 [75:68]								
56	S8 [99:92]								S8 [91:84]								
57	K28.1								K28.1								idle
58	K28.1								K28.1								
59	K28.1								K28.1								
60	K28.1								K28.1								

Possible WIB Data-format (4.8Gbps GBT)

GBT-frame	4	4	80+32														Header/SC/data bits
	15		14	13	12	11	10	9	8	7	6	5	4	3	2	1	bytes
1	H	SC	WIB time stamp 56b							reset cnt 24b			conv cnt 16b		error	0xA5	WIB header
2	H	SC	S4-S1 Header		Reserved		Errors		t-stamp		ChkSm $B_{hi}, A_{hi}, B_{lo}, A_{lo}$				0xBC	0xBC	FE-n Cold ASIC 1
3	H	SC	S1[99:04]												S8-S5 Header		(112-bytes)
4	H	SC	S3[19:04]		S2[99:04]												
5	H	SC	S4[35:04]				S3[99:20]										
6	H	SC	S5[51:04]						S4[99:36]								
7	H	SC	S6[67:04]								S5[99:52]						
8	H	SC	S7[83:04]										S6[99:68]				
9	H	SC	S8[99:4]												S7[99:84]		
10	H	SC	S4-S1 Header		Reserved		Errors		t-stamp		ChkSm $B_{hi}, A_{hi}, B_{lo}, A_{lo}$				0xBC	0xBC	FE-n Cold ASIC 2
11	H	SC	S1[99:04]												S8-S5 Header		(112-bytes)
12	H	SC	S3[19:04]		S2[99:04]												
13	H	SC	S4[35:04]				S3[99:20]										
14	H	SC	S5[51:04]						S4[99:36]								
15	H	SC	S6[67:04]								S5[99:52]						
16	H	SC	S7[83:04]										S6[99:68]				
17	H	SC	S8[99:4]												S7[99:84]		
18	H	SC	CRC				Reserved										WIB trailer
19	H	SC	IDLE/Open														
20	H	SC	IDLE/Open														

Overflow of 2Mhz conv cnt without a corresponding 30.5Hz sync command would flag an error.
Time-stamp with 56b would give long rollover time when run off of a fast WIB clock
IDLE words give us 50ns per convert of room to catch up.

WIB data flow

Each FE board is merged into one FELIX link

- Stream A and B from each CDA are placed into a FIFO
- When both CD ASICs transition to IDLE, we can check for errors, and build WIB header
- Then transmit header, CD ASIC 1 stream, CD ASIC 2 stream, and trialer.
- The two output idle frames (50ns) could be dynamically dropped if the current packet started late.