Notes of wire scanner upgrade meeting 19.05.2016

Agenda:

1. New wire scanner: Investigation of the choice of the digital controller hardware. (J. Emery)

2. New high performance inverter for the wire scanner intelligent drive v2. (P. Andersson)

3. Status of the actuator tests. (J. Emery)

Indico: https://indico.cern.ch/event/531955/

Jonathan - Electronics

Option 1 : VFC motherboard with FMC mezzanine

Option 2 : New single WS board incorporating FPGA & I/O

Option 3 : Current development kit

- One intelligent drive per scanner
- 6U space required per scanner + VME
- One VME crate with VFC for slow control, acquisition & diagnostics
- ADC up to 500MHz transmission
- SFP possible for optical link?

Option 1 & 2 & 3 possible from integration point of view
- VFC needs removal of 4xSFP bank
- May be possible to have higher with flexible FMC cable. However need to check maximum speed (as 500MHz required)

Power supplies
- Looks OK for VFC - need to check that it can supply 1.8V required by mezzanine

EMI
- Better on custom & development kit

Digital Architecture
- Dev kit has Aria V SX/ST with embedded ARM processor
  - Allows fast Ethernet connection (x10 compared to NIOS)
- Existing code to VFC
  - Need to re-implement much of the code
- Advantage is that many designers working on this
- Memory

- Development kit - 3 banks
- Up to 6.4Gbit/s

- VFC
- Up to 3.2Gbit/s
  - Speed could be limit for optical & resolver data
- Could maybe use internal RAM for control ADC data (36.12Mbit/s)
- System & Firmware testability
  - OK for all options
  - Most in VHDL so selection of FPGA not so critical for final implementation
  - Choice of FPGA more of an issue for design
- Faster prototyping with c-code in processor

Summary
- All 3 options viable for wire scanner control

- Option 3 quickest, but questions about long term maintainability & possibility of procuring large quantities

- Option 2 best for customisation & optimal configuration. However lead time to have a working board is at least 1 year. Possibly 1-2 years if second version required. This is very tight for LIU installation in LS2 & will require significant resources from a small team.

- Option 1. Not ideal in terms of integration and may have limitation on read-out rate & memory access. However, the board will be available soon and is guaranteed long term maintainability as it's used by many future BI systems.

DECISION : Use the VFC as the motherboard for the new wire scanner control electronics.

Patrik - Power Electronics

New control card prepared & tested
Adapted to 600V (PCB & connectors)
- New motor will in the end be at 300V
  - If 600V required then PCB OK but would need new capacitor & power supplies
- Tested with & without active cooling
  - 1hr with 1scan/s led to rise up to 50C without cooling
  - With cooling limited to 32C
- Next step
  - Integrate current measurement

Action:

Jonathan

Look up if SFP could be used for optical encoder
Look up if cable connection is possible for FMC connections

1.8 volt needed for the used ADC to be used on the FMC
Memory calculations to be more detailed
NYOS usage of some ram? to be investigated
Existing firmware investigations
ARM needed?

Christos

Investigations if ARRIA 5 with ARM is compatible with VFC layout
Investigation of other FPGA options

Bernd

Decide if in and out scans are used