

GBT-FPGA Tutorial

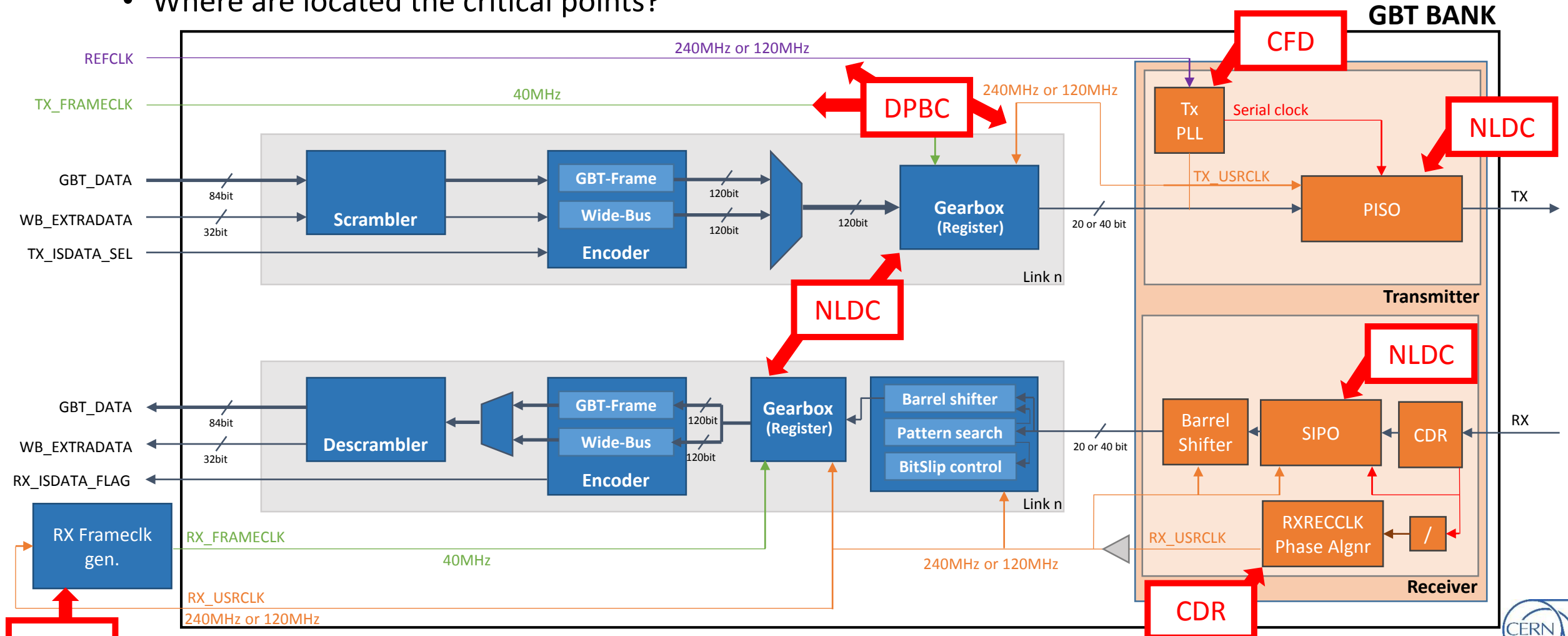
Creation of a reference design in standard mode

Outline

- What are the critical points of the latency-optimized mode?
- How to improve the design to use latency-optimized mode?
- How to constraint my design?
- How to debug the design?

What are the critical points of the latency-optimized mode?

- Where are located the critical points?



CFD

27/06/2016

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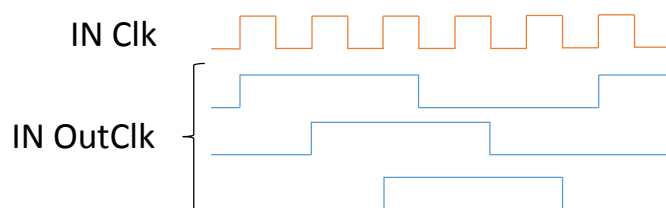


What are the critical points of the latency-optimized mode?

- How to configure the transceiver for the latency-optimized mode?
 - NLDC: Non Latency Deterministic Components
 - Clock domain crossing shall be made using register-based modules.

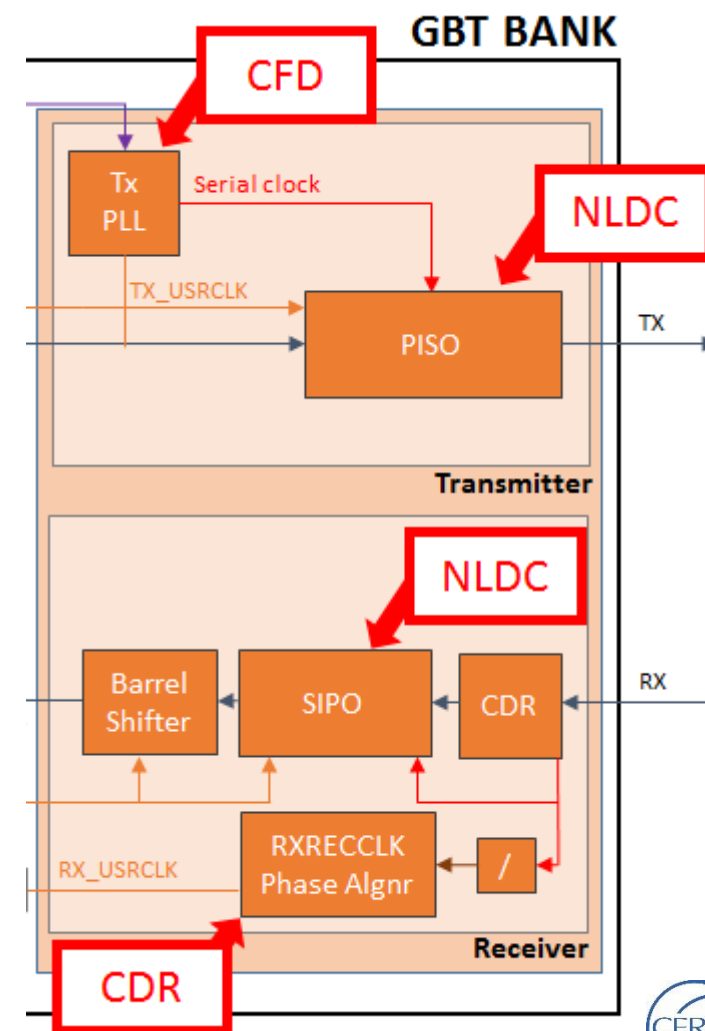
- CFD: Clock frequency division

- Rising edge of derived clock may lock onto any of the rising edge of the input clock.



- CDR: Clock and Data recovery

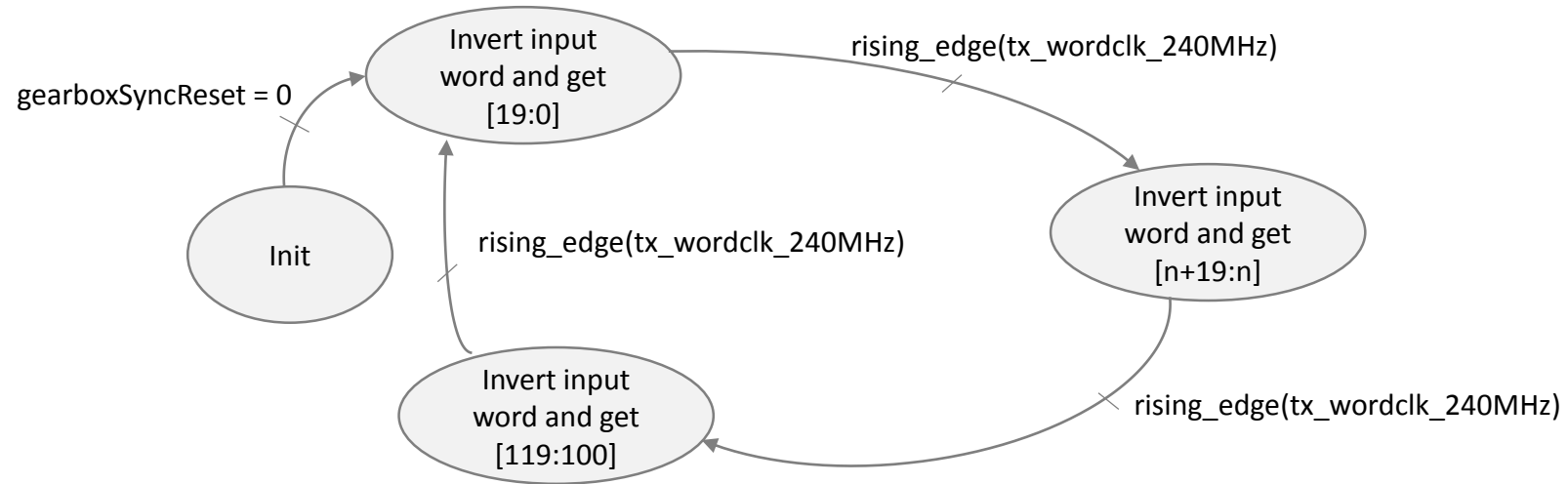
- Serial clock is divided by N to construct the usrclk.
 - Dual data rate implies the recovered clock can latch on both rising and falling edge of the serial clock.
 - State machine monitors the CDR to ensure a deterministic phase.



DEMO

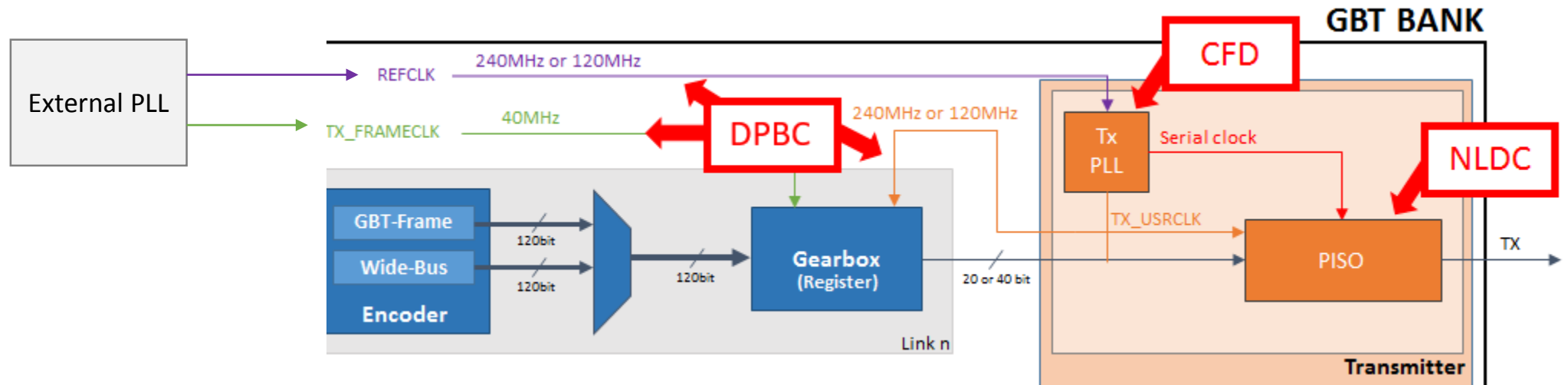
What are the critical points of the latency-optimized mode?

- How does the gearbox work in latency-optimized mode?
 - Standard mode: based on RAM memory
 - Latency-optimized mode: register-based
 - Special case for TX Gearbox: external PLL



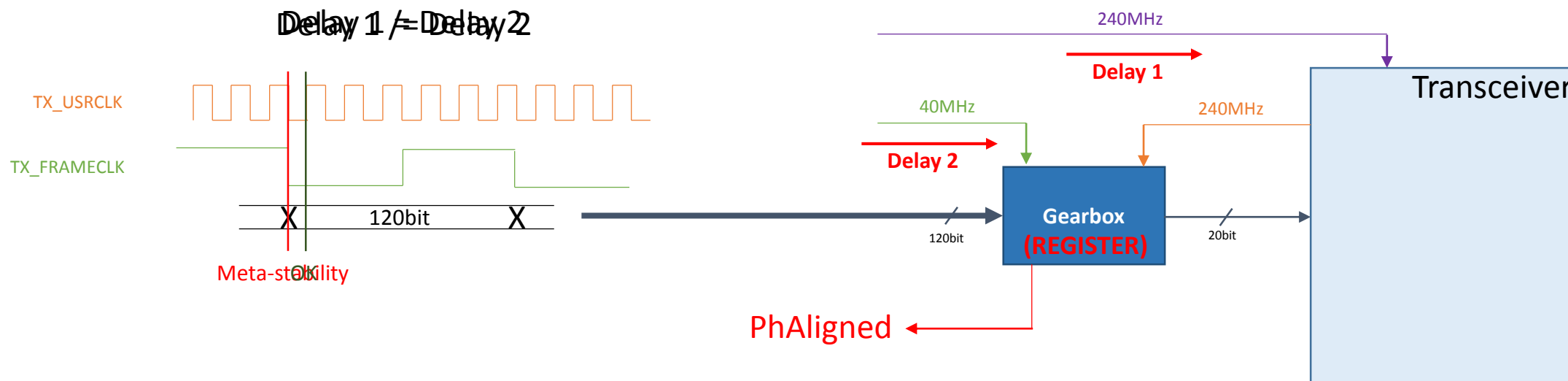
What are the critical points of the latency-optimized mode?

- Why does the TX gearbox is a special case?
 - DPBC: Deterministic Phase Between Clocks



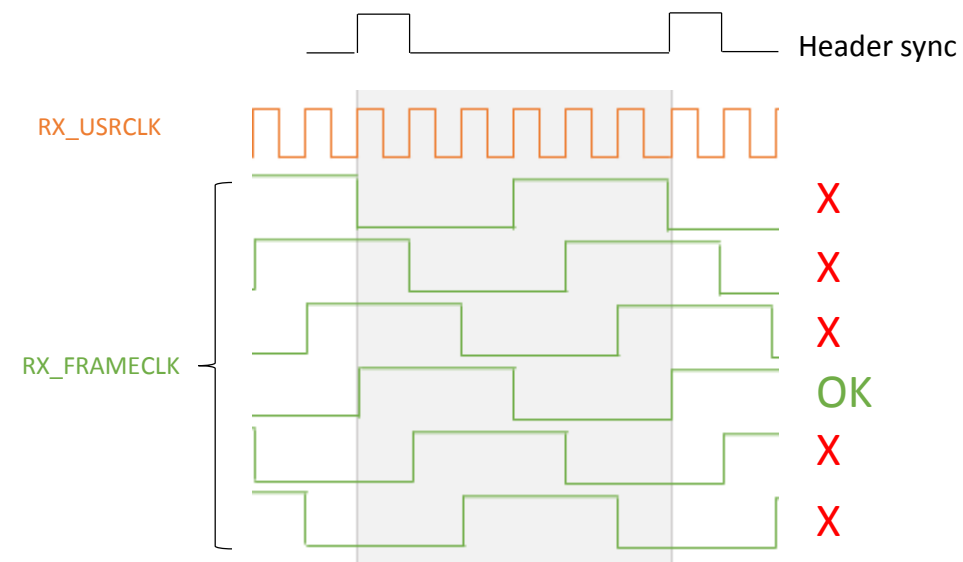
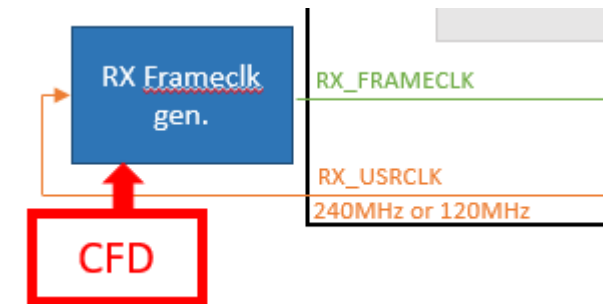
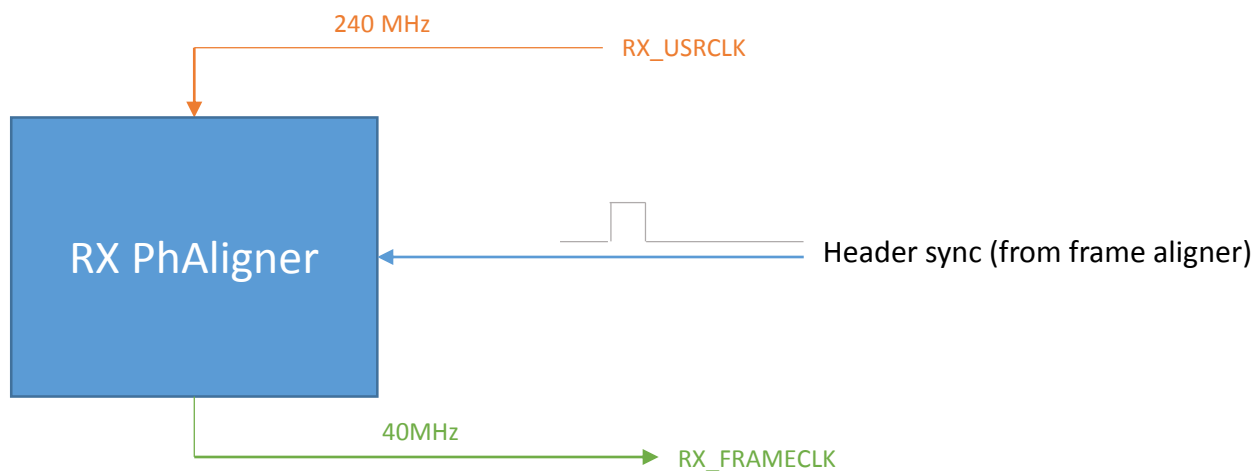
What are the critical points of the latency-optimized mode?

- Why does the TX gearbox is a special case?



What are the critical points of the latency-optimized mode?

- How the RX FrameClk (40MHz) is generated?

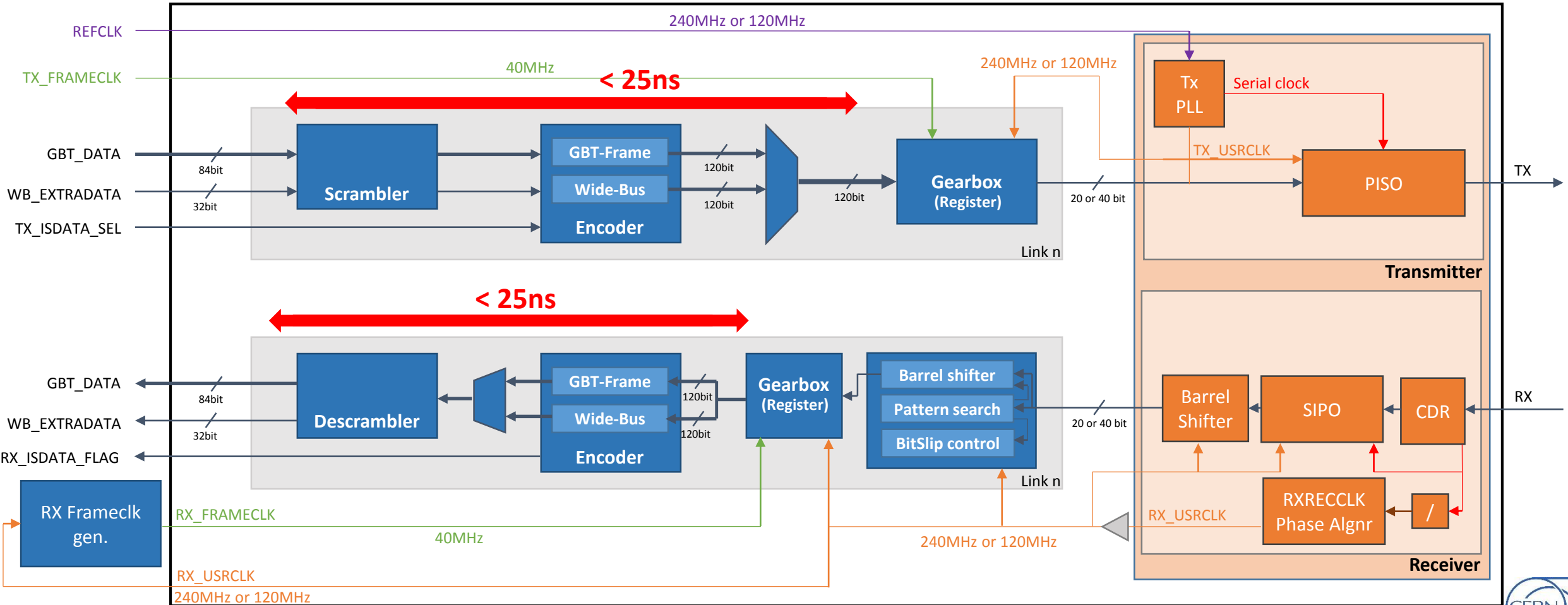


What are the critical points of the latency-optimized mode?

- What are the other solutions to generate the RX FrameClk (40MHz)?
 - VHDL clock divider:
 - Pros: no clocking resources
 - Cons: worst jitter and require a special care for the constraints
 - Clock enable:
 - Pros: less clocking resources
 - Cons: Duty cycle is not 50%

DEMO

How to constraint my design?



DEMO