GBT-FPGA Tutorial

Tips & Tricks

Outline

- Clock Schemes and external PLLs
- GBT-FPGA to GBTx loopback demonstration
- More information about GBTx e-links
- AOB

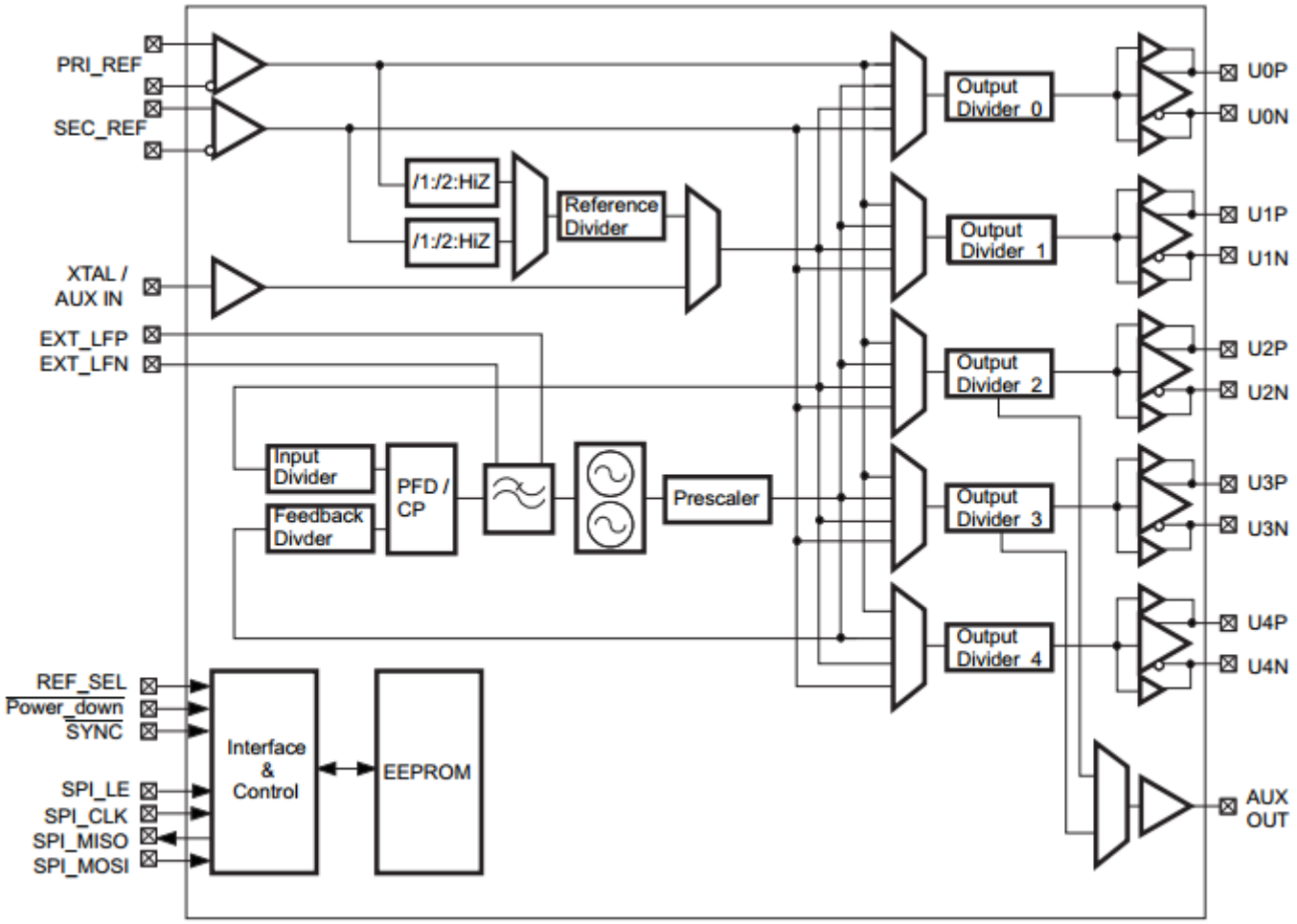
PLLs for GBT-FPGA

- Fixed and deterministic phase:
  - 40MHz input, 120MHz or 240MHz output
  - The phase of the output clocks vs input clock (skew) remains always constant
    - After power cycles
    - After reset cycles
  - Changes only linearly with temperature
  - Good jitter performance

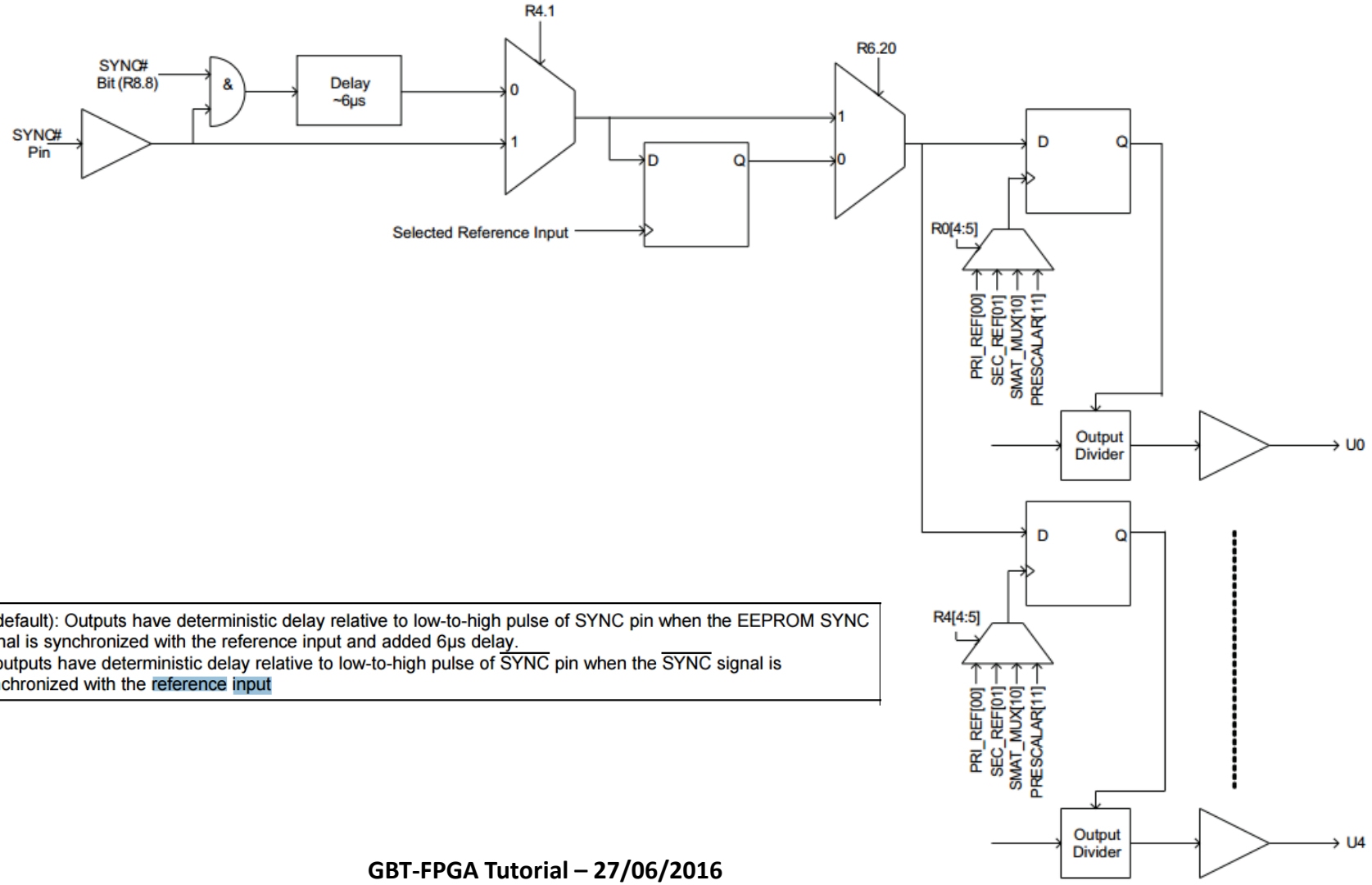
- 3 PLLs identified
  - CDCE62005 (Texas) – excellent jitter performance, not fully deterministic
  - Si5338 (Silabs) – poor jitter cleaning, fully deterministic
  - Si5344/45 (Silabs) – excellent jitter performance, seems fully deterministic*

* Simple Temperature tests performed, to be contined

CDCE62005

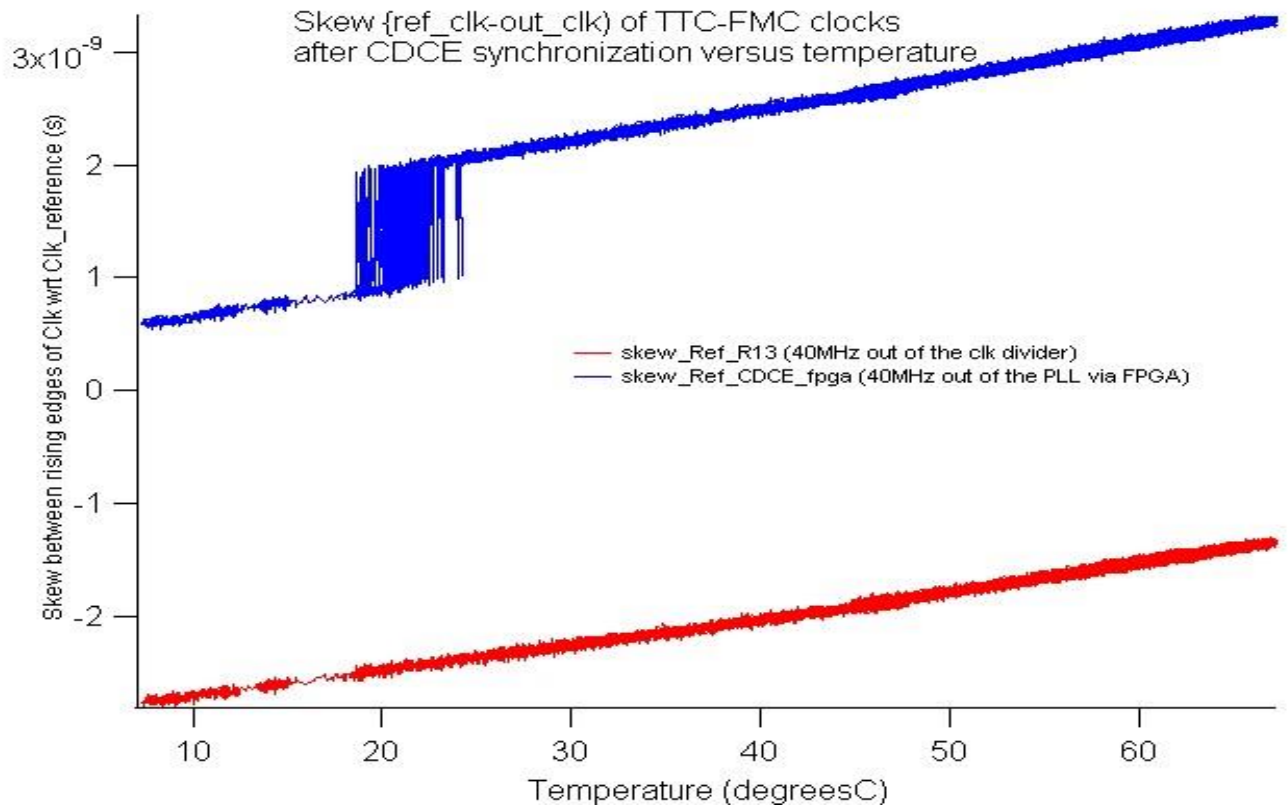

PRI_REF
SEC_REF
XTAL / AUX IN
EXT_LFP
EXT_LFN
/1:/2:HiZ
/1:/2:HiZ
Reference Divider
Input Divider
Feedback Divder
PFD / CP
Prescaler
Output Divider 0
Output Divider 1
Output Divider 2
Output Divider 3
Output Divider 4
U0P
U0N
U1P
U1N
U2P
U2N
U3P
U3N
U4P
U4N
AUX OUT
REF_SEL
Power_down
SYNC
SPI_LE
SPI_CLK
SPI_MISO
SPI_MOSI
Interface & Control
EEPROM

CDCE62005

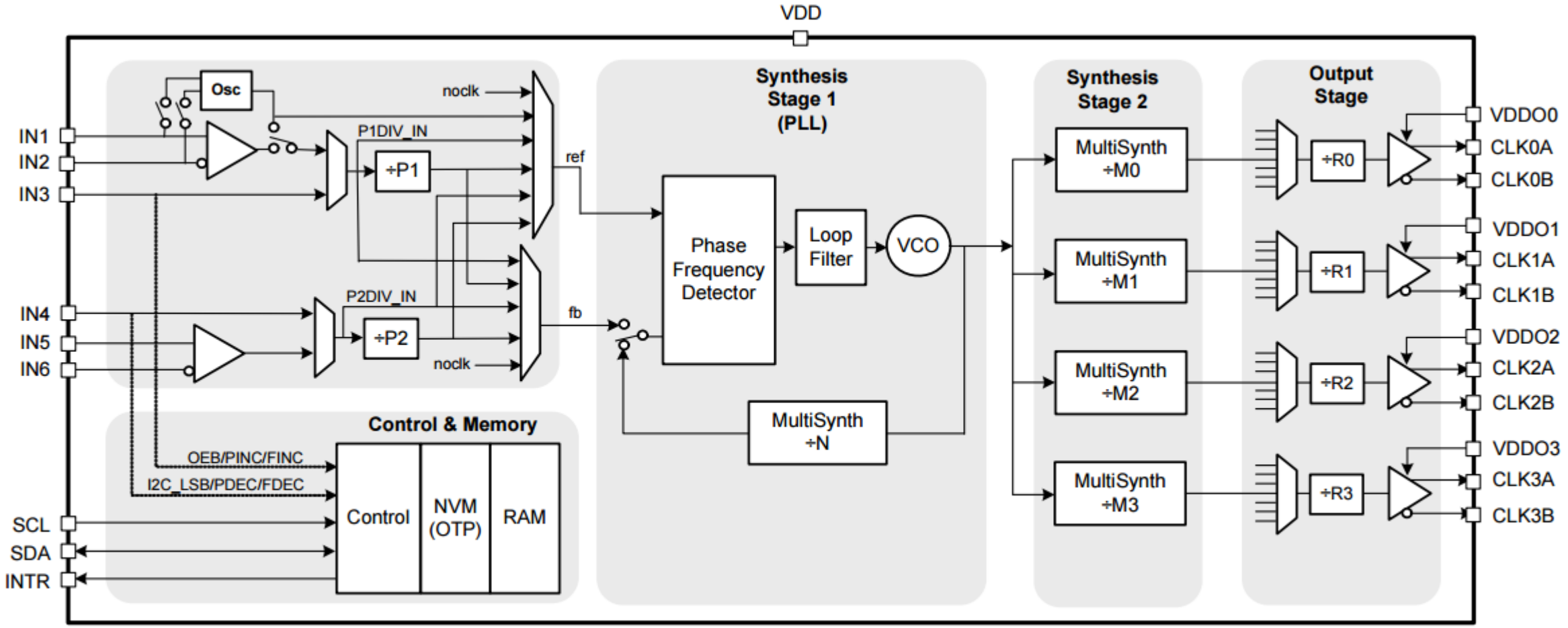


1	SYNC_MODE1	Outputs	0 (default): Outputs have deterministic delay relative to low-to-high pulse of SYNC pin when the EEPROM SYNC signal is synchronized with the reference input and added 6µs delay. 1: outputs have deterministic delay relative to low-to-high pulse of $\overline{\text{SYNC}}$ pin when the $\overline{\text{SYNC}}$ signal is synchronized with the reference input

CDCE62005
Deterministic phase versus temperature



Si5338 & Si5344



Si5338 & Si5344

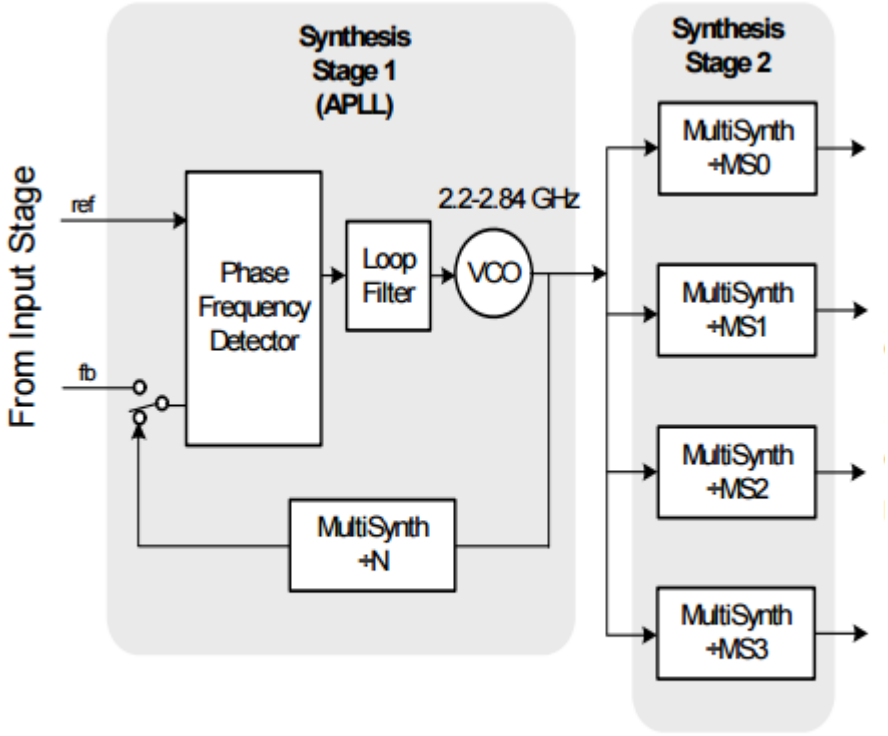


Figure 5. Synthesis Stages

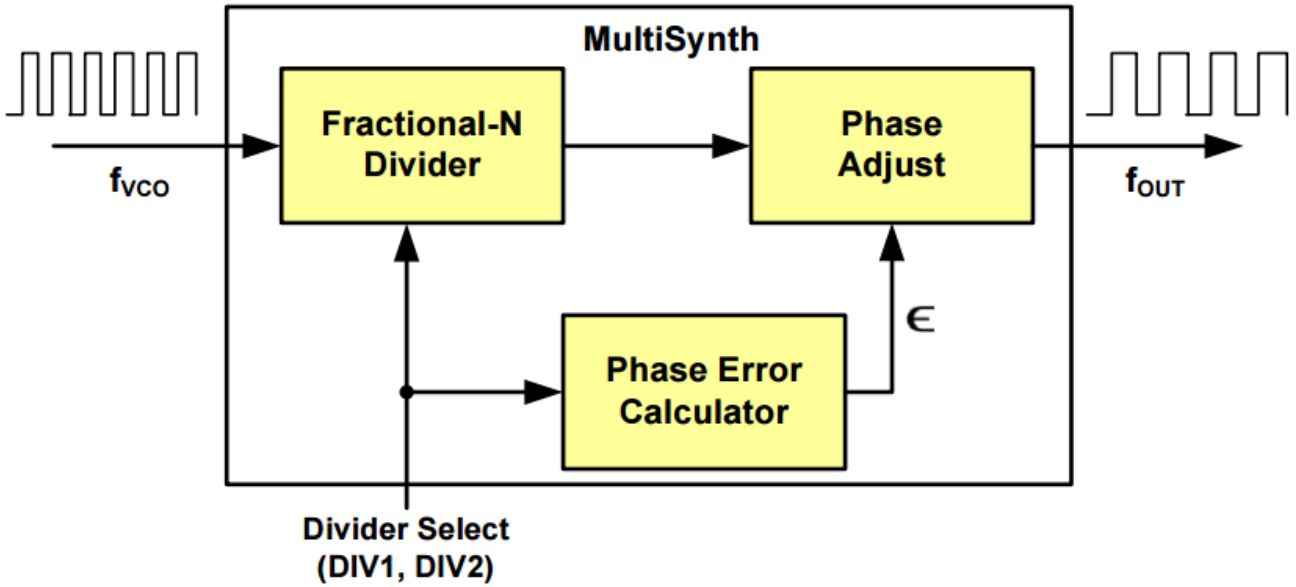
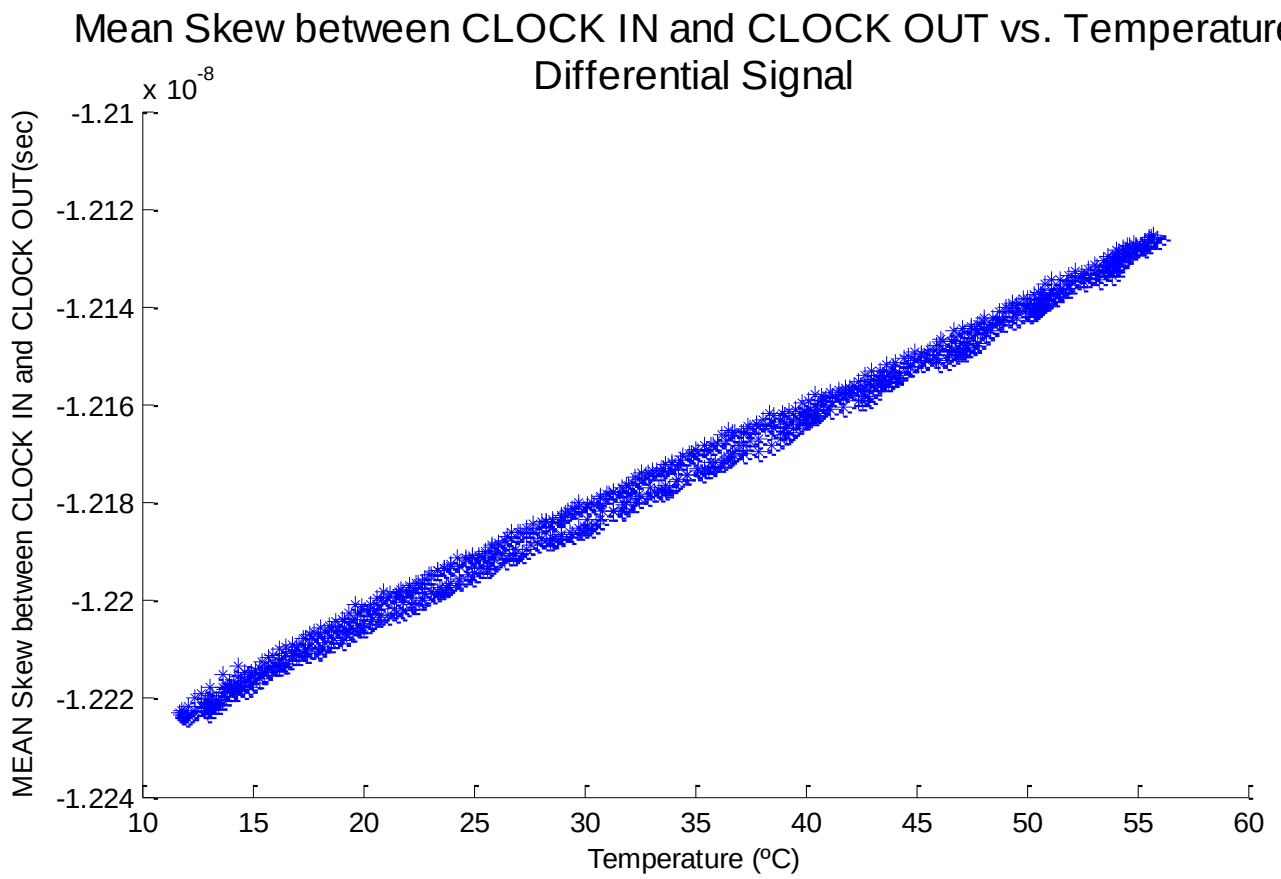
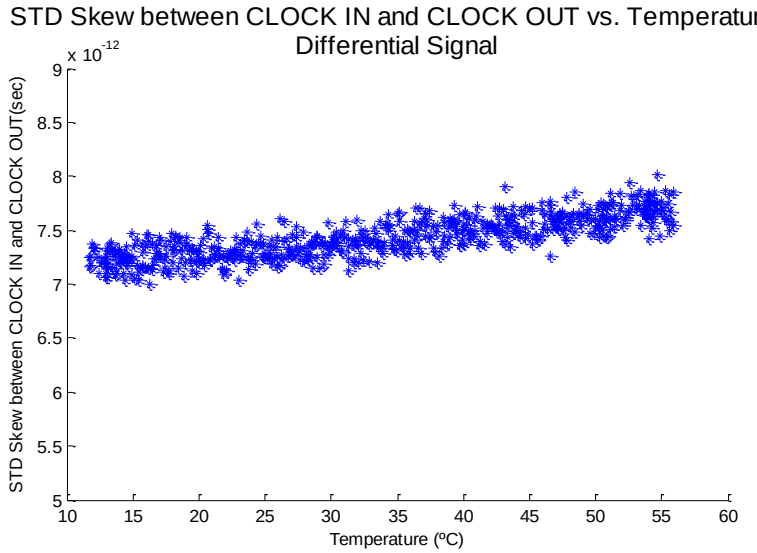


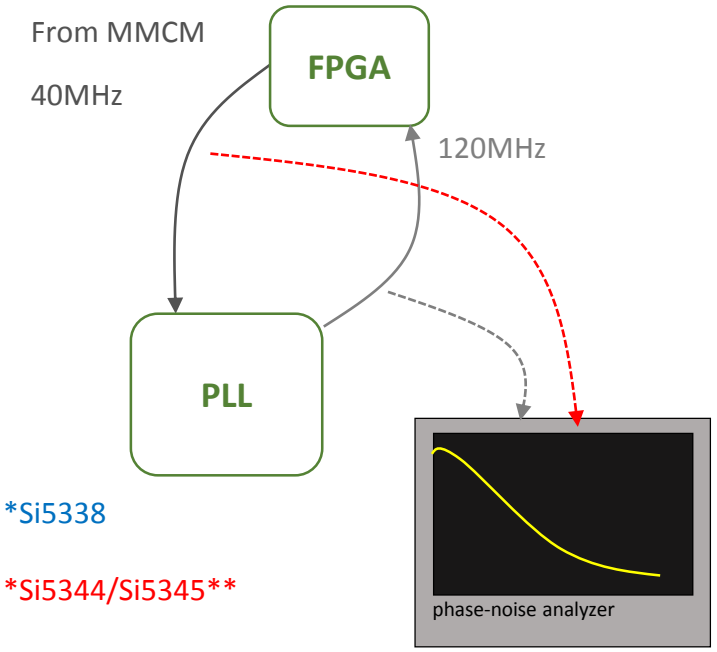
Figure 6. Silicon Labs' MultiSynth Technology

Si5338


Mean Skew between CLOCK IN and CLOCK OUT vs. Temperature
Differential Signal
x 10^-8
MEAN Skew between CLOCK IN and CLOCK OUT(sec)
-1.21
-1.212
-1.214
-1.216
-1.218
-1.22
-1.222
-1.224
10
15
20
25
30
35
40
45
50
55
60
Temperature (ºC)

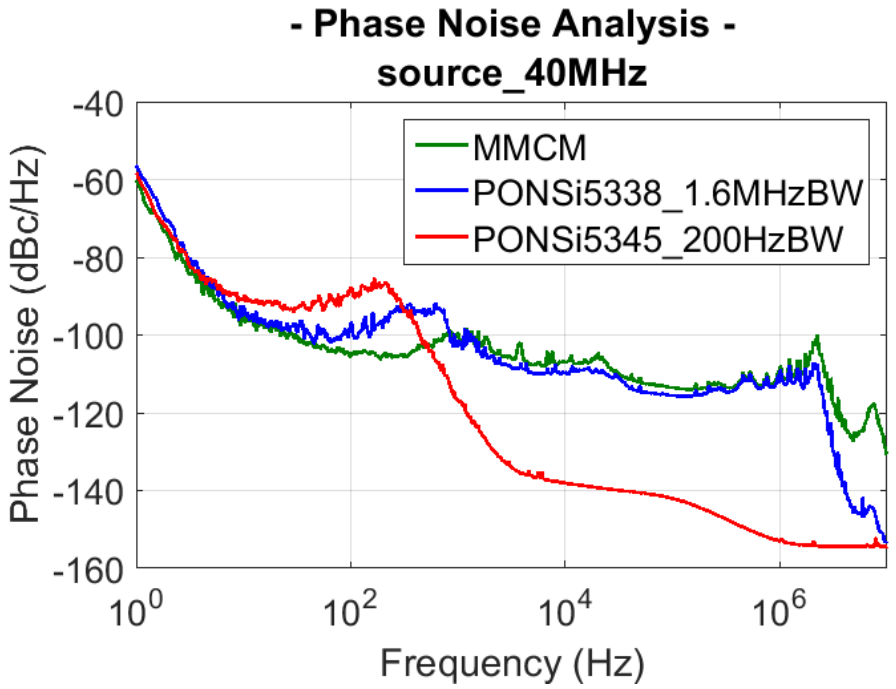

STD Skew between CLOCK IN and CLOCK OUT vs. Temperature
Differential Signal
x 10^-12
STD Skew between CLOCK IN and CLOCK OUT(sec)
9
8.5
8
7.5
7
6.5
6
5.5
5
10
15
20
25
30
35
40
45
50
55
60
Temperature (ºC)

PLLs – cleaning performance



*Si5338

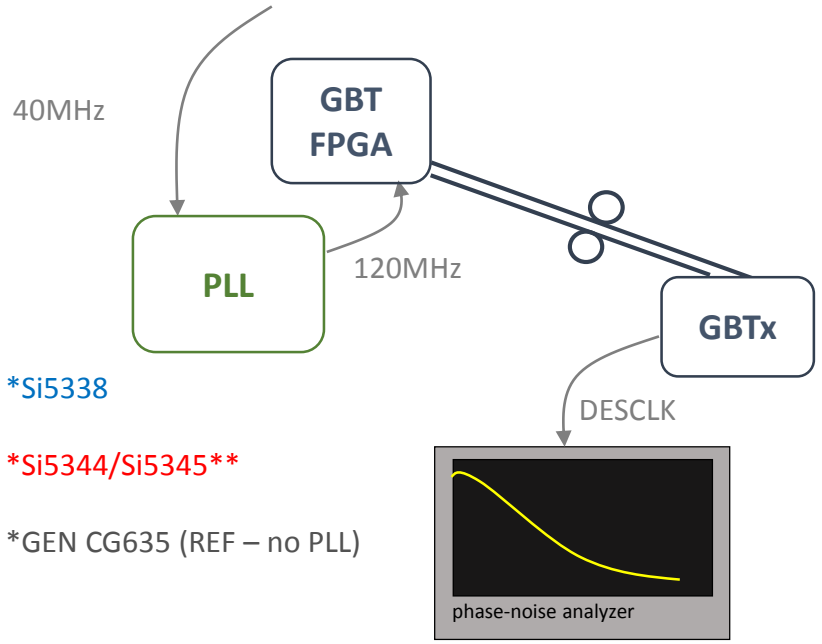
*Si5344/Si5345**

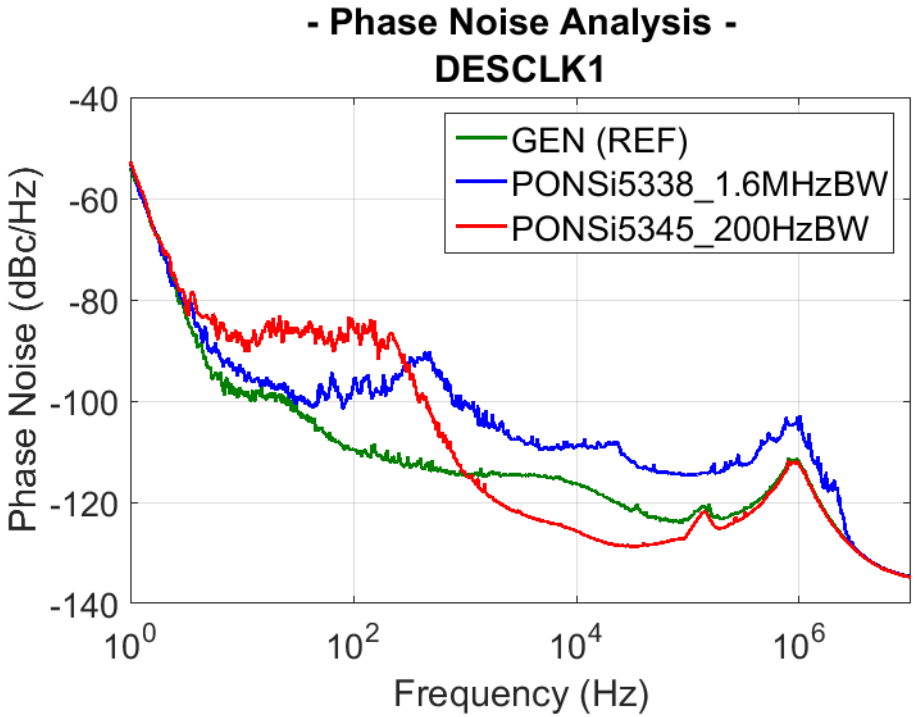


	MMCM	Si5338	Si5344
RMS jitter (1Hz-10MHz)	43.39ps	24.99ps	4.95ps

**CDCE has jitter performance close to Si5344C

GBT link / Jitter map

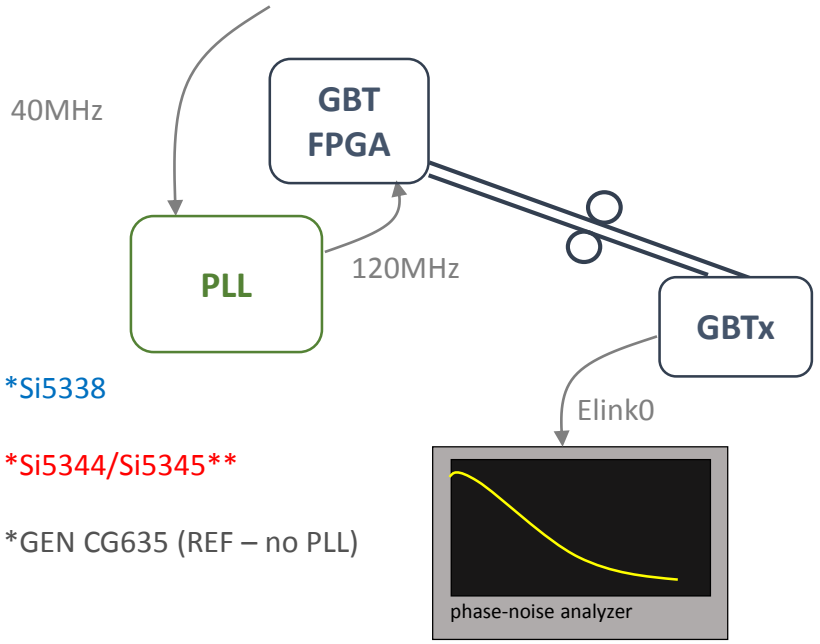




DESCLK1	GEN (REF.)	Si5338	Si5344
RMS jitter (1Hz-10MHz)	13.74ps	29.94ps	13.85ps

**CDCE has jitter performance close to Si5344

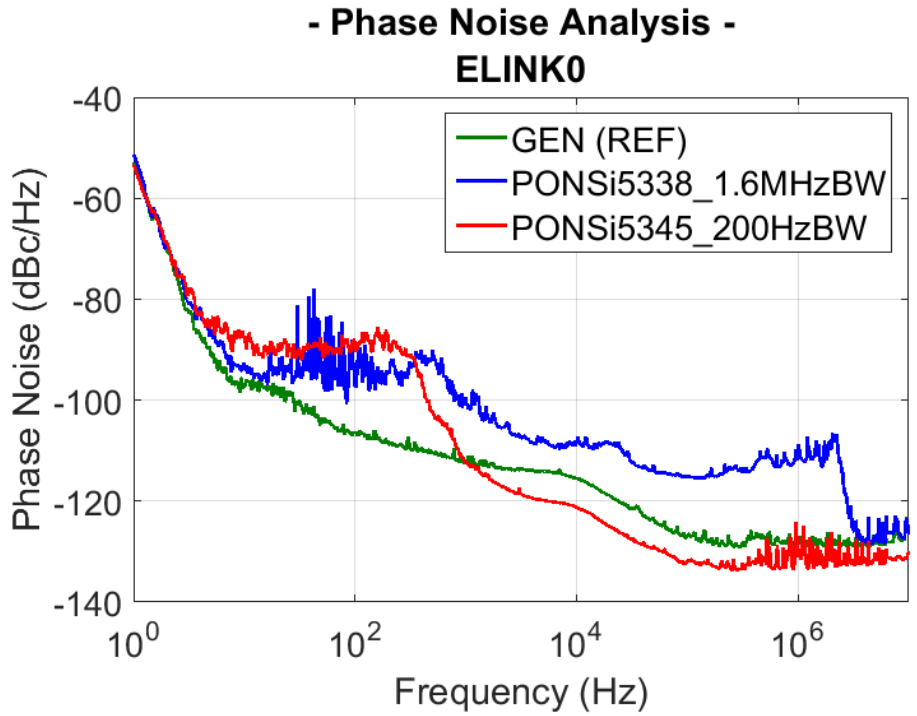
GBT link / Jitter map



*Si5338

*Si5344/Si5345**

*GEN CG635 (REF – no PLL)



ELINK0	GEN (REF.)	Si5338	Si5344
RMS jitter (1Hz-10MHz)	9.79ps	28.31ps	8.49ps

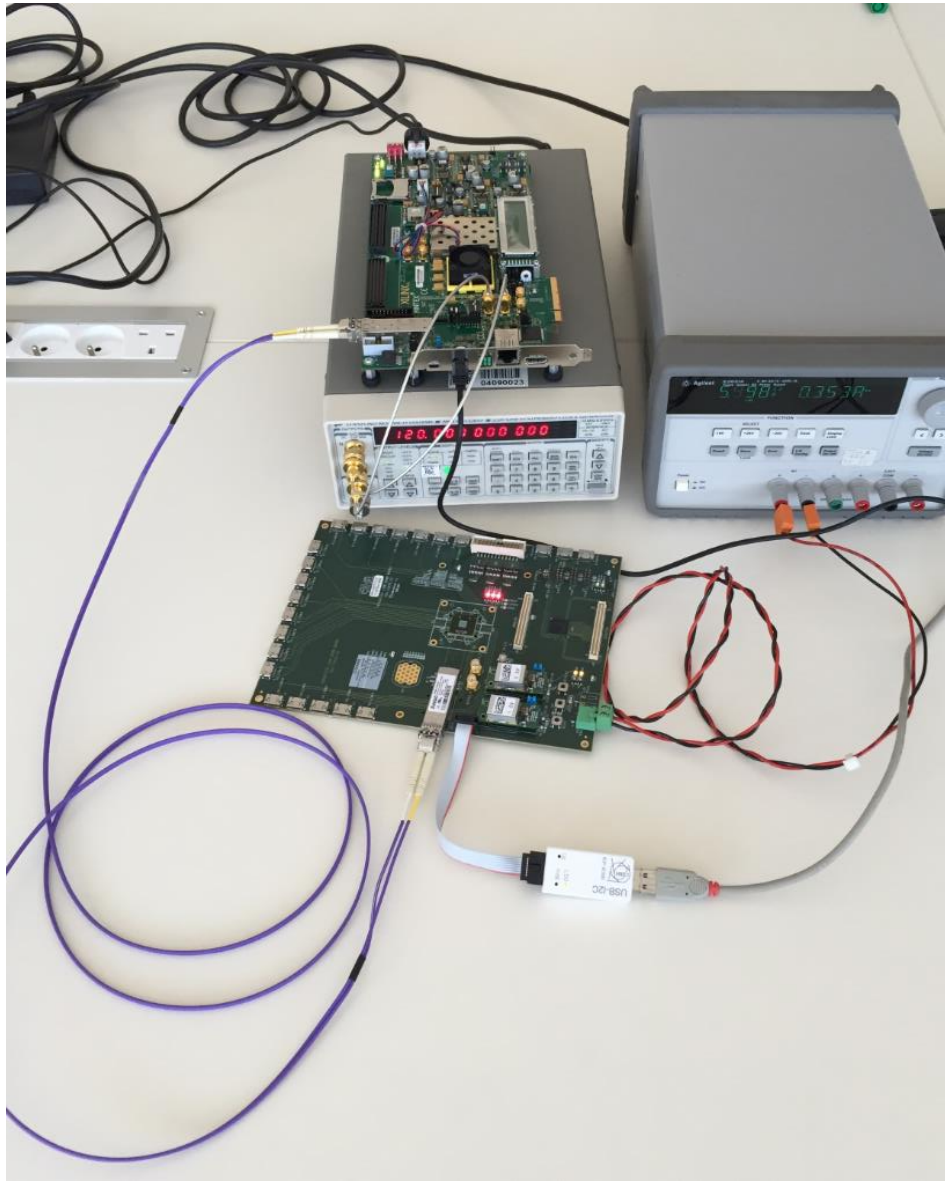
**CDCE has jitter performance close to Si5344

Outline

- Clock Schemes and external PLLs
- GBT-FPGA to GBTx loopback demonstration
- More information about GBTx e-links
- AOB

DEMO

GBT-FPGA to GBTx loopback



GBT Mode

"x2 mode"= elinks @ 80MHz

G0	Din	7	6	5	4	3	2	1	0
G1	Din	15	14	13	12	11	10	9	8
G2	Din	23	22	21	20	19	18	17	16
G3	Din	31	30	29	28	27	26	25	24
G4	Din	39	38	37	36	35	34	33	32
G0	Dio	7	6	5	4	3	2	1	0
G1	Dio	15	14	13	12	11	10	9	8
G2	Dout	23	22	21	20	19	18	17	16
G3	Dout	31	30	29	28	27	26	25	24
G4	Dout	39	38	37	36	35	34	33	32

UP – 40 links

DOWN – 40 links

Groups are evenly used down and up

Outline

- Clock Schemes and external PLLs
- GBT-FPGA to GBTx loopback demonstration
- More information about GBTx e-links
- AOB

E-links : GBT Mode

"x4 mode"= elinks @ 160MHz

G0	Din	6	4	2	0
G1	Din	14	12	10	8
G2	Din	22	20	18	16
G3	Din	30	28	26	24
G4	Din	38	36	34	32
G0	Dio	6	4	2	0
G1	Dio	14	12	10	8
G2	Dout	22	20	18	16
G3	Dout	30	28	26	24
G4	Dout	38	36	34	32

UP – 20 links

DOWN – 20 links

Groups are evenly used down and up

E-links : GBT Mode

"x8 mode"= elinks @ 320MHz

G0	Din	4	0
G1	Din	12	8
G2	Din	20	16
G3	Din	28	24
G4	Din	36	32
G0	Dio	4	0
G1	Dio	12	8
G2	Dout	20	16
G3	Dout	28	24
G4	Dout	36	32

UP – 10 links

DOWN – 10 links

Groups are evenly used down and up

E-links : GBT Mode

GBT Mode

“x2”=80Mbps = D7 & D6 & D5 & D4 & D3 & D2 & D1 & D0
“x4”=160Mbps= D6 & D4 & D2 & D0
“x8”=320Mbps= D4 & D0

E-links : Wide Bus Mode

"x2 mode"= elinks @ 80MHz

G0	Din	7	6	5	4	3	2	1	0
G1	Din	15	14	13	12	11	10	9	8
G2	Din	23	22	21	20	19	18	17	16
G3	Din	31	30	29	28	27	26	25	24
G4	Din	39	38	37	36	35	34	33	32
G5	Dio	7	6	5	4	3	2	1	0
G6	Dio	15	14	13	12	11	10	9	8
G2	Dout	23	22	21	20	19	18	17	16
G3	Dout	31	30	29	28	27	26	25	24
G4	Dout	39	38	37	36	35	34	33	32

UP – 56 links

DOWN – 24 links

Up path uses more links than Down path

E-links : Wide Bus Mode

"x4 mode"= elinks @ 160MHz

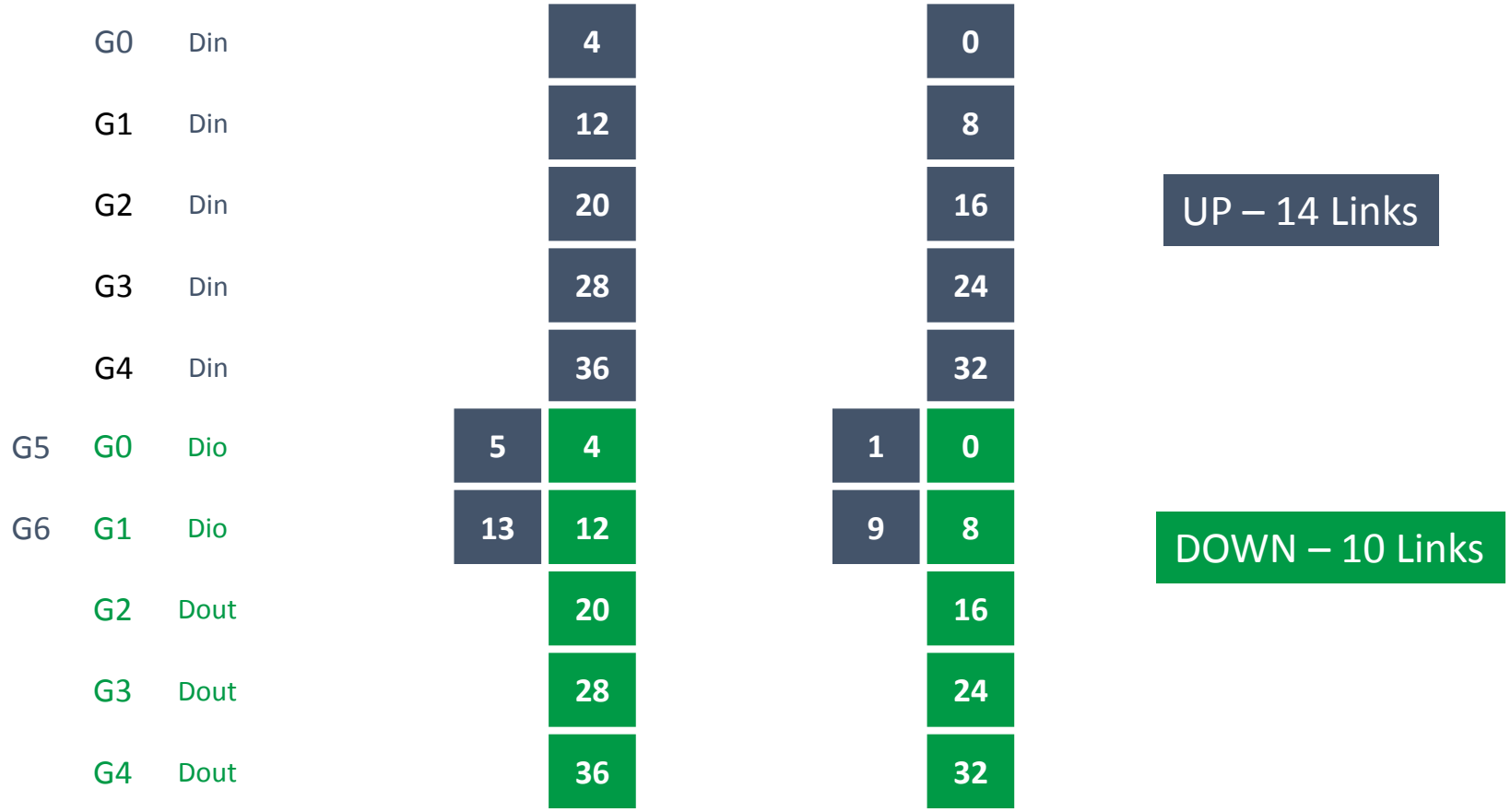
UP – 28 Links

DOWN – 20 Links

- Up path uses more links than Down path

E-links : Wide Bus Mode

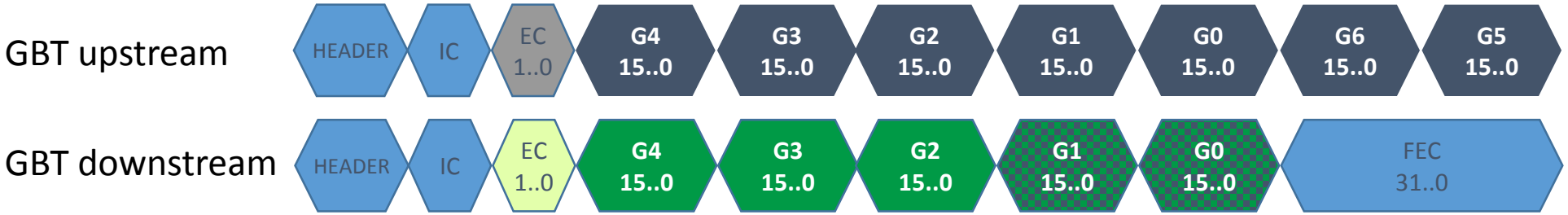
"x8 mode"= elinks @ 320MHz



Up path uses more links than Down path

E-links & serial frame: widebus mode

Wide-Bus Mode (GBT down/Wide-Bus up)

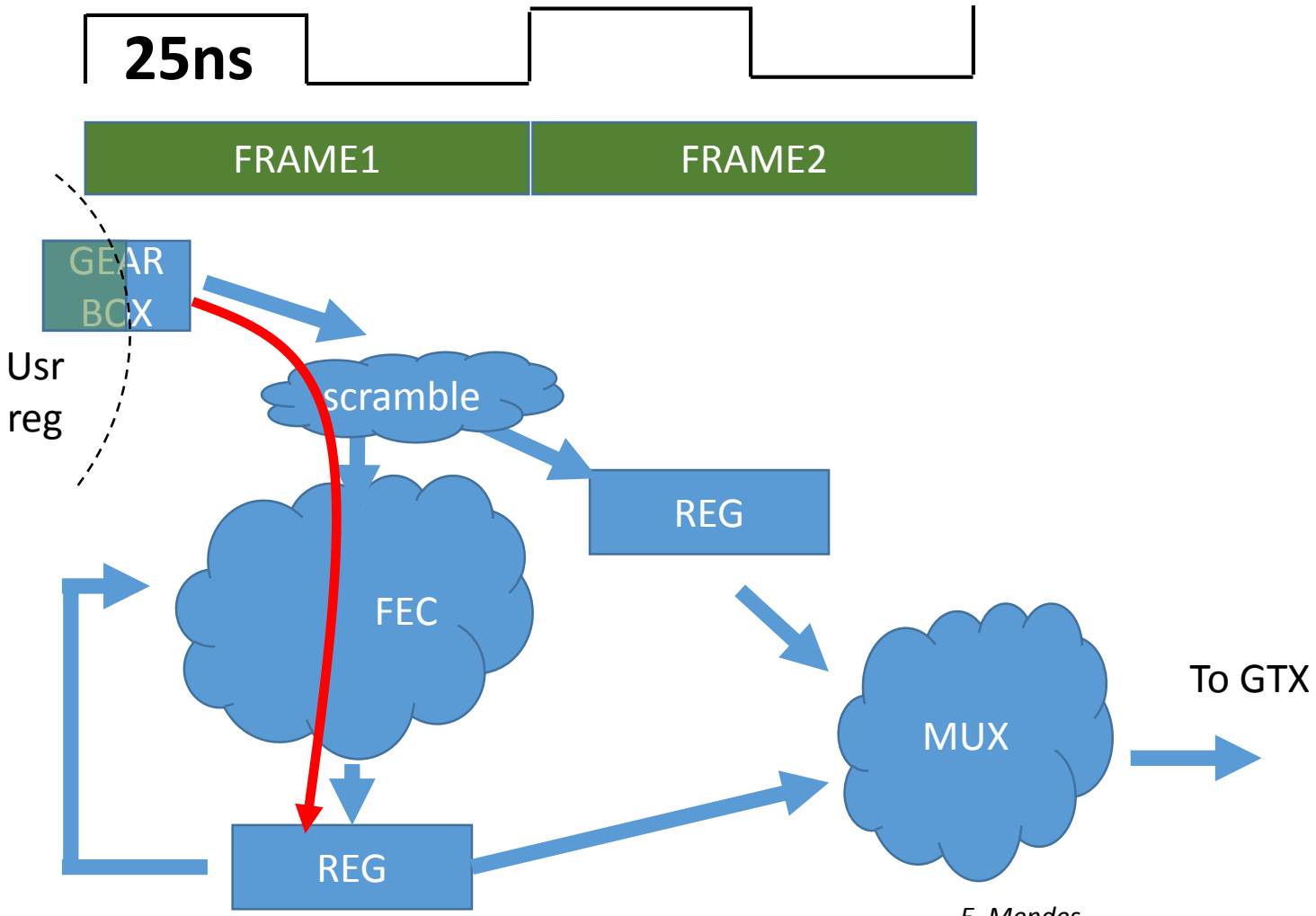


Downstream payload reduced @ “x2 mode”

Outline

- Clock Schemes and external PLLs
- GBT-FPGA to GBTx loopback demonstration
- More information about GBTx e-links
- AOB

GBT-FPGA @ 240MHz (or 120MHz)?



-simplifies interface with the logic of the FPGA if it runs faster than 40MHz
-use 120MHz or 240MHz with multi cycle
-parallelise encoding and serialization

E. Mendes