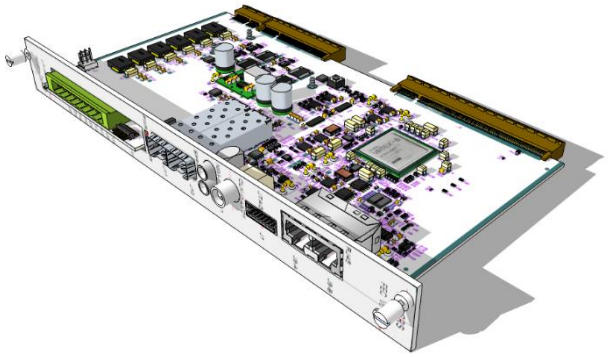
SRS electronics update

- Status SRS hardware (classic)
- Ongoing R&D on new devices
- SRS licencies

Hans Muller CERN EP

FEC –V6: Front End Concentrator



- SRS readout concentrator card
- V6 version based on Virtex-6 technology
- Successor of V3 FEC card for zero suppression enhancement
- New fontpanel I/O connector
- Socket for 2GB DDR3 memory*
- NIM-out trigger counter (firmware)
- VMM readout firmware for FEC-V6
- Firmware updates : tutorial manual on

https://espace.cern.ch/rd51-wg5/srs/Documentation/Forms/AllItems.aspx

*Micron **MICMT47H128M16RT-25E:C**

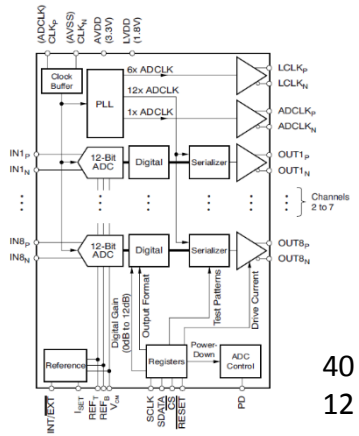
Photo : FEC V6 production (SAMWAY)

ADCard: adapter card for analogue frontends

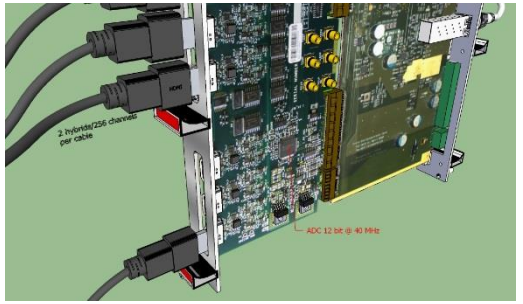
- Plugs directly to FEC cards (V3 or V6)
- 16 shannels of 40 MHz , 12 bit ADCs
- good for readout of 16 APV hybrids (2k channels)
- 2 Hybrids (M+S) connected via one single HDMI port
- 8 HDMI ports with power for APV's
- HDMI cable length up to 25 m

ADCard revisions:

- power selection for short –long cables
- 20 MHz operation (doubles APV pipeline trigger latency)



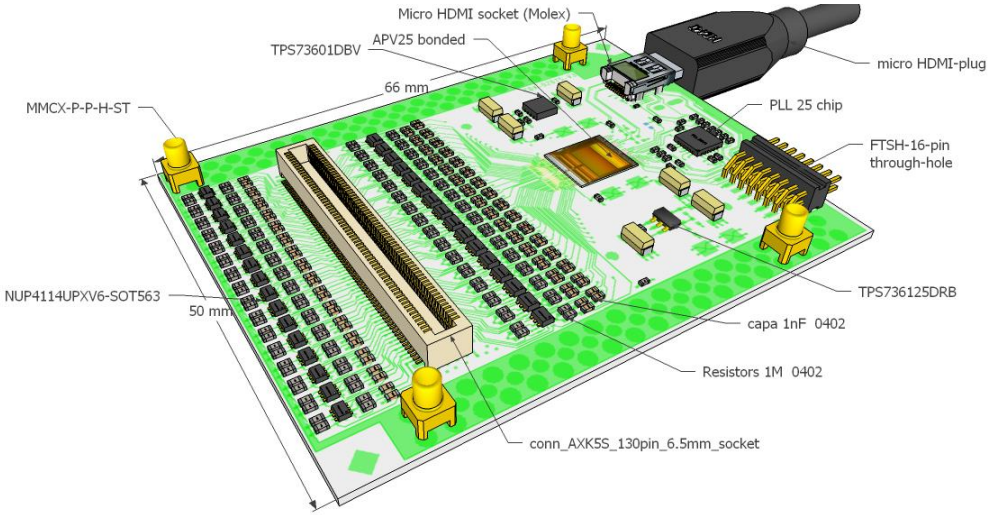
40 MHz
12 bit ADC

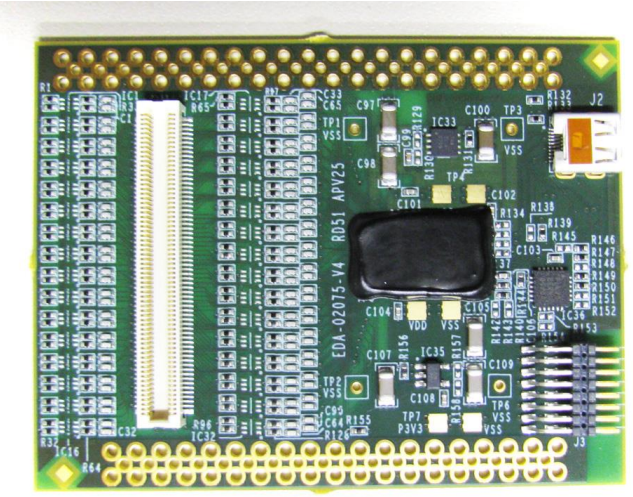


ADC-FEC Combo

APV-128: analogue frontend for SRS

- APV25 ASIC: designed for CMS silicon strip detectors
- Tested up 10 Mrad, no significant degradation
- 128 analogue readout channels
- 192 deep analogue pipleline @ 40 MHz (4us)
- 0.3 Watt power consumption 128 ch
- ENC noise 430 + 61/pF (1 fC @ 20 pF)





SRS: 6 layer APV hybrid V3 (masters/Slaves) produced by NEOHM

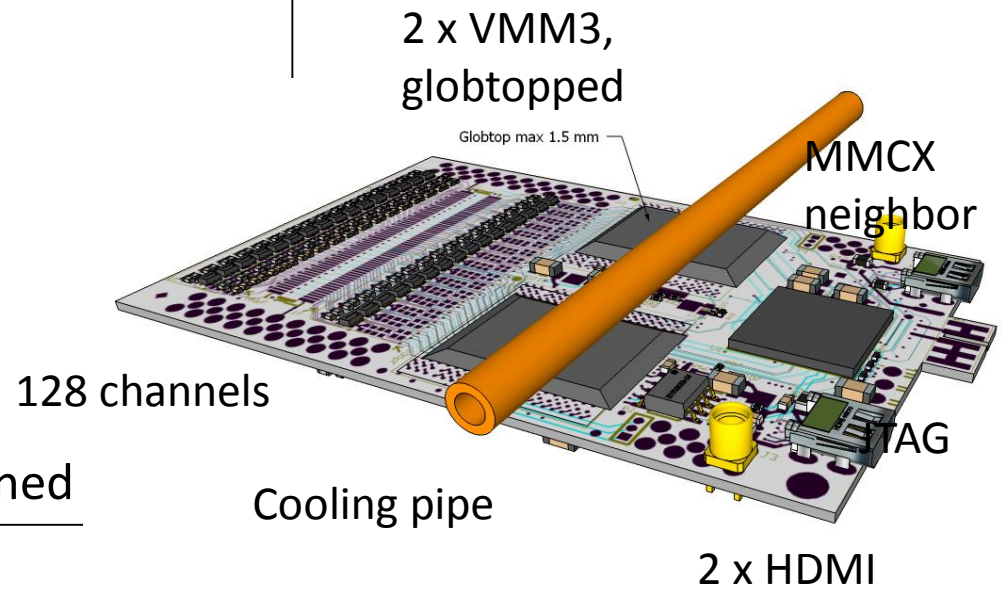
- wire-bonded APV 25 (globtopped)
- Detector AC coupling 1M x 100pF
- ESD spark protection <1pF, 8kV peak 30A(1ns)-16A(30ns)-8A(60ns)
- SRS Clock &Trigger recovery via PLL25 chip

VMM-128: digital frontend for SRS

- overcome APV (analogue readout) limitations of O (3kHz) per APV hybrid
- VMM Chip (digital, peak finding, Z-suppressed) min. 1MHz / channel
- RD51: wire-bonded VMM-128 hybrid : 8-layer PCB routing ready
- neighbor-channel interconnection via MMCX interconnection
- Master-slave option via 2nd HDMI: FPGA firmware
- 2.9W per hybrid* => cooling very important
- VMM3 availability: no EAR restrictions
- New connector + DCDC power saving Voltage Regulators : planned

VMM features:

- Triggerless
  … but can be triggered
- max 5MHz / channel
- 1fC noise at 200 pF
- 1ns timing resolution
- configuration via bit stream
- FiFo latency 12.8ys

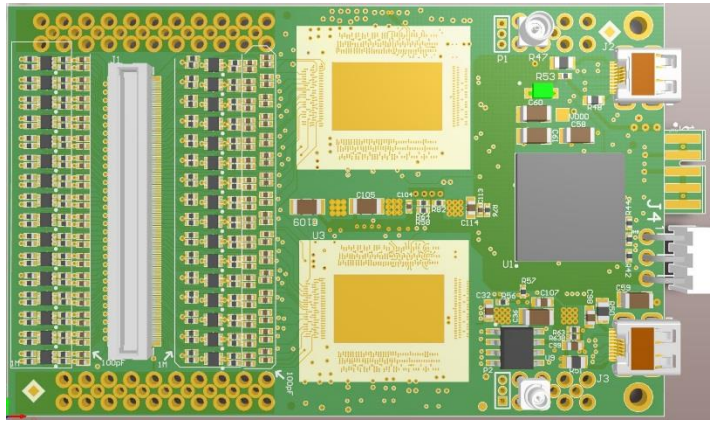


- max. 2x 1 Watt (VMM) + 0.9Watt (LDOs + FPGA) :
- reduce to ~ 2W by using DCDC and disabling unused drivers

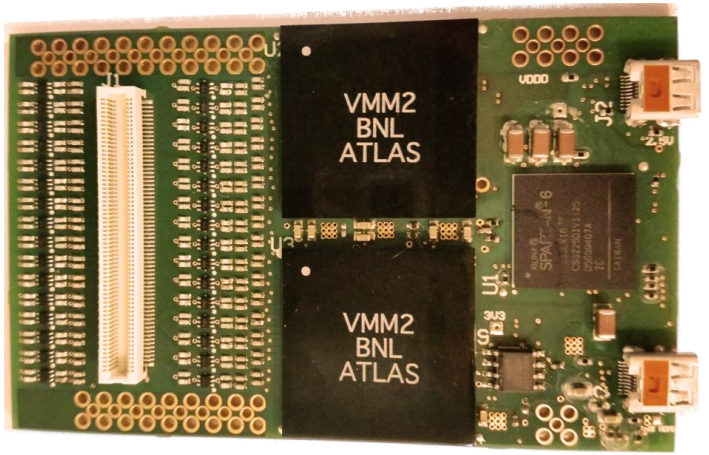
Who should / can use VMM SRS frontends

- **RD51 teams with high-rate requirement > 1kHz**
- **RD51 teams who have no access to APV**
- **TPC detectors with drift times up 12.8 us**

8-layer PCB (80 x 50 mm) RD51



Wire bond-PCB for VMM2 => VMM3



Previous BGA version VMM2

<u>VMM – SRS Applications (as far as we know)</u>

-ATLAS NSW (Mini-2.1): testbeams

-ESS Spallation source: neutron detectors

-Tsukuba Tech: modified VMM for ALICE FOCal

-T2DM2: MUST detector @ LSBB

- VMM1, VMM2, VMM3 is an ASIC developed by ATLAS/BNL

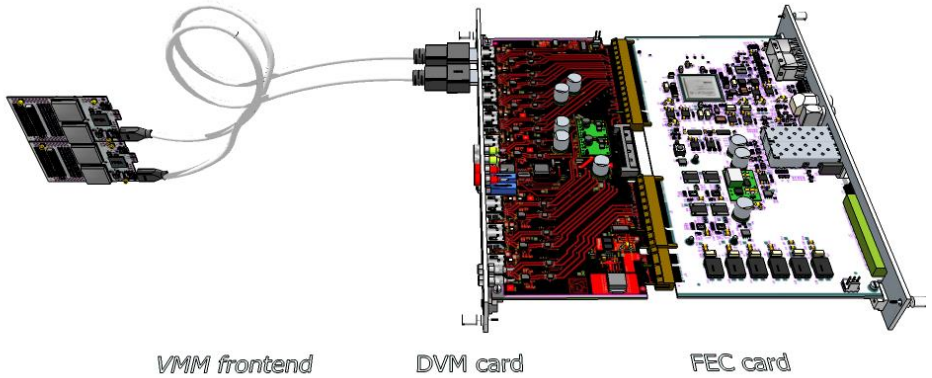
DVMcard: SRS adapter for VMM

Status: being validated in GDD lab

Dcard = Digital adapter for SRS classic

New:

DVMcard for VMM -128 hybrids



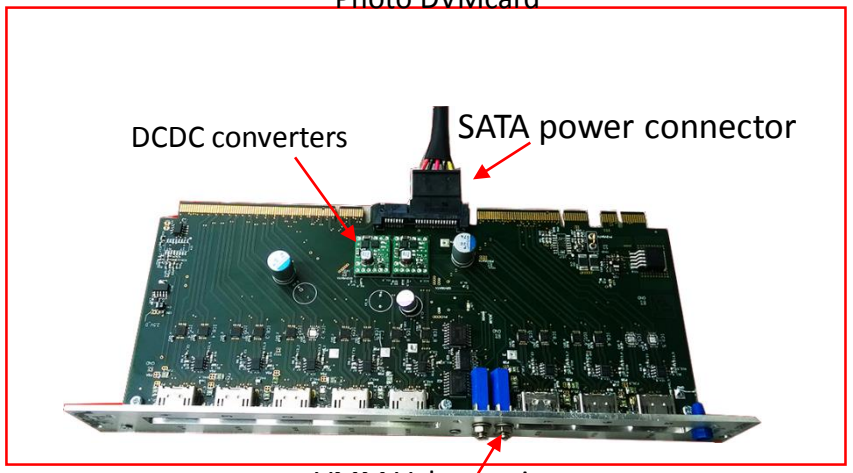
8 x HDMI ports for VMM-128

- 2 power lines 2 x P2, 1 x P1 , frontend potentiometers for P2 adjustment
- 2 downlinks (clock, configuration)
- 2 uplinks (data, trigger)

Features DVM

- 8 x HDMI ports, LVDS and power
- Power for 8 VMM-128 (1.6 + 14 Ampere)
- Power lines P1+P2: solid-state fuses/LED indicators for each port
- SATA power from ATX cable
- Current and voltage monitoring via I2C

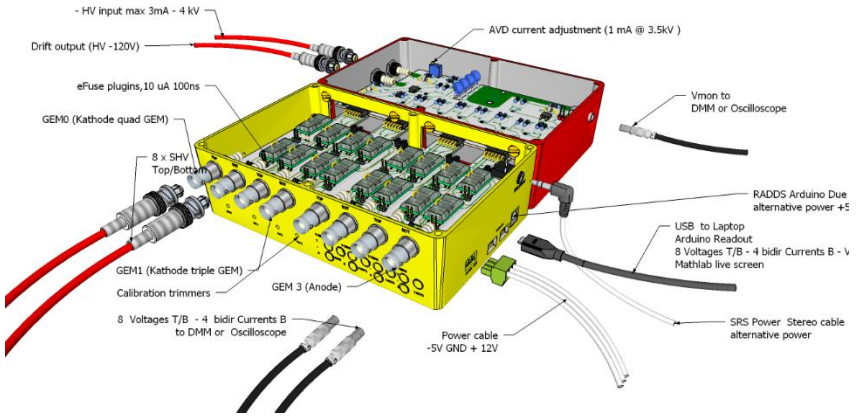
Photo DVMcard

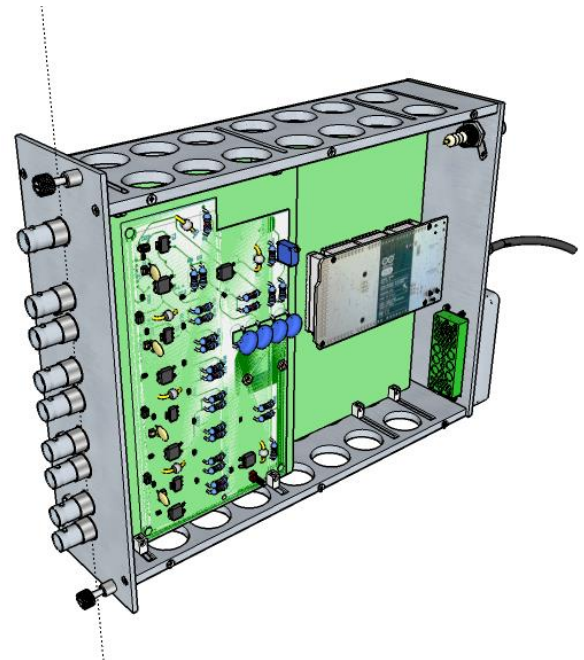


AVD: Active Voltage Divider (ongoing)

- Combine 4 AVD-related prototype units
  AVD + eFuse + U-I monitoring + external HV supply

  ➔ **one single NIM module for MPGD HV**
- AVD generates current-independent MPGD fields on up to 5 electrodes
- AVD board: 5 user-defined Voltages : Drift, G1, G2, G3, (G4)
- Integrated, program-controlled HV generator for up 5 kV
- Voltage and Current Monitoring for kV (5kV, +-2V) and pA (1uA , +-100 fA)
- No batteries, no chargers, for monitoring hardware
- eFuse-ed electrode current (spark and short-circuit safe sectors)
- option for up to 6 sectors / electrode with CERN defined HV Lemo connector
- Arduino control and readout via Labview GUI
- Prompt monitoring via Oscilloscope outputs





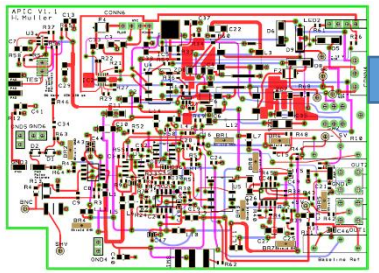
APIC : Analogue Pickup Amplifier

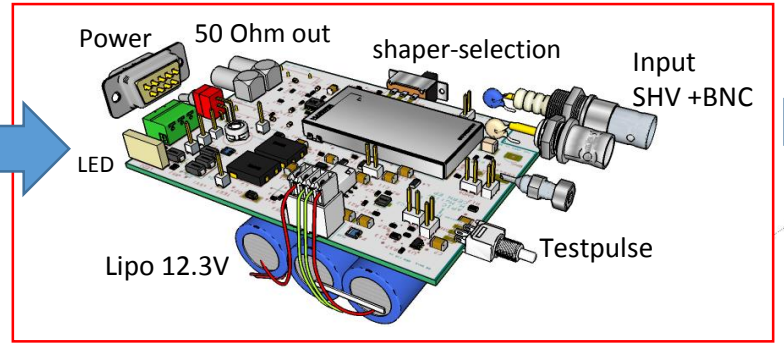
a (solar) battery operated preamp-shaper box for detector meshes

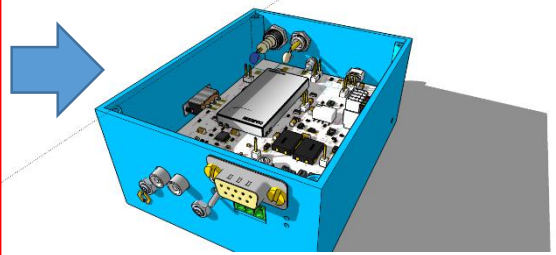
- Re-design of 2015 proto-versions
- Power : Solar or NIM Power (DSUB-9)
- Hand-held metal box
- Spark protected pos/neg input
- 2 default peaking times selectable: 200ns* / 1us (switch)
- Gain range 1- 200 (potentiometer), analogue out
- Complementary 50 OHM output with baseline shift (potentiometer)
- Integrated test pulse (pushbutton)

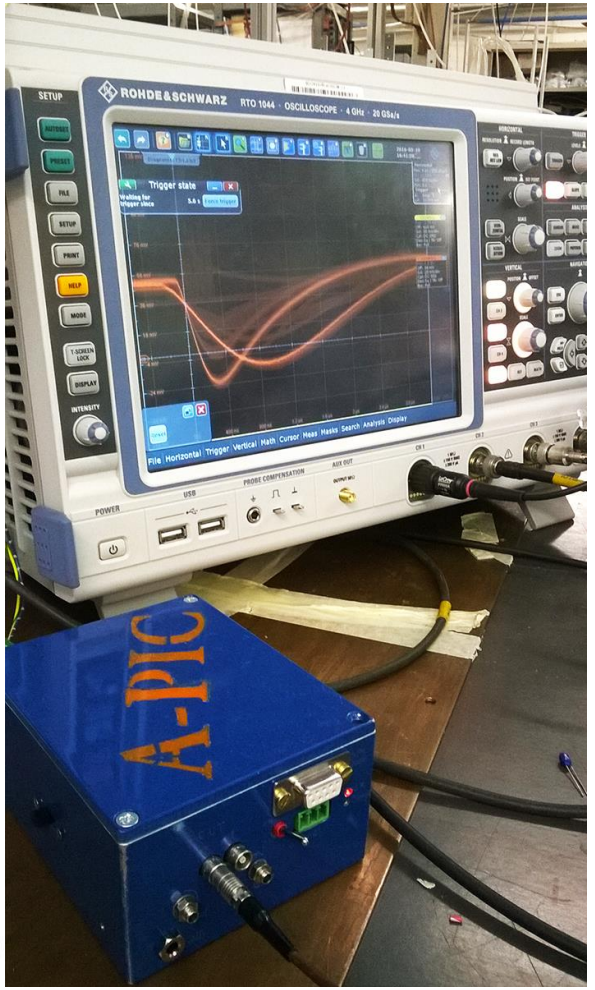
*different peaking times possible

4 layer PCB

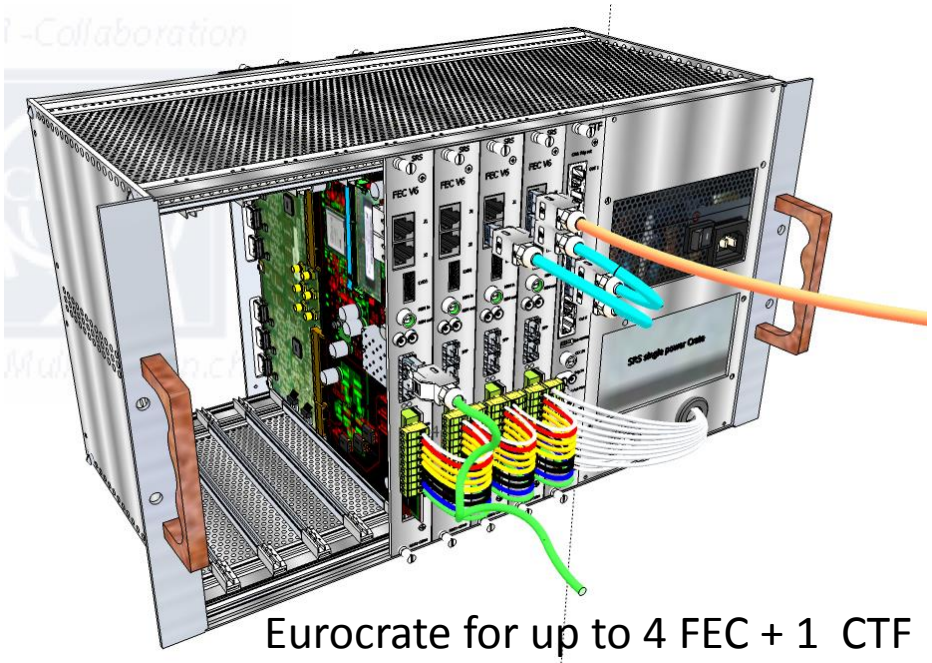








Eurocrate / ATX filter V2



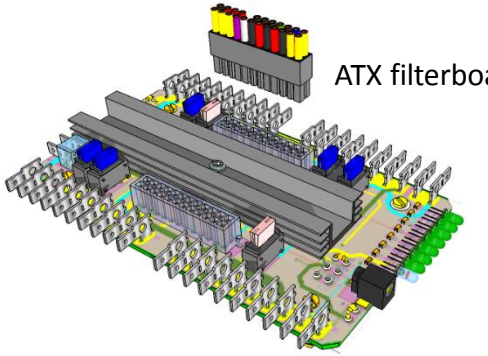
Eurocrate for up to 4 FEC + 1 CTF

Severe quality problems with SRS Eurocrate V1 :

CERN store stopped sales

<u>Eurocrate 2 features</u>

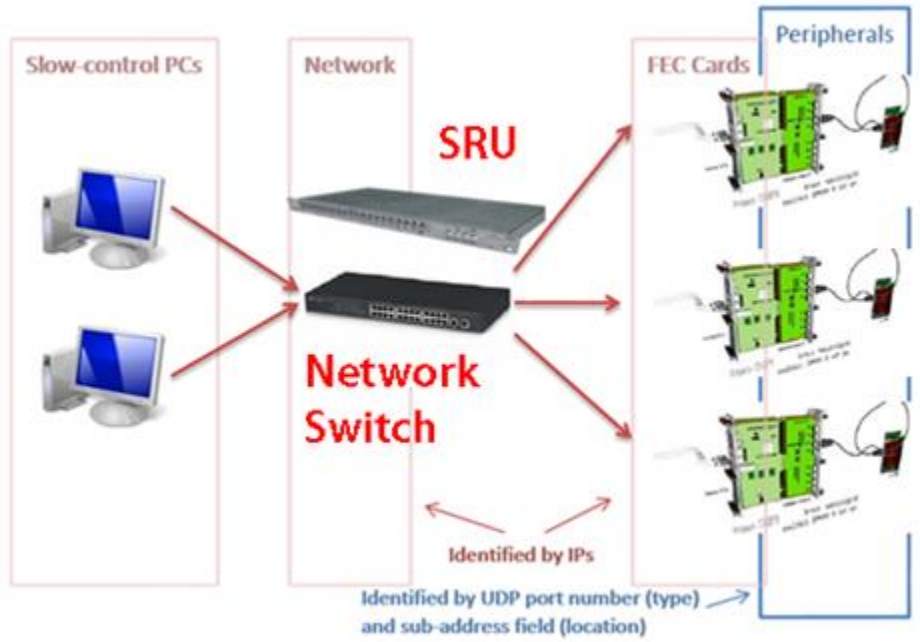
- > 40 Ampere on 3V3 (for up to 64 APV hybrids)
- ATX filter V2 with integrated -5V PSU and resettable fuses
- CTF power connector
- SRU power plug
- 5 slots (4 x FEC + 1 x CTF)
- Aux. power panel (+12,+5,+3.3,-5 V- fused) with 2mm Banana jacks

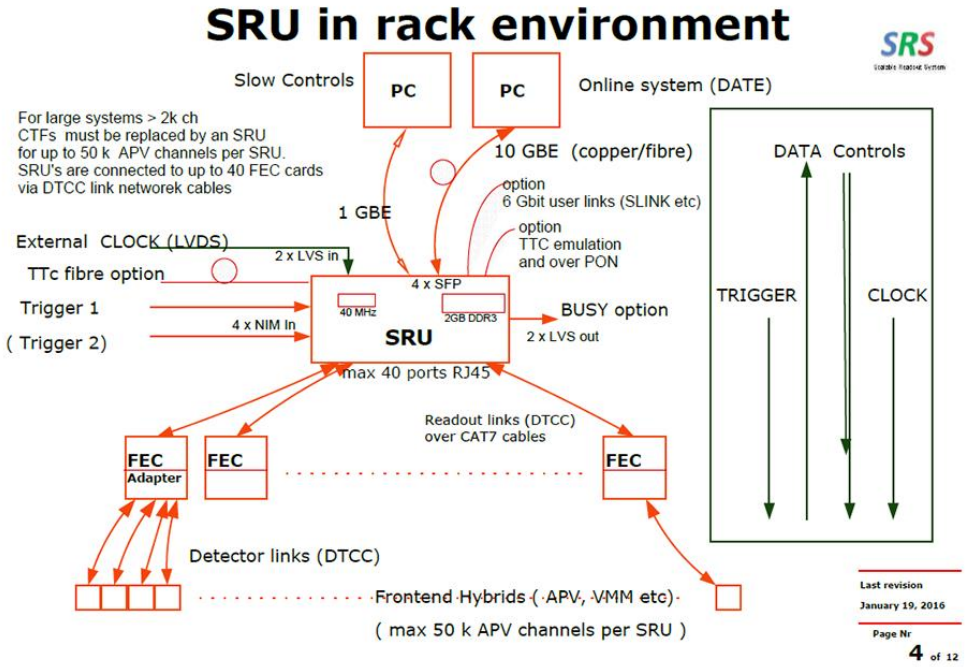


ATX filterboard

SRU V3: Scalable Readout Unit

Compared to a Network switch, the 1U SRU box distributes clock, trigger and slow controls via point-point DTCC links. DTCC protocol between SRU and FEC's distributes a common, very low-jitter clock + low-latency trigger signal to the frontends. Data from up to 40 FECs or Blades can add up to a tens of Gbps. SRUs-3 boxes are equipped with 10 Gbit Ethernet connecting a single PC or a PC-farm. An optional DDR3 buffer (2GB) can be plugged for 2nd level trigger applications.

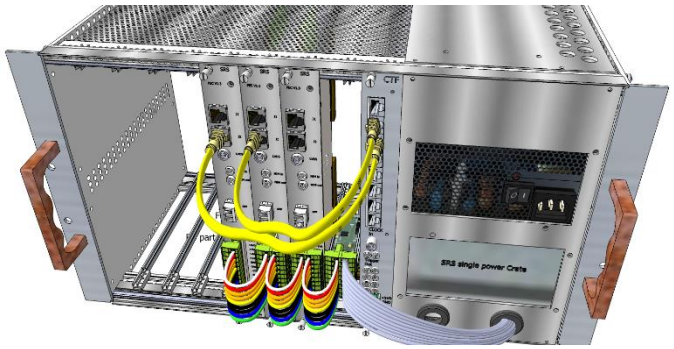


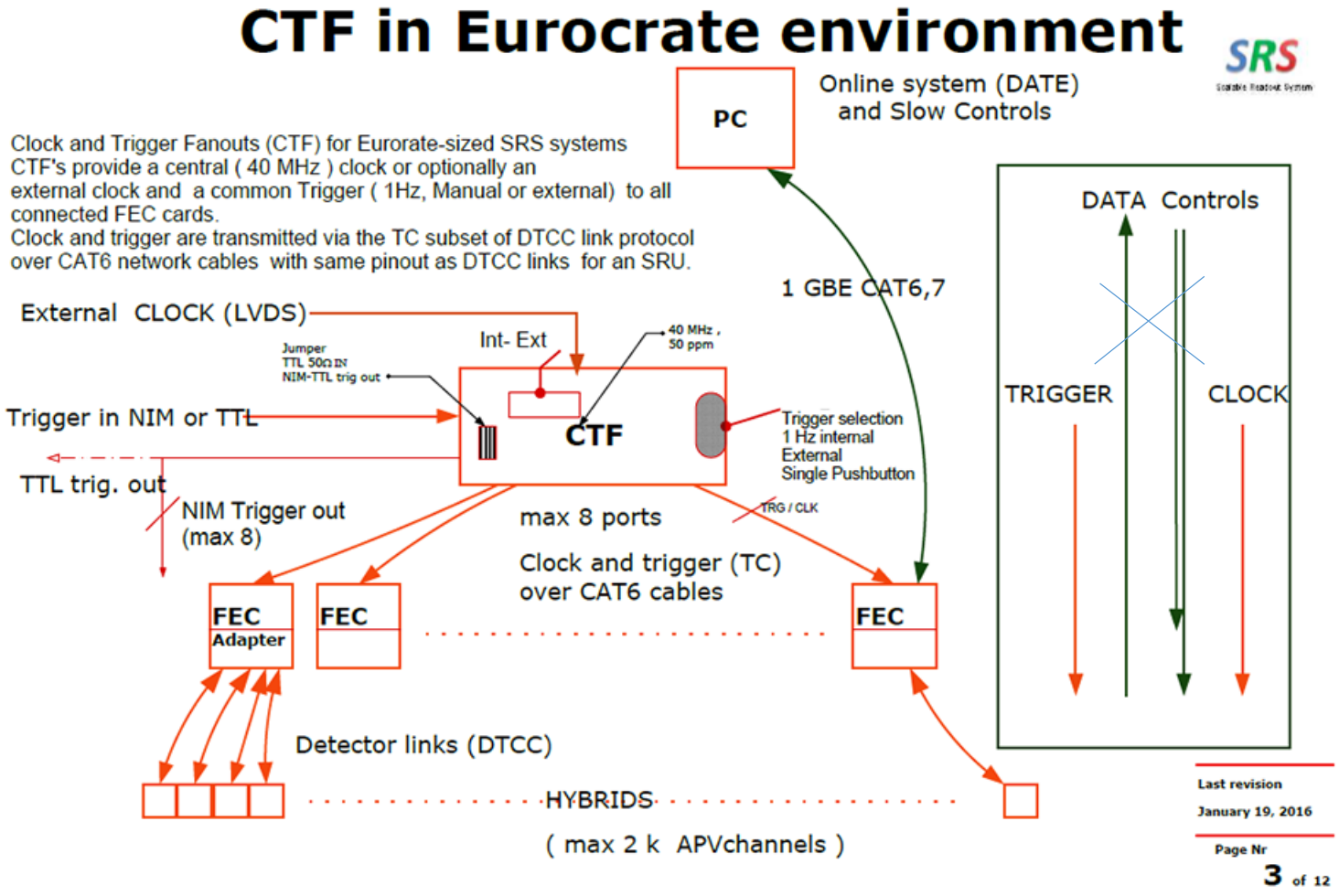


CTF V2.1: Clock-Trigger Fanout for FECs

"simple version of SRU"

- Revised CTF for low jitter trigger fanout from NIM input
- NIM –IN trigger fanout to NIM-OUT + RJ45
- RJ45: same pinout as (SRU) DTCC link for clock and trigger





Fi-Femto: Fast Insulated Femtometer (upgrade)

Upgrade of Femtobox-1
(I = 10fA … 1 uA / Q = 1fC … 1 pC / R = 45M…10 TeraOHM)
➔

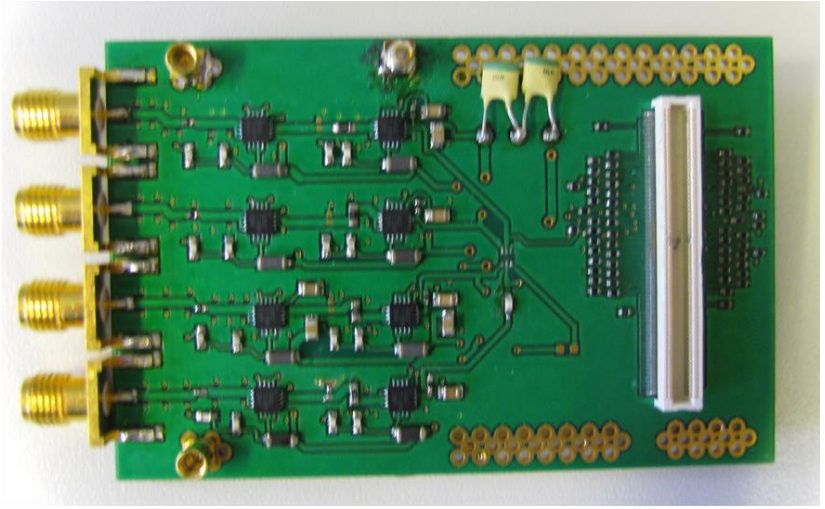
- higher Bandwidth 25-50 MHz for direct analogue output
- combined neg. / pos. input
- dynamic range auto-range (no more selector switches)
- Solar re-charge option

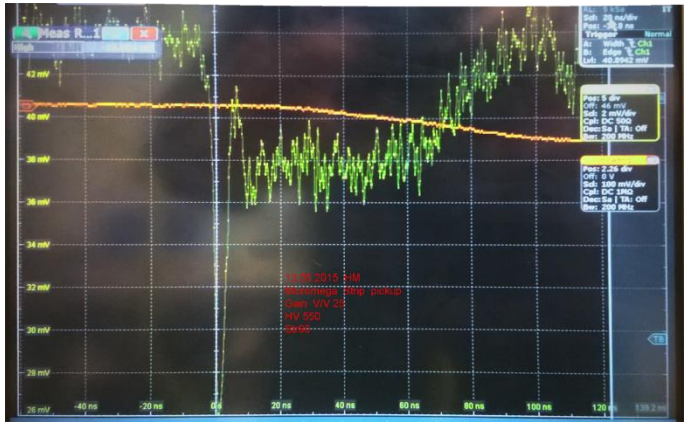
Femtobox -1

Application 1: Battery-operated , NIM or solar-rechargable
Femto-box 2 with prompt analogue readout both polarities
Application 2: HV insulated (!) analogue readout of pA currents
from 3 kVolt detector potential @ 100ns /point

QCA: 4-ch current amplifier (planned revision)

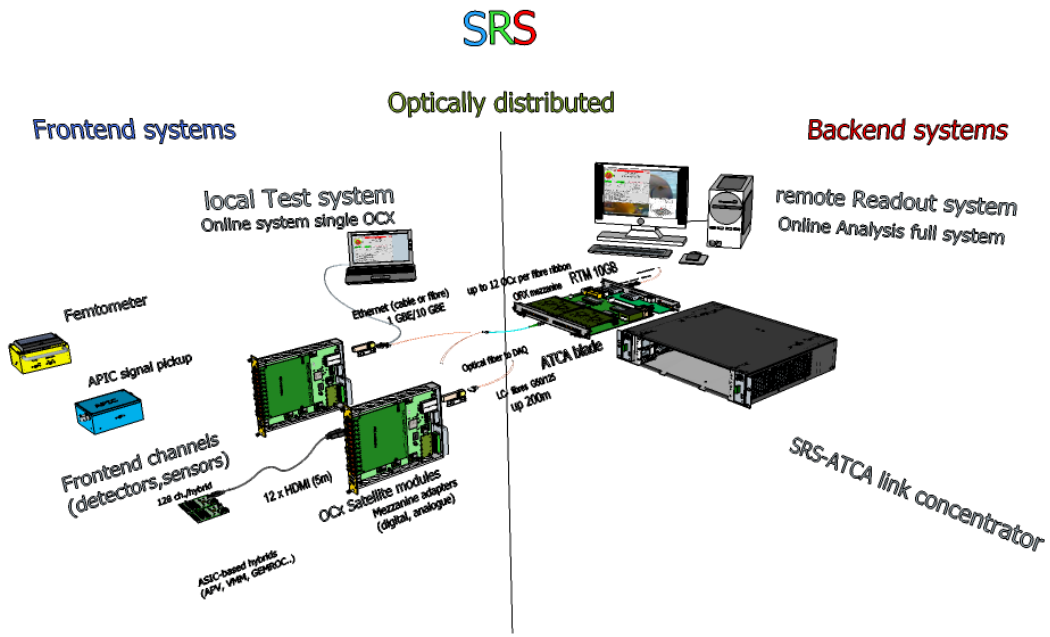
- For study of MPGD avalanche charge dynamics on neighboring electrodes
- Based on previous QUAD amplifier with 2 GHz, 50 OHM gain 20 V/V amplifiers
- New design with 4 GHz TIAs: (current-to-voltage converters)
- Voltage/Current gain = 2 x 10**4
- Leakage current 3 fA
- QCA card with Panasonic connectors on detector and SMA outputs





MicroMega single strip: a direct dQ/dt measurement with
Quad amplifier proto: electron peak (few ns) followed by ion pulse (60ns)

Optical SRS (ongoing)



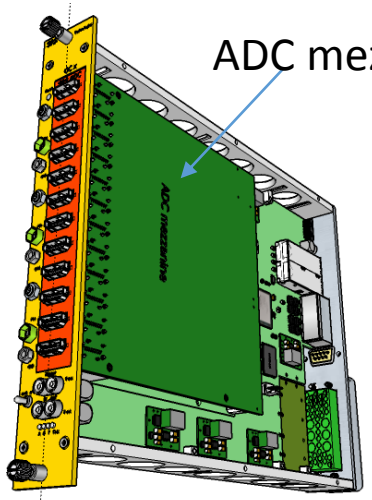
COx : copper to optical X-box for SRS frontends (APV or VMM)

- redesign of "OCx" box as NIM module
- For use with single SRS mezzanines (APV, VMM, ..)
- Embedded processor with 10 GB-ethernet (instead of FPGA)
- NIM coincidence/OR logic included in NIM module

ORx: optical receiver card

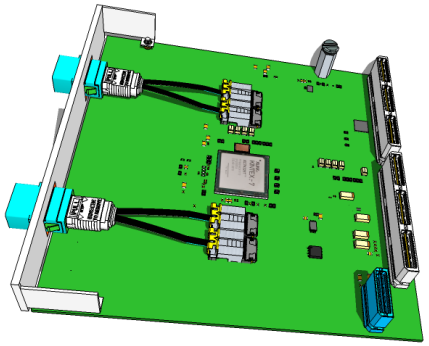
- Firefly ATCA mezzanine for 12(24) fibres from COx satellites up 200m

COx NIM module



ADC mezzanine

ORx FireFly mezzanine



SRS production licence

Licencies and legal aspects of Intellectual Property are handled by CERN KT

- Companies to request licence from CERN for direct sales of SRS
- List of ca 20 potential SRS hardware items to be updated yearly
- Contributions from RD51 teams to IP possible
- Royalties on sales to non-RD51 teams apply
- SRS firmware and software not part of licence but controlled

SRS Purchase & Procurement situation

Since 2011, CERN store is the major provider for SRS

Progressively unsatisfactory:

- Major efforts for complementary inhouse productions (SRU, CTF, ATX filter board, Eurocrates ..)
- Major efforts on acceptance testing (i.e. APV hybrids) and after-sales support (ADC cards, FECs, Crates …)
- Major administrative barriers for SRS purchase by RD51 teams without team account
- No solution that makes everybody happy visible