SPS RF signal distribution using White Rabbit

Eva Calvo

(with the collaboration of T. Wlostowski, J. Serrano and M. Rizzi)

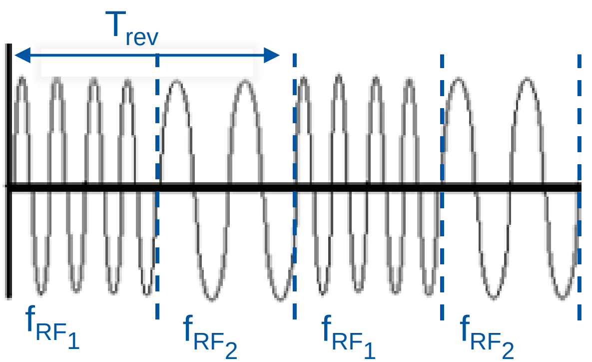
Outline

- Motivation and objectives
- Beam time of flight compensation algorithm
- The Distributed Direct Digital Synthesis (D3S) over WR
- The new layout proposed for the distribution of Wide BW RF signals over WR
- Conclusions and planning

Motivation and objectives

- Most of the SPS and LHC beam instrumentation systems use the BST (Beam Synchronous system) → Trev, Bclk + triggers (capture triggers, post-mortem triggers, etc.) + messages (beam intensity, acc. mode, etc.)
- However, BST does not fulfil some needs:
  - Can not lock to FSK modulated SPS RF signal during ions fills.
  - It lacks of beam time of flight (TOF) (and propagation delay) compensation feature
- These two points have motivated the development of this project. CO/HT committed to help by providing:
  1) Bunch clock and Trev
     - With TOF compensation
     - Synchronous during ion fills.
  2) Rms jitter <0.5ns (between FBCT signal and provided Bclk).
  3) UTC time
- Prove of concept to show the potential of a future BST&GMT upgrade system based on WR.

FSK modulation of the RF during ions ramps



Because ions arrive with too low energy to the SPS, the f_{RF} signal at the SPS cavities are FSK modulated.

During the half turn that the beam crosses the RF cavities:

- $f_{RF} = f_{RF_1}$ (f_{RF_1} where follows the acceleration ramp).

During the other half turn:

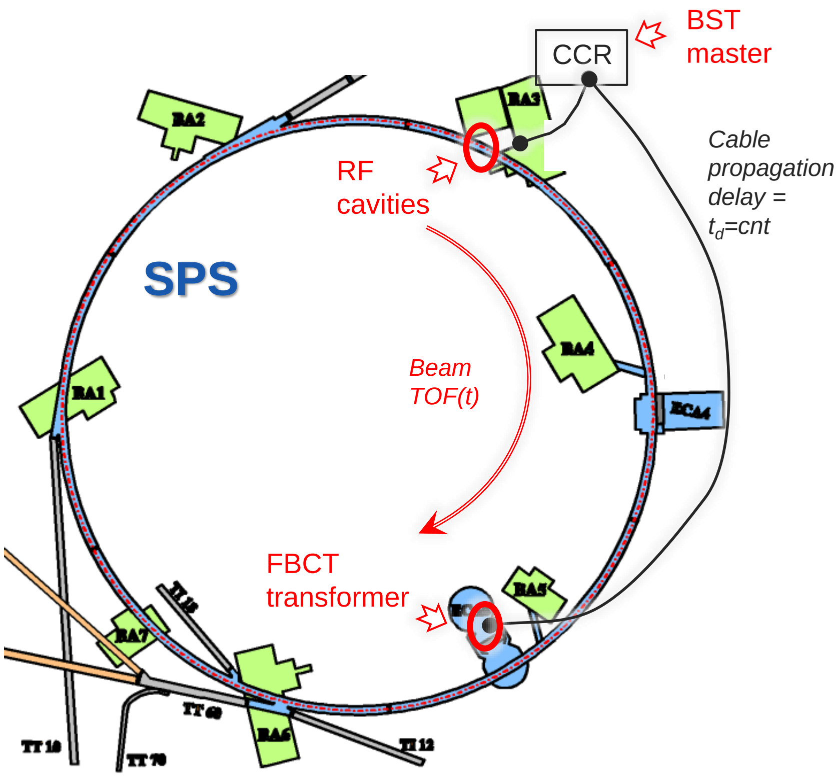
- $f_{RF} = f_{RF_2}$ (where f_{RF_2} is such, that a complete revolution will have 6420 full periods).

	f_{RF1} [MHz]	f_{RF2} [MHz]	f_{AVG} [MHz]	$f_{RF1}/5$ [MHz]	$f_{RF2}/5$ [MHz]	f_{REV} [kHz]
Injection	199.927	197.091	198.509	39.985	39.418	42.967
Flat bottom	From 199.927 to 200.222	From 197.091 to 196.796	198.509	From 39.985 to 40.044	From 39.418 to 39.359	42.967
Flat bottom to transition	200.222	**196.796** MHz to 200.222	From 198.509 to 200.222	40.044	From 39.359 to 40.044	From 42.967 to 43.338
Transition to top energy	From 200.222 to 200.392	From 200.222 to **200.392**	From 200.222 to 200.392	From 40.044 to 40.078	From 40.044 to 40.078	From 43.338 to 43.374

BW~3.5MHz

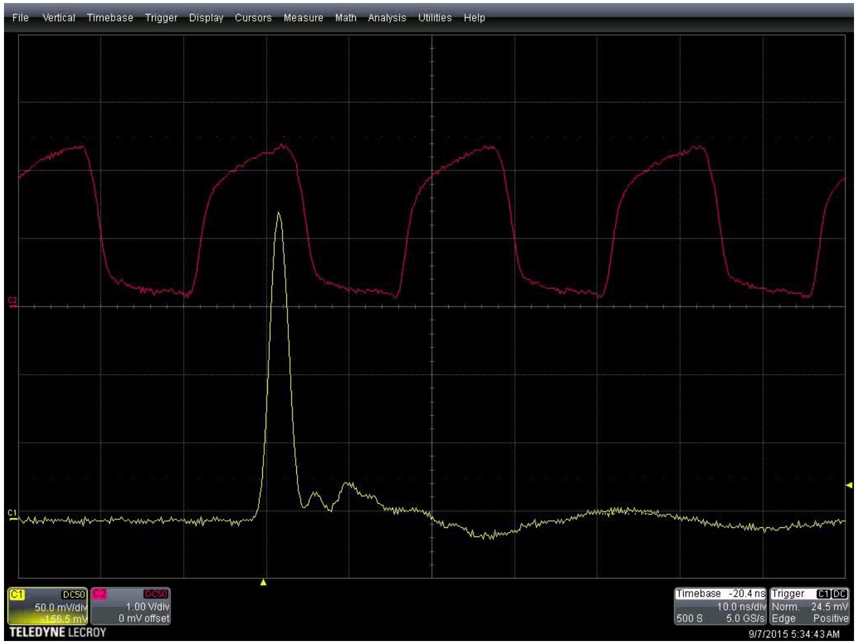
⚠ BST PLL can not lock to the FSK modulation. To mitigate the impact, RF sends to the BST master f_{AVG} instead of the real f_{RF}. This prevents aligning the bunch clock better than 9.25ns. (EDMS 1410586)

Time of flight (TOF) compensation



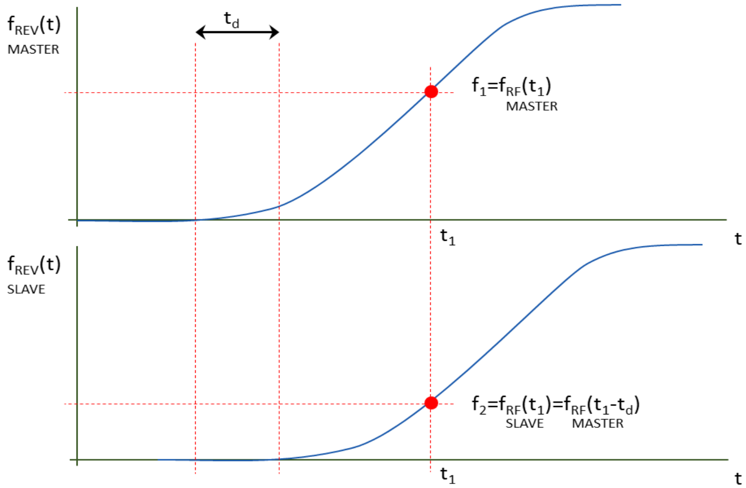
The beam travels from BA3 to BA5 in a certain Time of Flight (TOF) which depends on its energy.
TOF from BA3->BA5 ~ 1/3 Trev.

The BST signal coming from the CCR travels through a cable with a constant propagation delay (t_d).
(With WR system this delay will be the system latency).



The new SPS RF distribution system should provide a bunch clock (and Trev) synchronous to the beam at each node. ⇨ *It should continuously correct φ(t) (* Ideally, without an priory knowledge of the ramp cycle).*

Time of flight (TOF) compensation



This curve can vary among different cycle types.

Master node:

$$x_{RF_{BA3}}(t) = A \cdot \sin(2 \cdot \pi \cdot f_{RF}(t) \cdot t)$$

Slave node

$$\begin{aligned} x_{RF_{BA5}}(t) &= x_{RF_{BA3}}(t - t_d) \\ &= A \cdot \sin\big(2 \cdot \pi \cdot f_{RF}\,(t - t_d) \cdot (t - t_d)\big) \\ &= A \cdot \sin\big(2 \cdot \pi \cdot f_{RF}(t - t_d) \cdot t - \varphi_{BA5}(t)\big) \end{aligned}$$

To make the slave synchronous to the beam

$$\begin{aligned} x_{RF^{*}_{BA5}}(t) &= x_{RF_{BA3}}(t - t_{TOF}(t)) \\ &= A \cdot \sin\big(2 \cdot \pi \cdot f_{RF}\,(t - t_{TOF}(t)) \cdot (t - t_{TOF}(t))\big) = A \cdot \sin(2 \cdot \pi \cdot f_{RF}\,(t - t_{TOF}(t)) \cdot t - \varphi_{TOF}) \end{aligned}$$

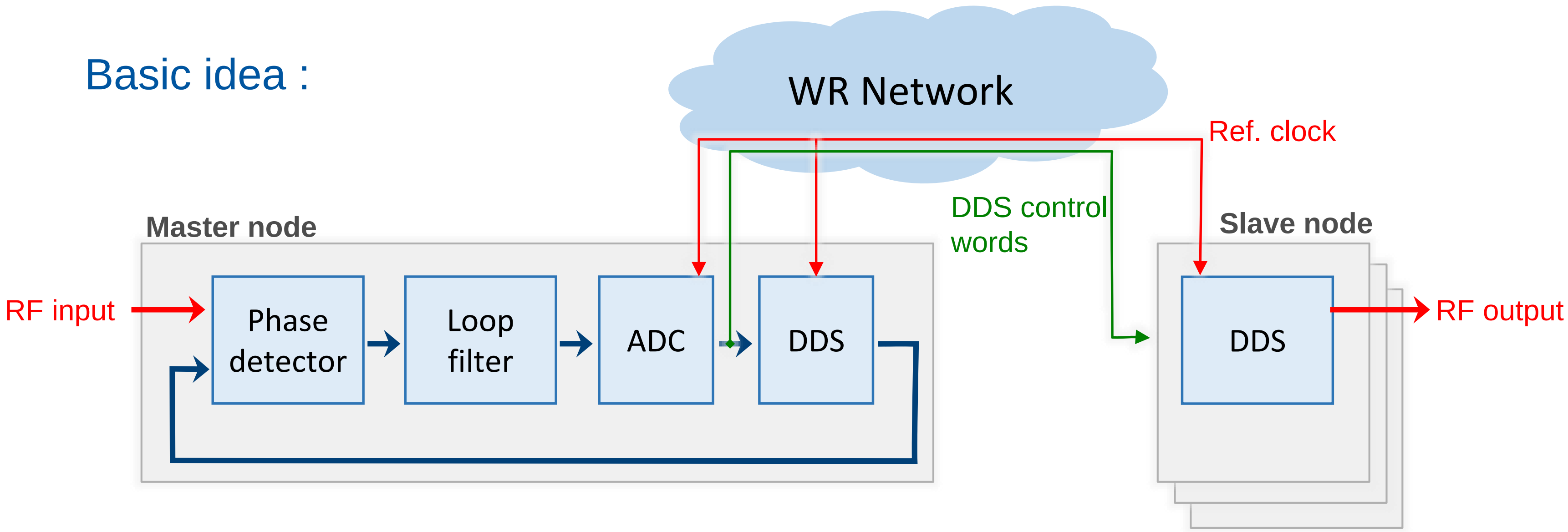
* Assuming: $f_{RF}\,(t - td\,) \approx fRF(t),\ since\ {}^{\delta f_{REV}}/_{\delta t} < 0.6\ Hz/ms$, so about ${}^{\delta f_{RF}}/_{\delta t} \sim 1.4\ ppm\ in\ about\ 100us$

We need to apply to the BA5 reconstructed signal a phase correction:

$$\theta(t) = \varphi_{TOF} - \varphi_{BA5}(t) \approx +2 \cdot \pi \cdot \left(\underbrace{-h \cdot \frac{distance_{BA3 \rightarrow BA5}}{SPS\ Circ.}}_{cnt} + \underbrace{\mathrm{h} \cdot \mathrm{f_{REV}}(\mathrm{t} - t_d) \cdot \mathrm{t_d}}_{\text{Varies with time *}} \right)$$

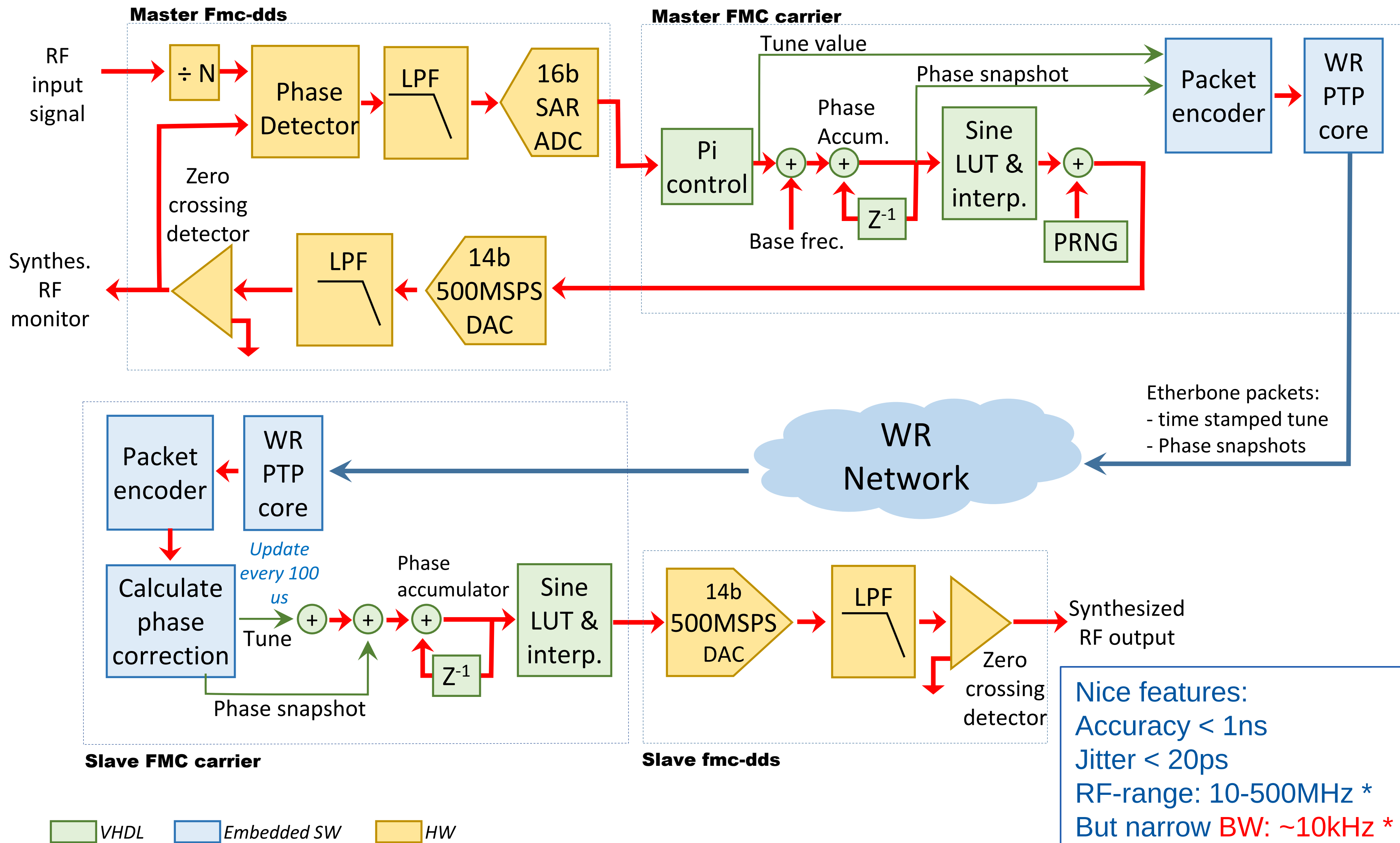
Distributed Direct Digital Synthesis over WR (D3S) Layout

Basic idea :



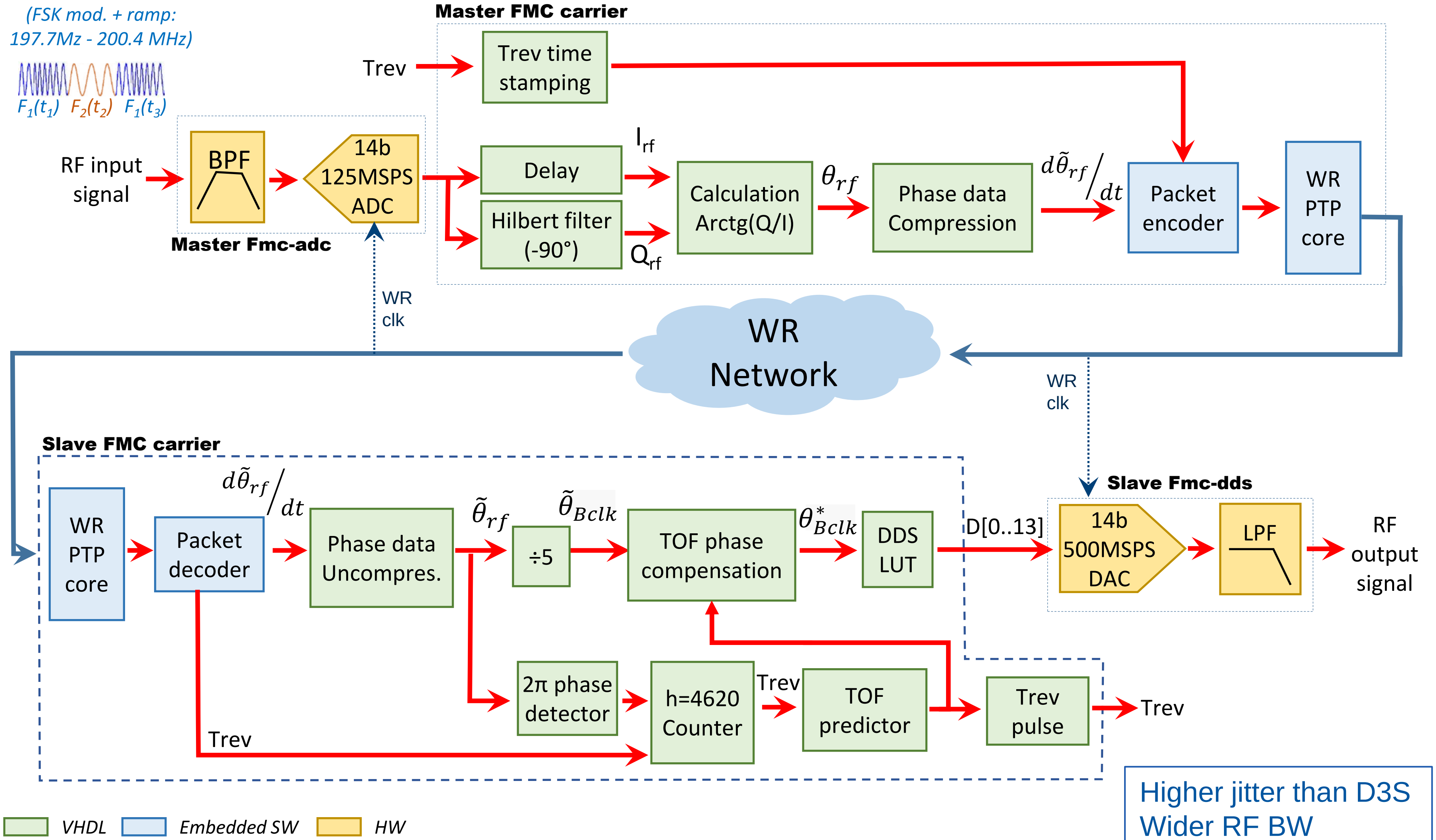
- The master node keeps a local DDS phase-locked to the RF ref. input.
- It broadcasts the DDS tuning words calculated by the PLL over the WR network.
- The slaves feed the received data into their local DDS.
- Since the reference clocks are identical (sub-ns accuracy and ps jitter) the slave reproduces an exact copy of the RF received by the master node.

Distributed Direct Digital Synthesis over WR (D3S) Layout



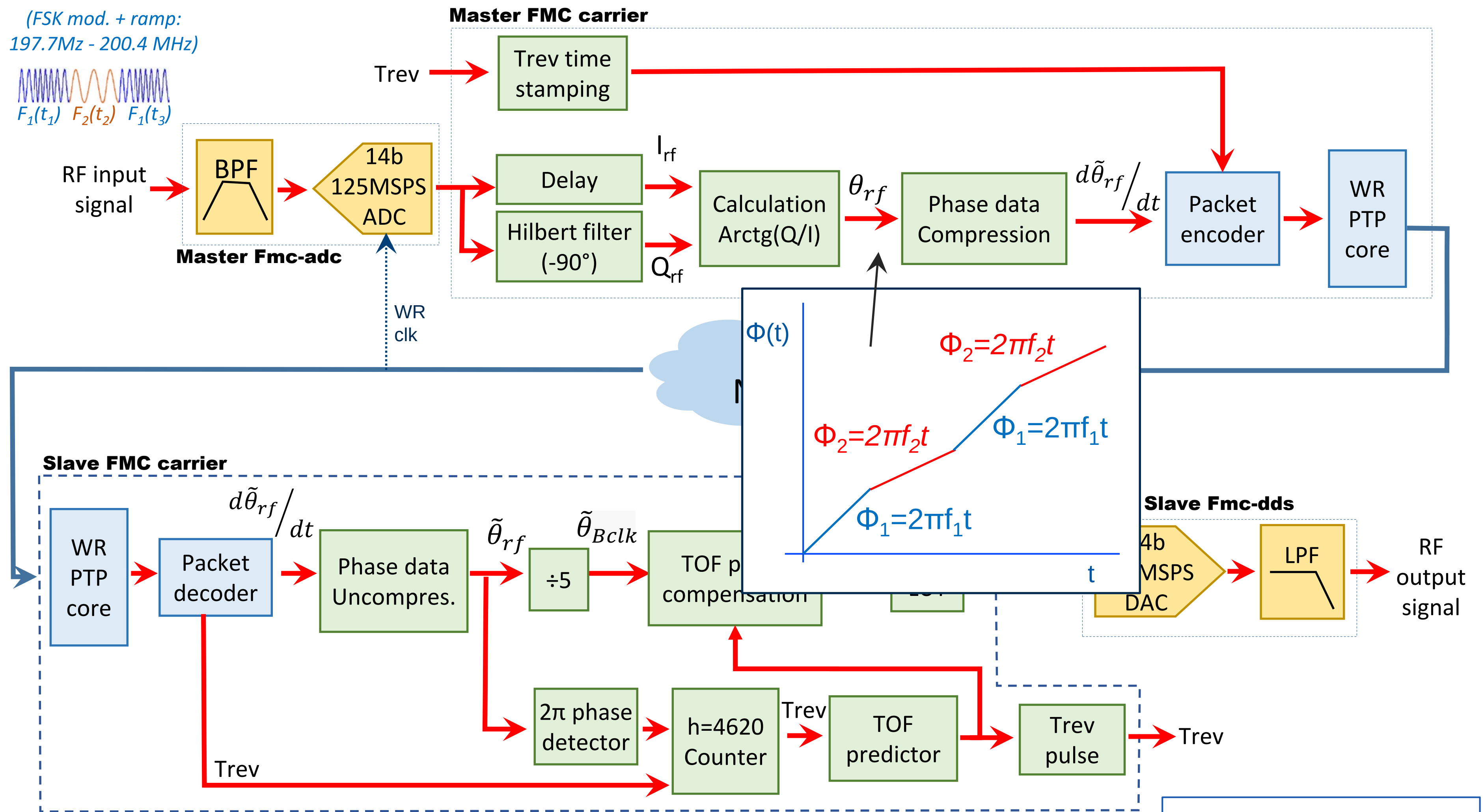
Nice features:
Accuracy < 1ns
Jitter < 20ps
RF-range: 10-500MHz *
But narrow BW: ~10kHz *

New layout for SPS f_{RF} distribution



Higher jitter than D3S
Wider RF BW

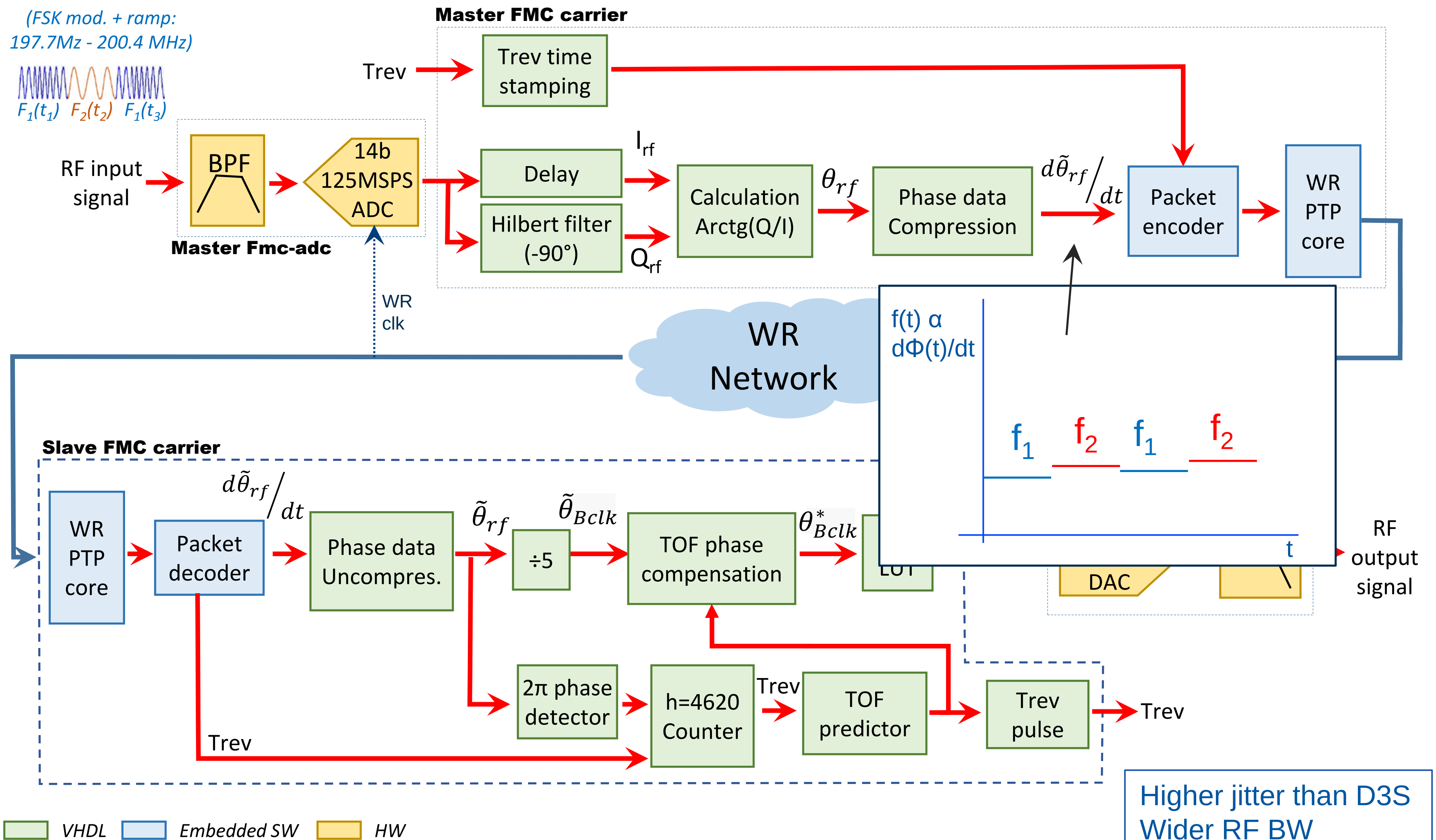
New layout for SPS f_{RF} distribution



VHDL | Embedded SW | HW

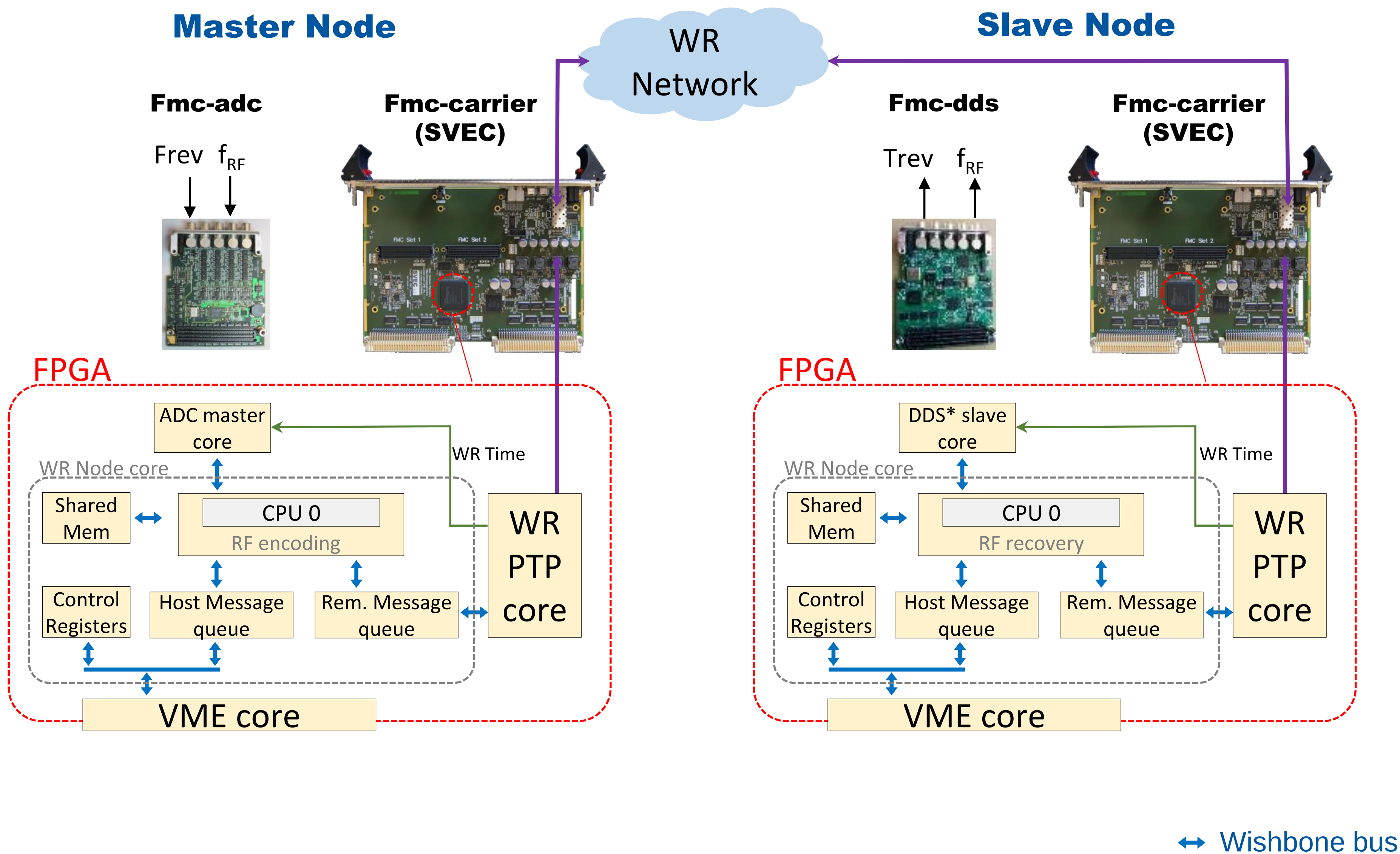
Higher jitter than D3S
Wider RF BW

New layout for SPS f_{RF} distribution



Higher jitter than D3S
Wider RF BW

New layout: D3S for WB RF signals distribution



Conclusions and planning

Conclusions:

- The D3S project was developed having in mind the distribution of timing signals like Bclk, Trev.
- New needs (large bandwidth and TOF compensation) have required to modify the layout. Requiring HW and GW changes w.r.t. the initial project.
- The TOF comp. alg. has been presented
- As well as the new proposed layout allowing to increase the BW of the signals to be transmitted.

Planning:

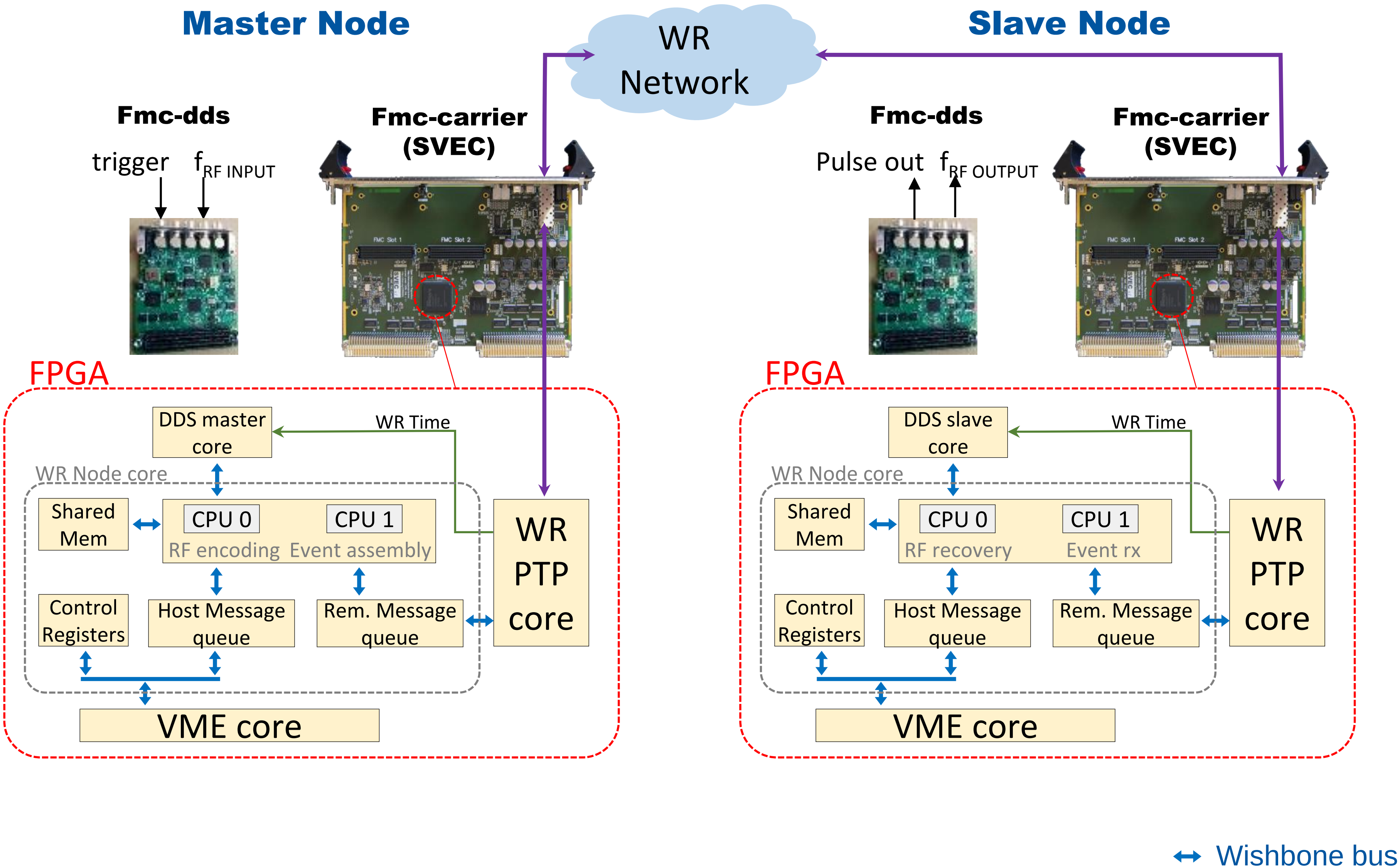
- The VHDL of the master node is done.
- The Fmc-adc cards are temporally modified by hand.(New circuits will be produced).
- We are currently working on the VHDL of the slave node.
  - Still to implement the TOF compensation algorithm.
- Next steps will be to test in the lab, BA3 and then BA5.
  - BA3 tests are estimated by the end of summer.

Thank you

WR introduction

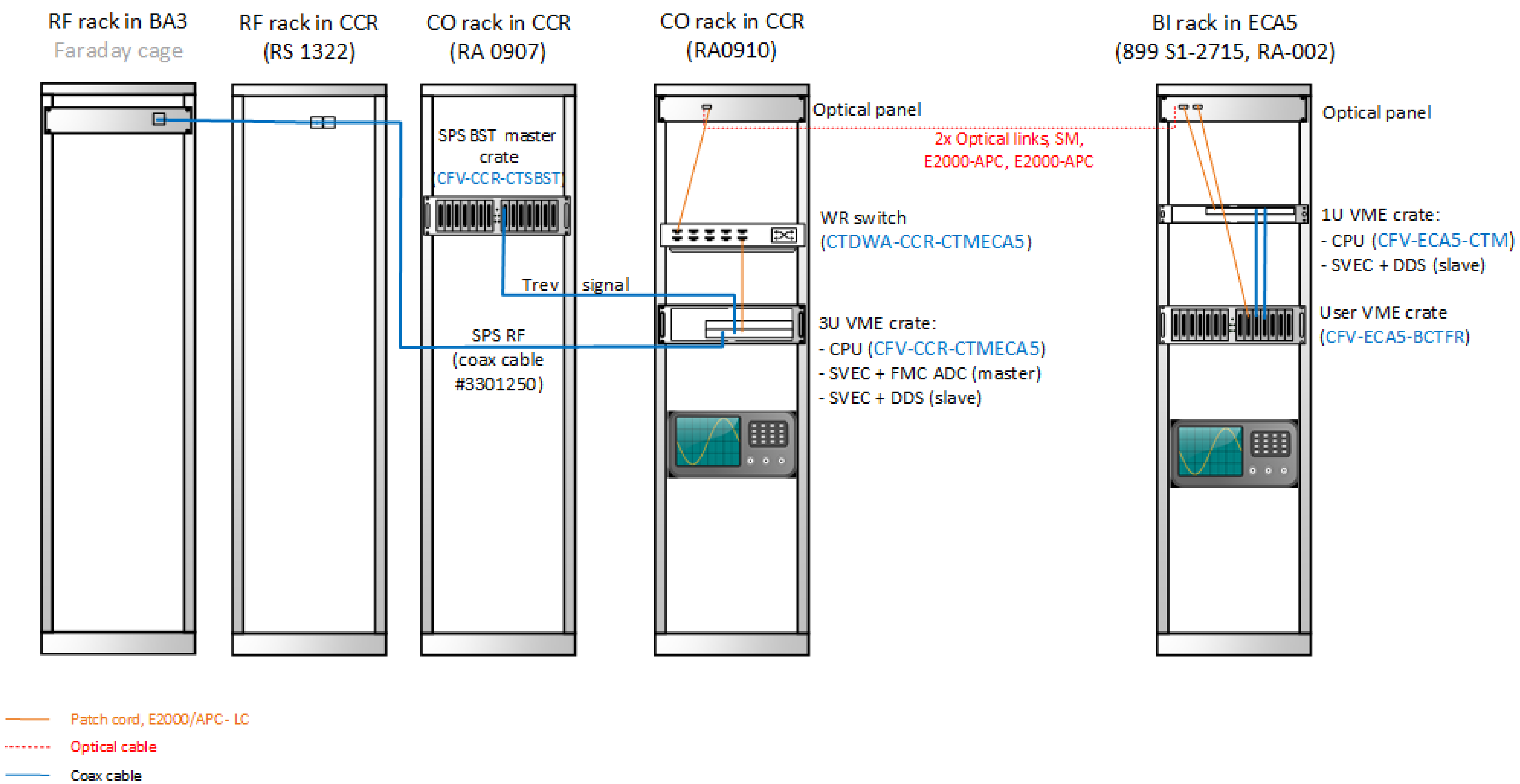
- It was initiated in 2008 to upgrade the GMT network.
- An extension of an **Ethernet** network which provides:
  - Transparently **sub-ns synchronization and ps jitter**
    - Layer-1 syntonization
    - Enhanced PTP protocol (IEEE 1588)
    - Precise phase tracking (DDMTD)
  - **Deterministic** data routing latency: a guarantee that a packet transmission delay between two stations will never exceed a certain boundary.
  - **Reliable** network: by means of topology redundancy (that reconfigures automatically) and data resilience with forward error correction schemes (FEC).
  - A **scalable and modular** platform: up to 2000 nodes, up to 10km of fiber links.
  - Ethernet features (VLANs) & protocols (SNMP).
  - 1 Gbps bandwidth
- Open design: HW, GW, SW. White Rabbit PTP core available.
- Already used in LIST, B-train, GSI, ESRF, etc.

D3S original scheme

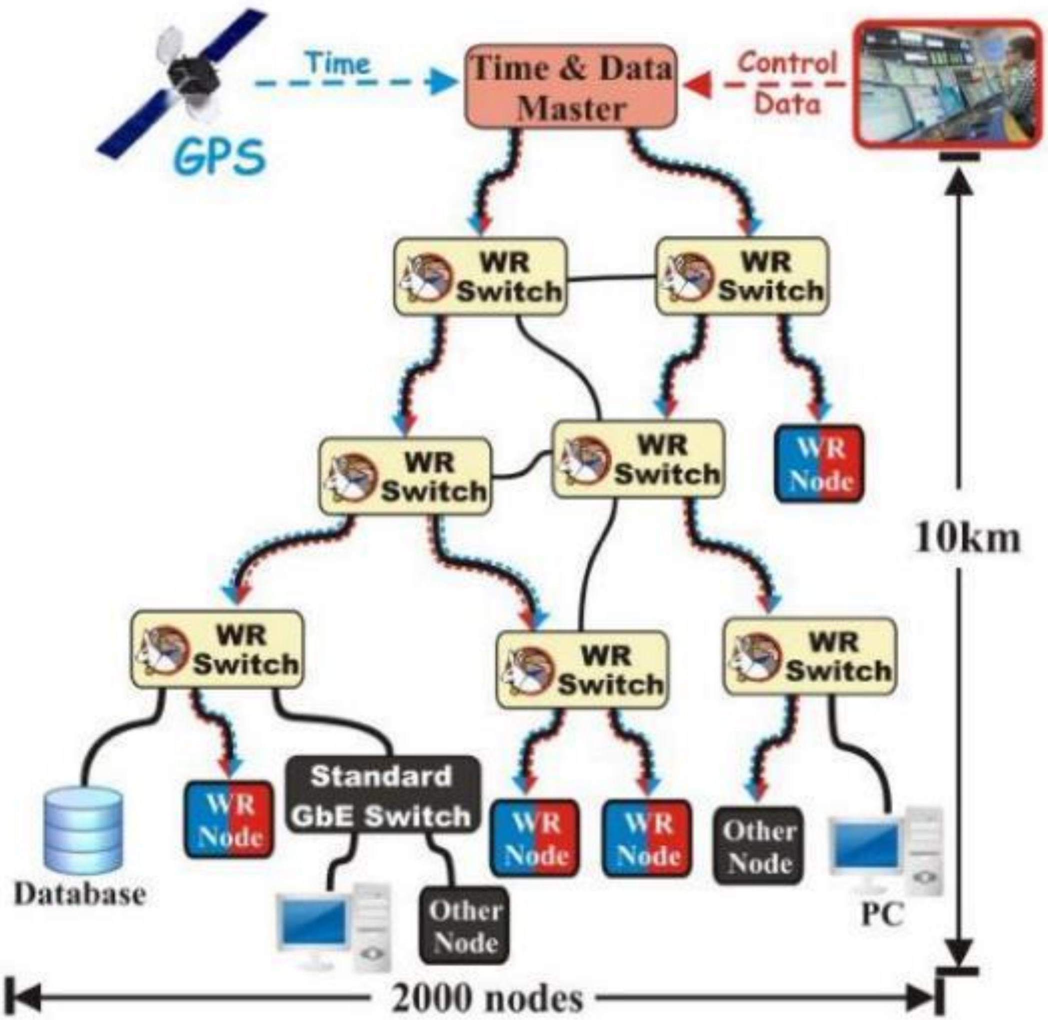


Infrastructure

SPS RF distribution over White Rabbit network from BA3 to BA5

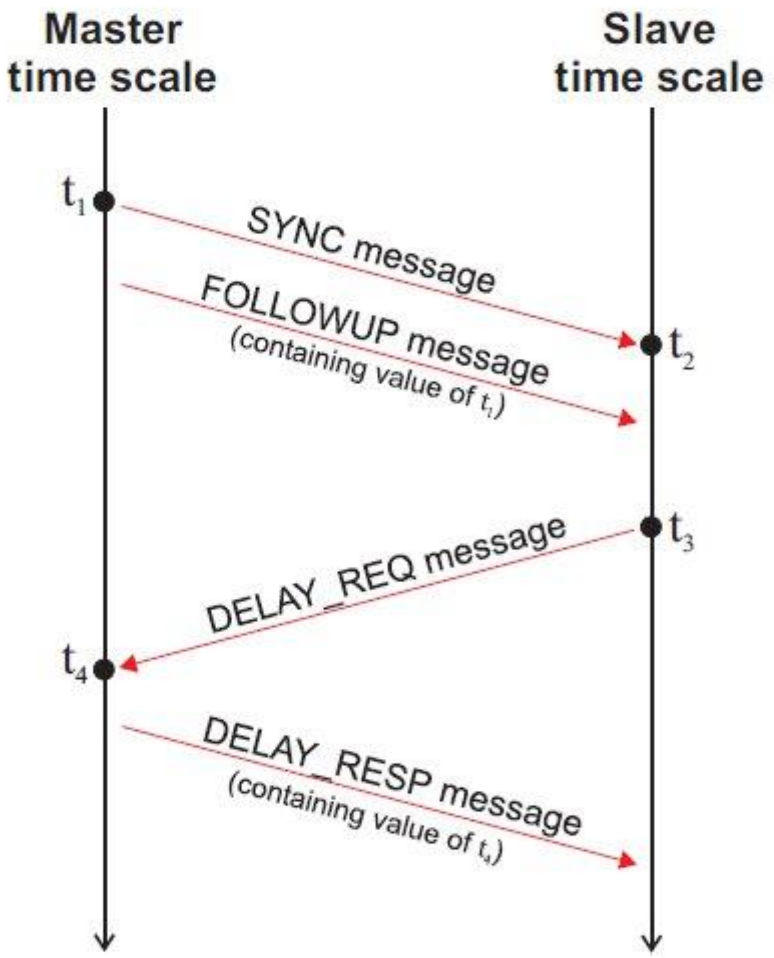


Network topology



- Upper bound latency by design < 10us for high priority data.
- On fail of link, the network reconfigures automatically, while loosing maximum of 2 frames.

PTP Protocol (IEEE 1588)



Having values of t1…t4, slave can:

- calculate on-way link delay:

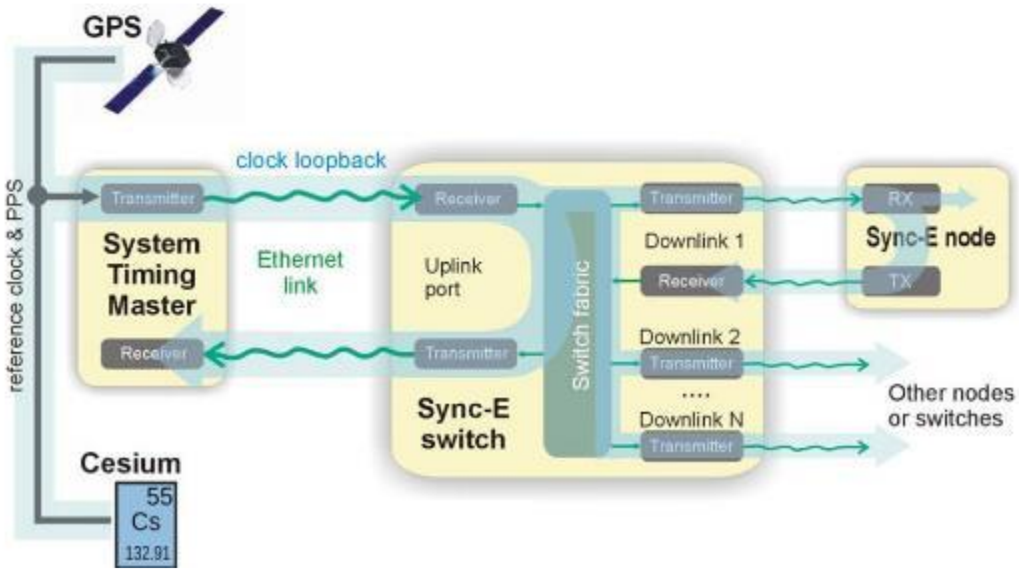
$$\delta_{ms} = \frac{(t_4 - t_1) - (t_3 - t_2)}{2}$$

- syntonize its clock rate with the master by tracking the value $t_2 - t_1$
- Compute clock offset:

offset = $t_2 - t_1 + \delta_{ms}$

Enhanced PTP

- The clock is encoded in the Ethernet carrier and recovered by the chip (PHY)



- Common clocks allow the use of precise phase measurement techniques (DDMTD) to improve the accuracy of the PTP timestamping and phase tracking.