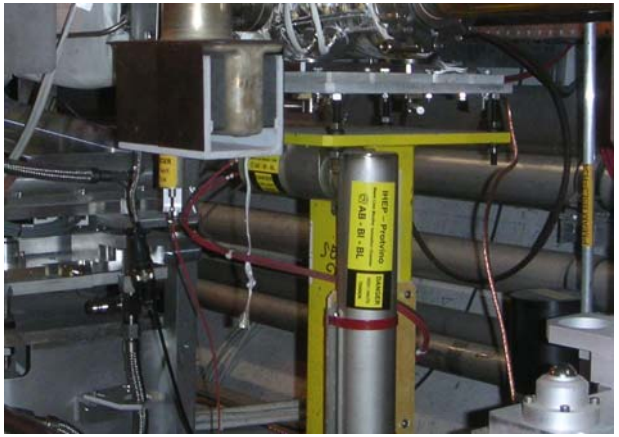
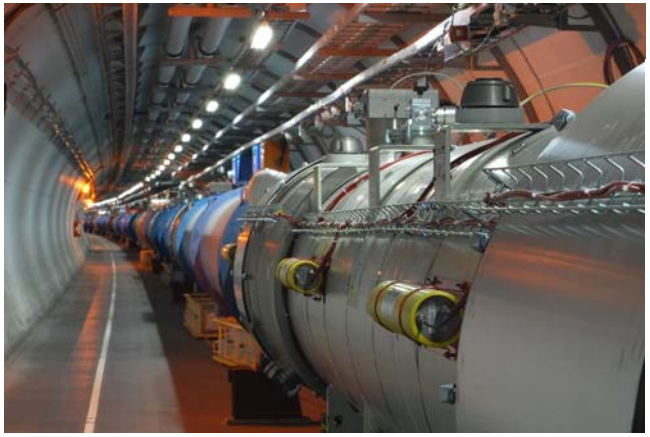
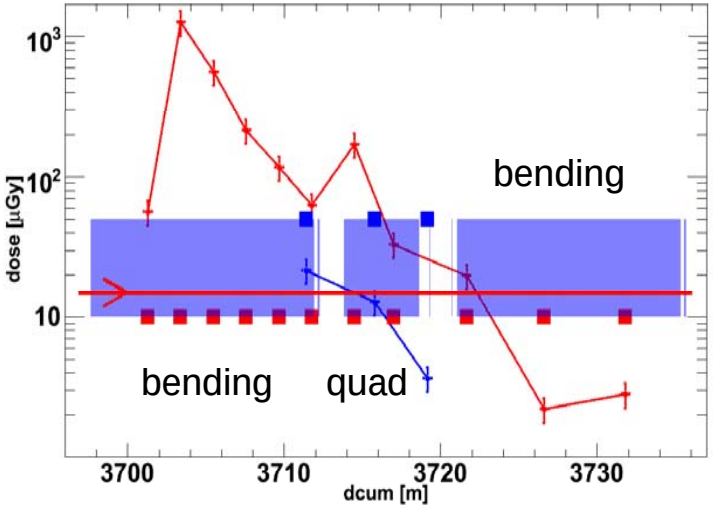
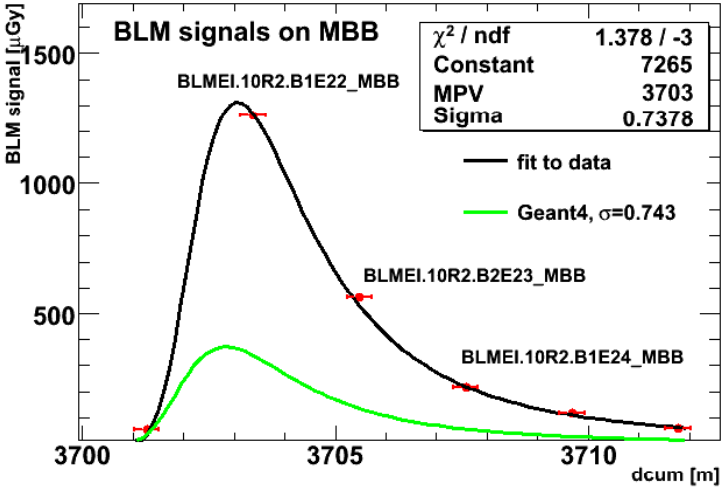
Beam Loss Monitor System Reliability and False Signals

Bernd Dehning









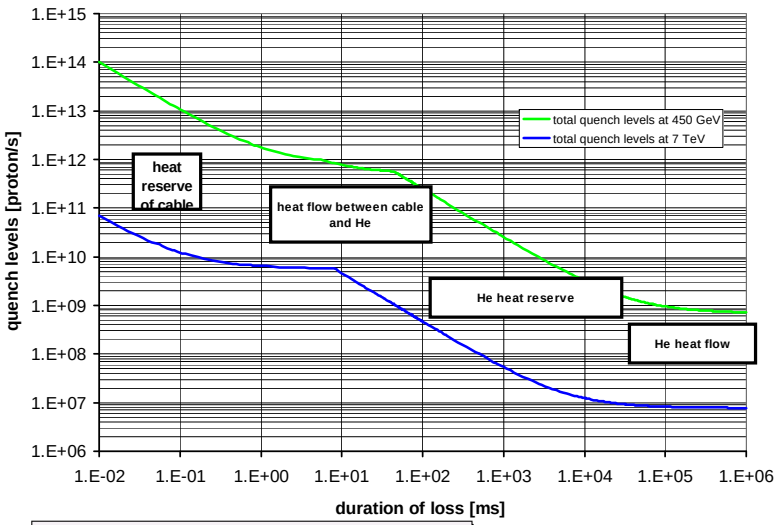
Ref: LHC beam induced quench

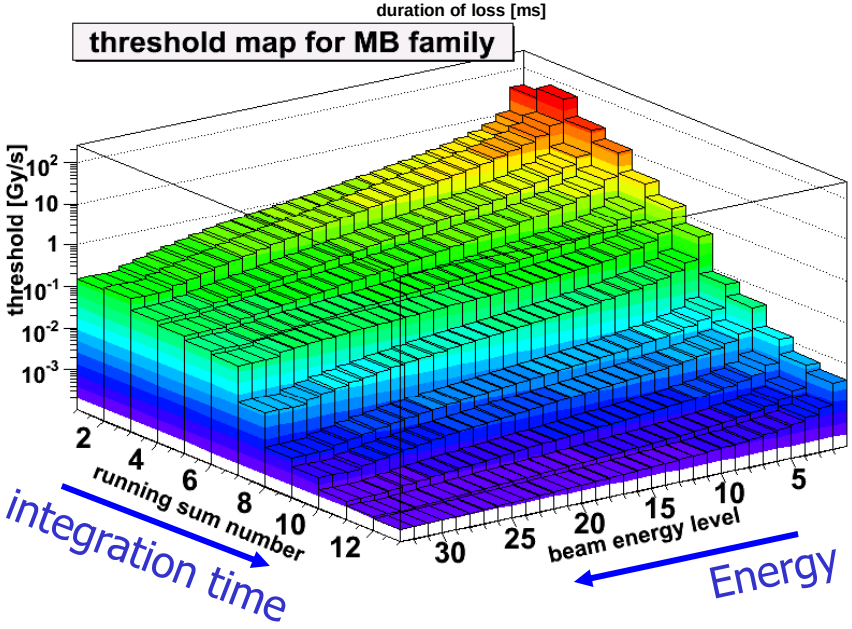
Content

- Reliability
  - Overview of system
  - Hardware
  - Software
  - Operational procedures
- False dumps
  - Some system issues
  - Failures of hardware
  - Measurements

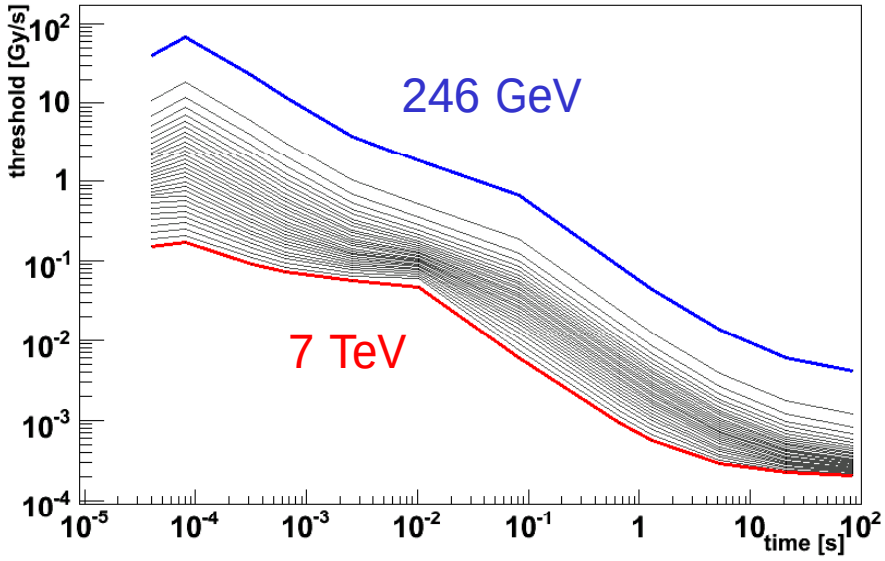
Thesis: Reliability of the Beam Loss Monitors System

Quench and Damage Levels



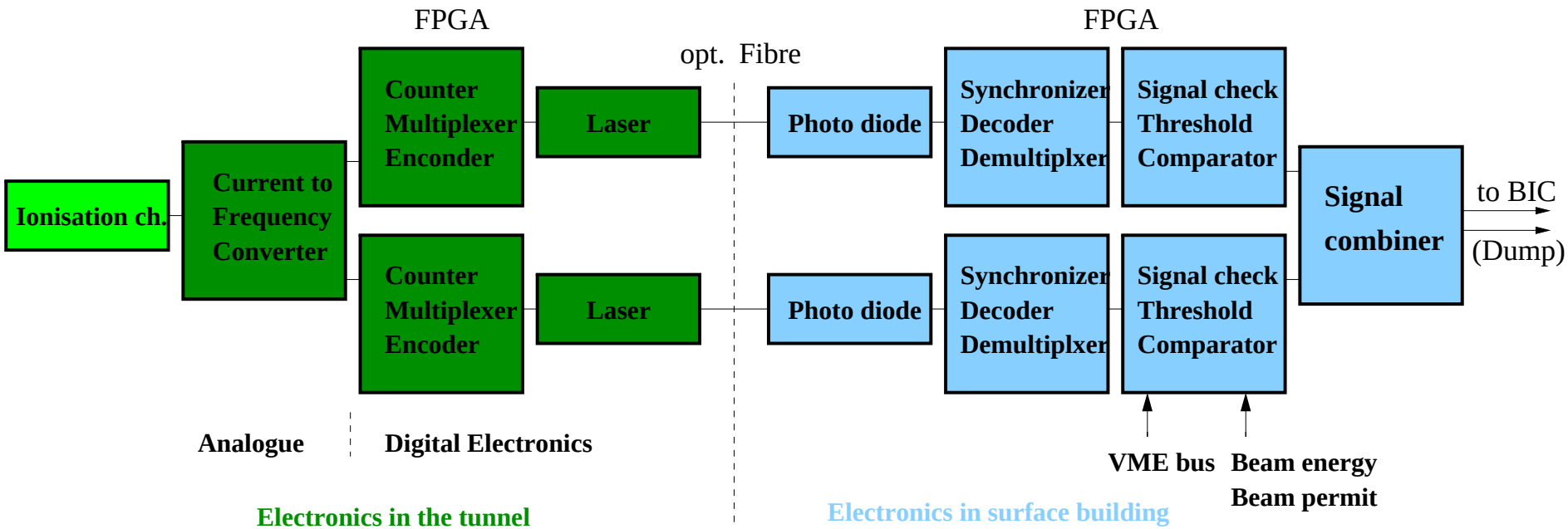


- High dynamic range dynamic
  - Arc: 10^8
  - Collimation: 10^{13} second detector
- Change of the thresholds:
  - As function of loss duration
  - As function of beam energy

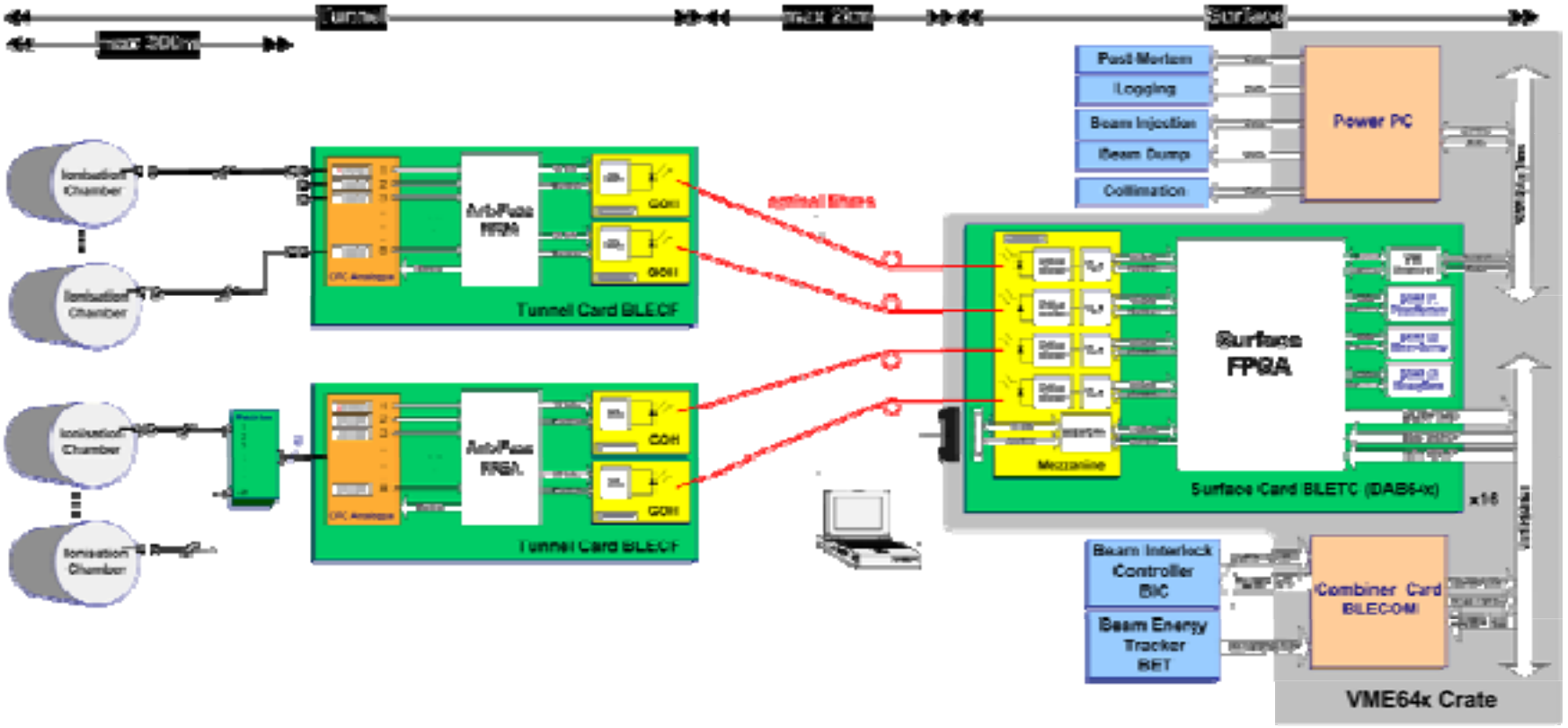


Beam Loss Measurement System Layouts

LHC



The BLM Acquisition System



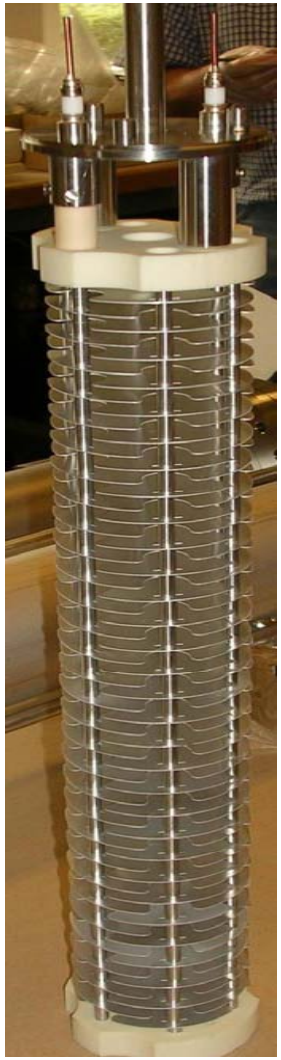
Analog front-end FEE

- **Current to Frequency Converters (CFCs)**
- **Analogue to Digital Converters (ADCs)**
- **Tunnel FPGAs:**
  Actel's 54SX/A radiation tolerant.
- **Communication links:**
  Gigabit Optical Links.
- **All radiation tested to 500 Gy and 1 10^{12} p/cm²**

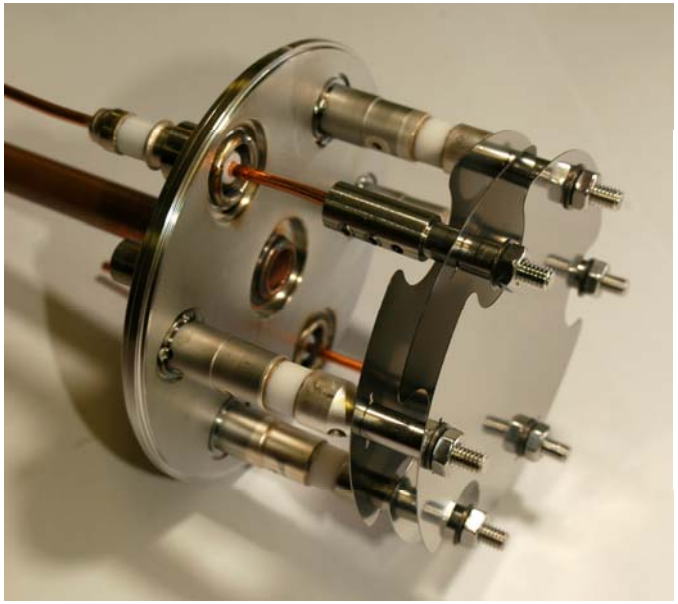
Real-Time Processing BEE

- **FPGA Altera's Stratix EP1S40 (**medium size, SRAM based**)**
- **Mezzanine card for the optical links**
- **3 x 2 MB SRAMs for temporary data storage**
- **NV-RAM for system settings and threshold table storage**

Ionisation Chamber and Secondary Emission Monitor



- Stainless steal cylinder
- Parallel electrodes distance 0.5 cm
- Diameter 8.9 cm
- Voltage 1.5 kV
- Low pass filter at the HV input



Signal Ratio: IC/SEM = 60000

IC:

- Al electrodes
- Length 60 cm
- Ion collection time 85 us
- N_2 gas filling at 1.1 bar
- Sensitive volume 1.5 l

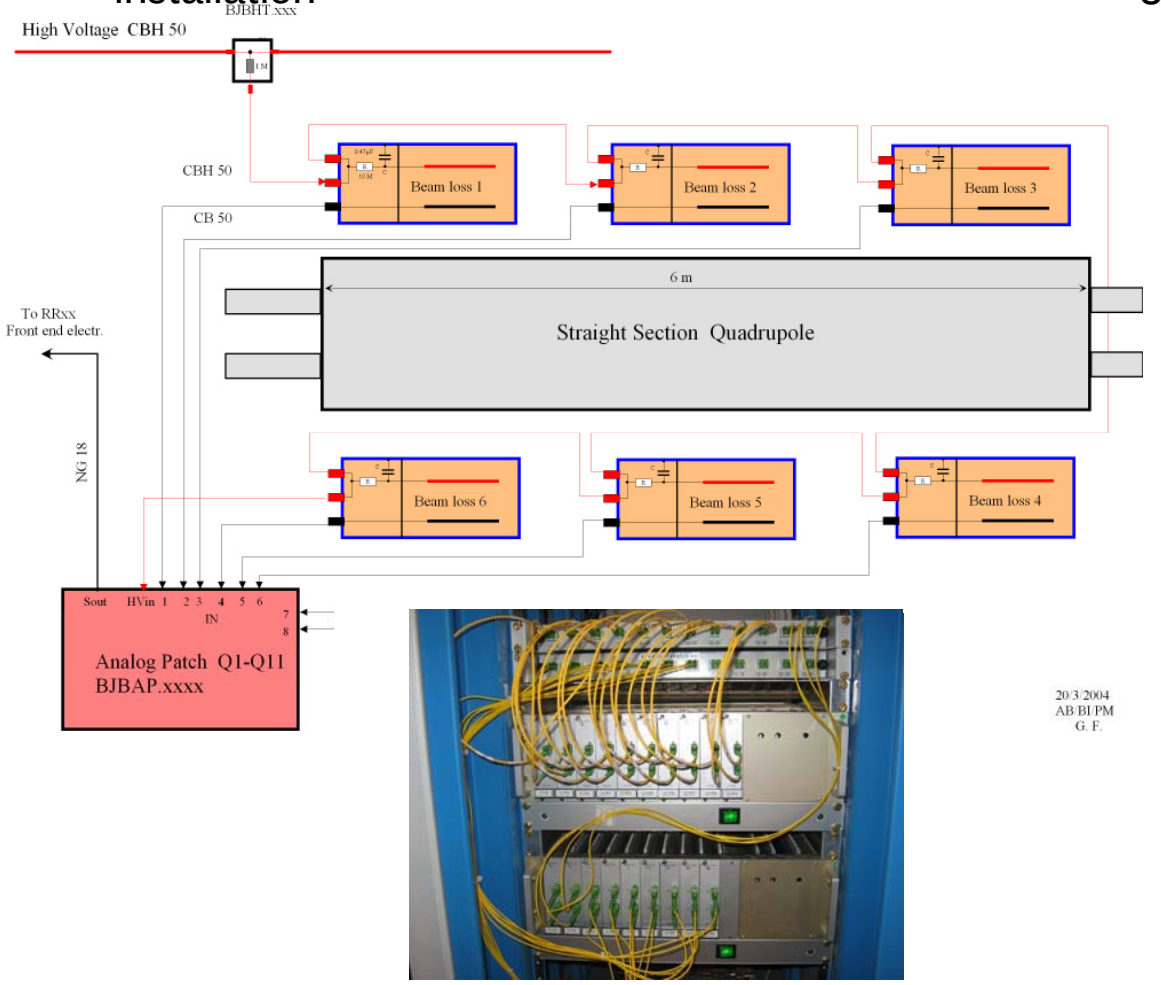
SEM:

- Ti electrodes
- Components UHV compatible
- Steel vacuum fired
- Detector contains 170 cm2 of NEG St707 to keep the vacuum < 10-4 mbar during 20 years

Robust and failure tolerant design

Tunnel hardware installation

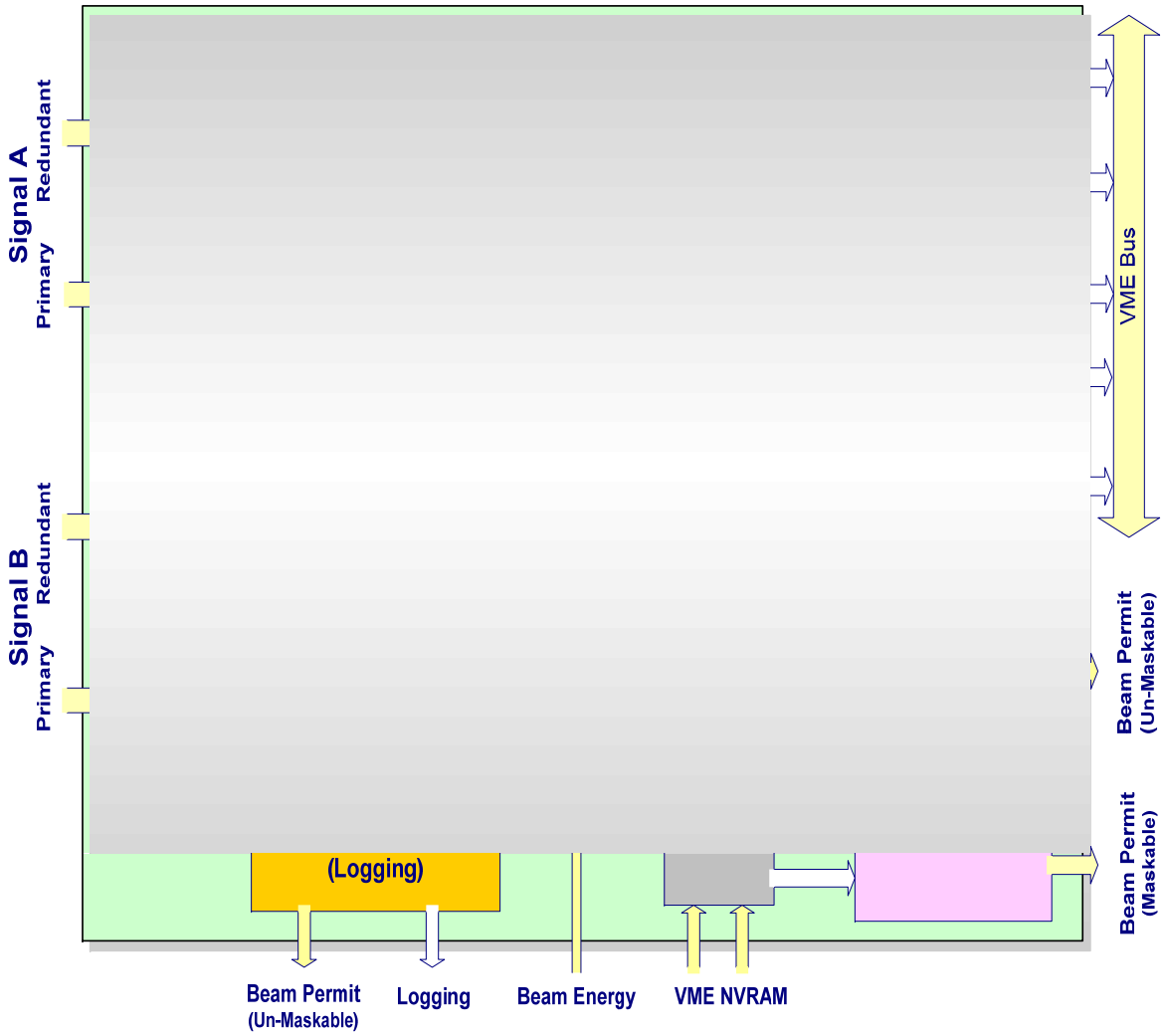
- Schemes of the straight section installation

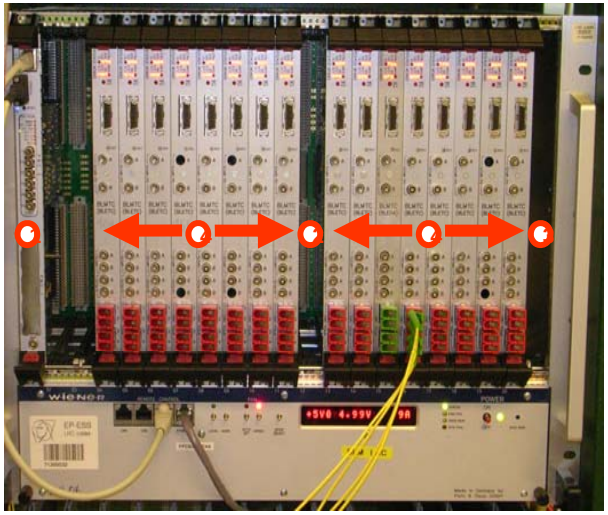


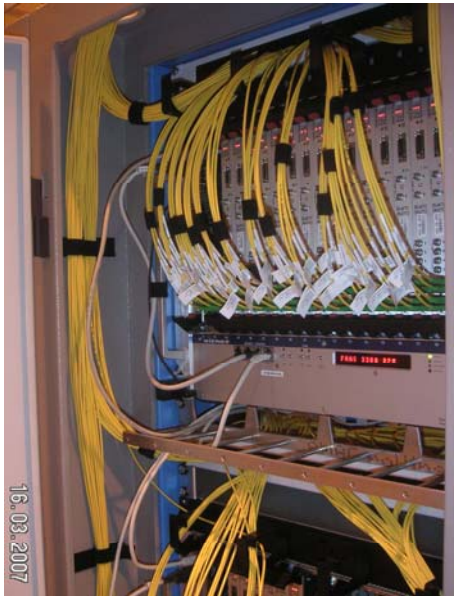
- Schemes of the ARC installation: electronics below magnets

- Ionization chambers
- Filter capacitors and resistors are installed in the IC
- Signal cable length up to 600m

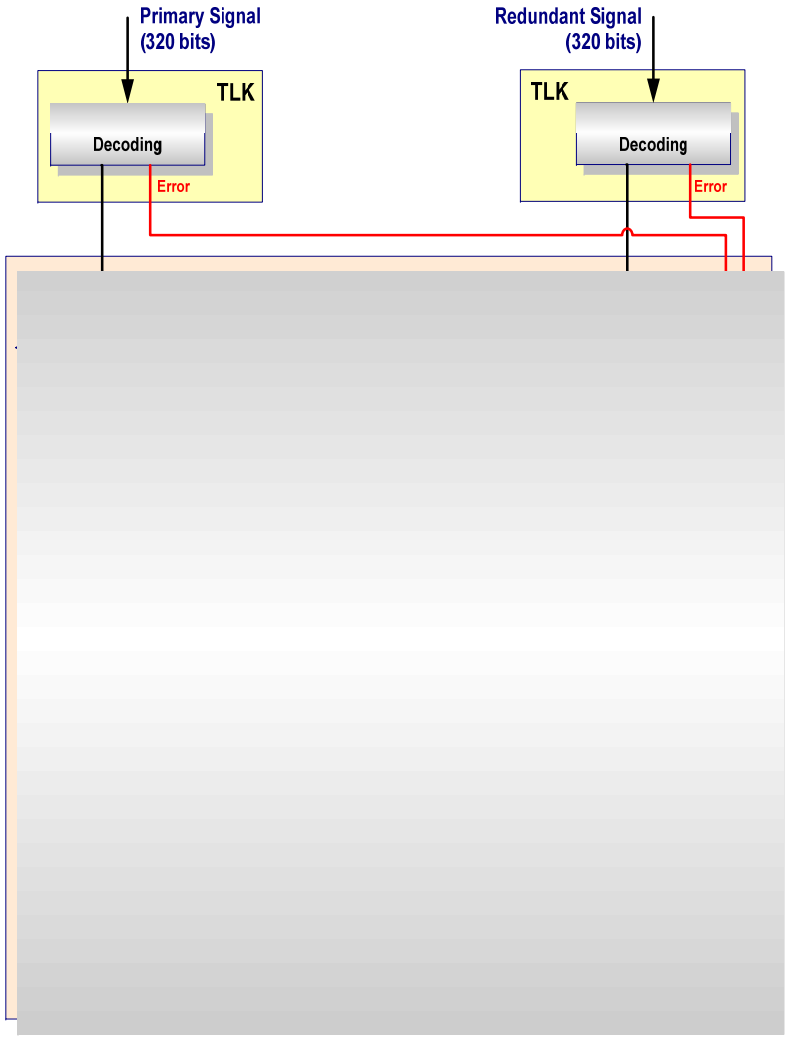
Data Processing Overview







Transmission & Tunnel Status Check

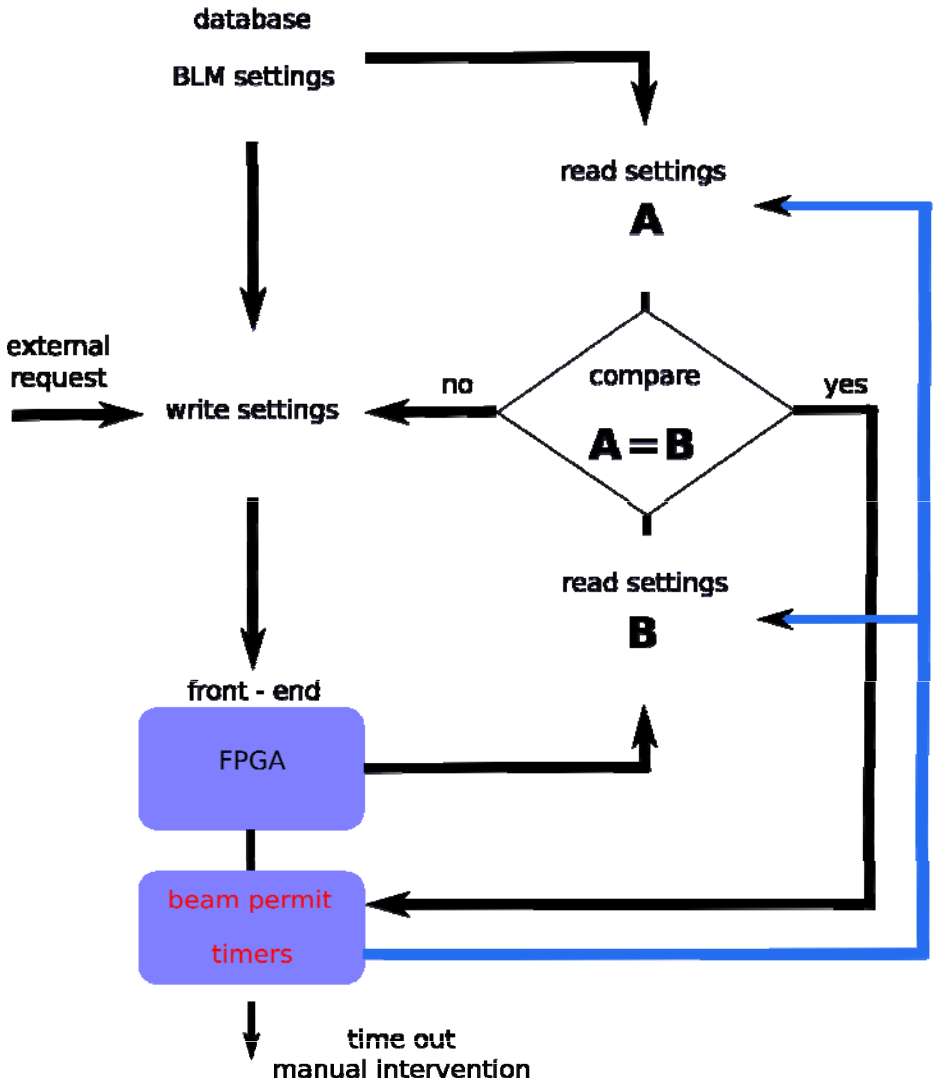


At the Surface FPGA:

- CRC-32
  - Error check / detection algorithm for each of the signals received.
- Comparison of the pair of signals.
- Signal Select block
  - Logic that chooses signal to be used
  - Identifies problematic areas.
  - Increases availability
- Tunnel's Status Check block
  - High Voltage, Power supplies
  - FPGA errors
  - Temperature

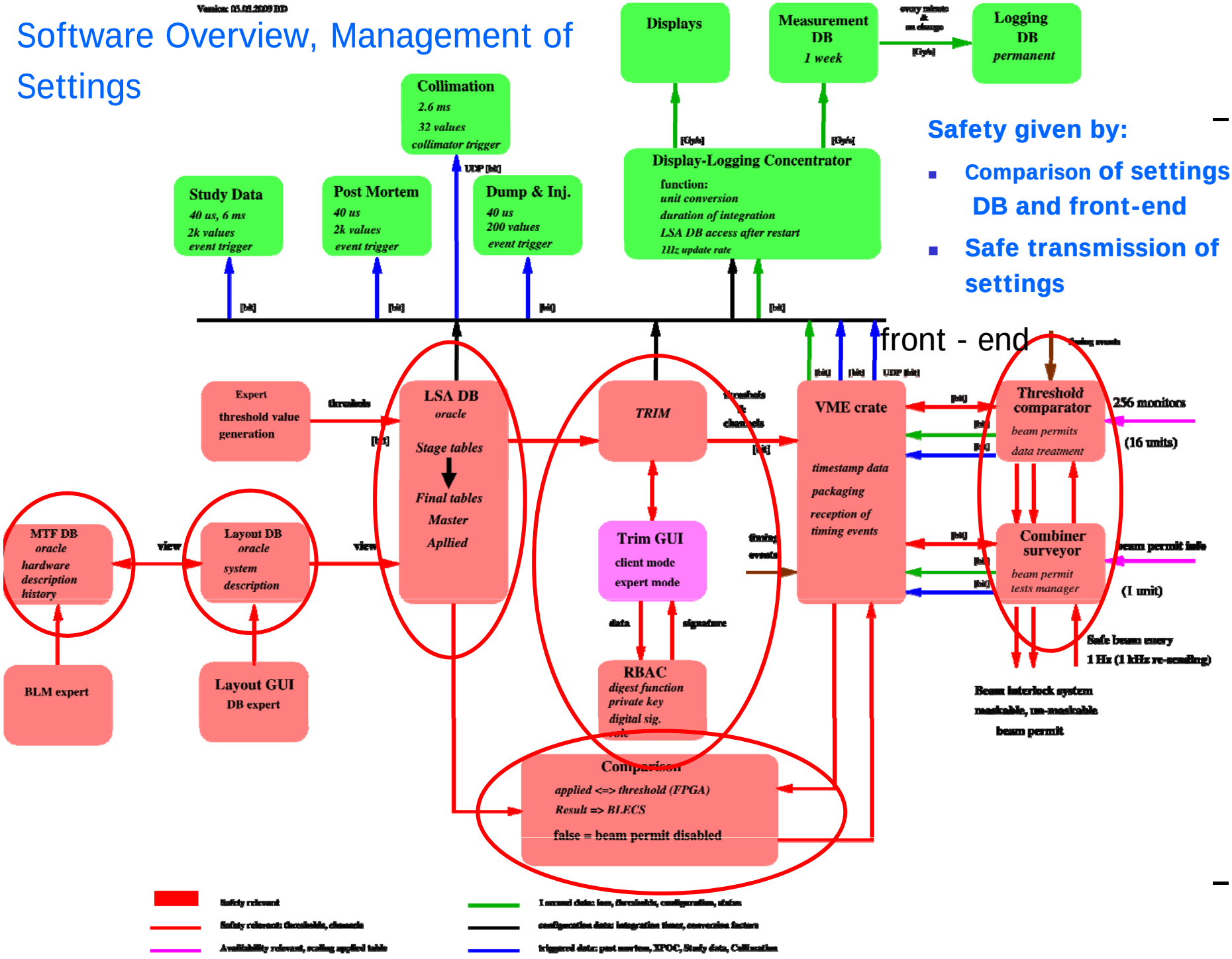
Signal Select Table				
CRC32 check		Comparison of 4Byte CRCs	Output	Remarks
A	B			
Error	Error	Error	Dump	Both signals have error
Error	Error	OK	Dump	S/W trigger (CRCgenerate or check wrong)
Error	OK	Error	Signal B	S/W trigger (error at CRC detected)
Error	OK	OK	Signal B	S/W trigger (error at data part)
OK	Error	Error	Signal A	S/W trigger (error at CRC detected)
OK	Error	OK	Signal A	S/W trigger (error at data part)
OK	OK	Error	Dump	S/W trigger (one of the counters has error)
OK	OK	OK	Signal A	By default (both signals are correct)

Settings and Checks from Database to Frontend



- Setting storage in Oracle database (LSA)
- Settings:
  - Threshold values
  - Voltages, currents, phase limits for automatic test
  - Serial numbers for ever equipment in the acquisition chain
  - Software version numbers
- Comparison of frontend settings with database every 12 hours or after every update
  - If positive hardware base beam permit given
  - If negative after retry, manual intervention (no beam permit)

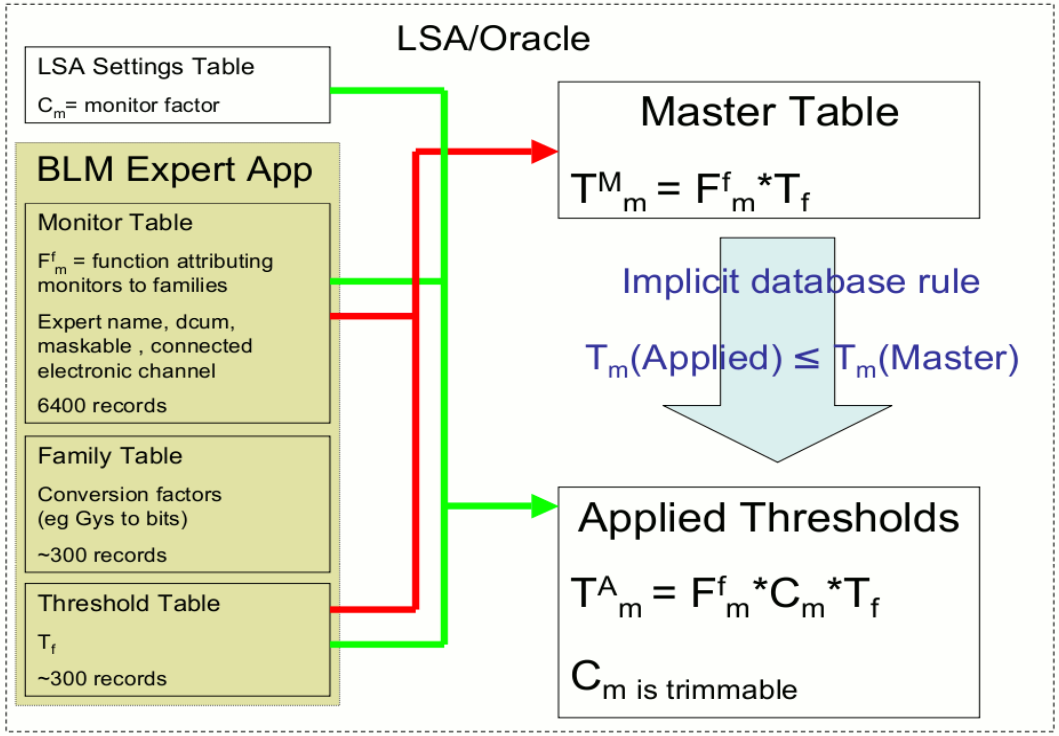
Software Overview, Management of Settings



Safety given by:

- Comparison of settings at DB and front-end
- Safe transmission of settings

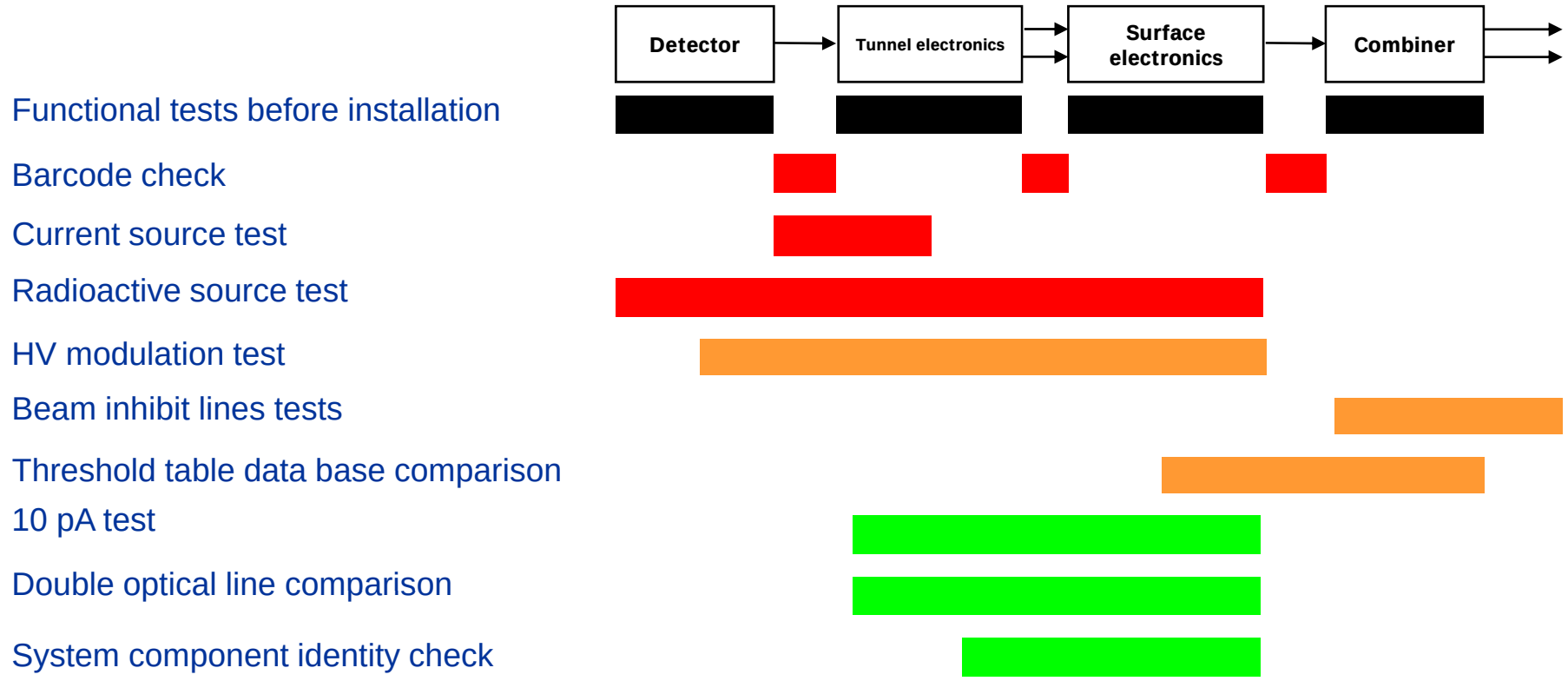
Data Base Structure



- Two layers
  - entry layer (stage tables)
  - validated layer (final tables)
- Concept of Master and Applied table
- Comparison of Threshold values
  (Applied < Master)
  - Master: less frequent changes
  - Applied: change of thresholds possible with user interface

Functional Tests Overview

PhD thesis G. Guaglio



Inspection frequency:

Reception

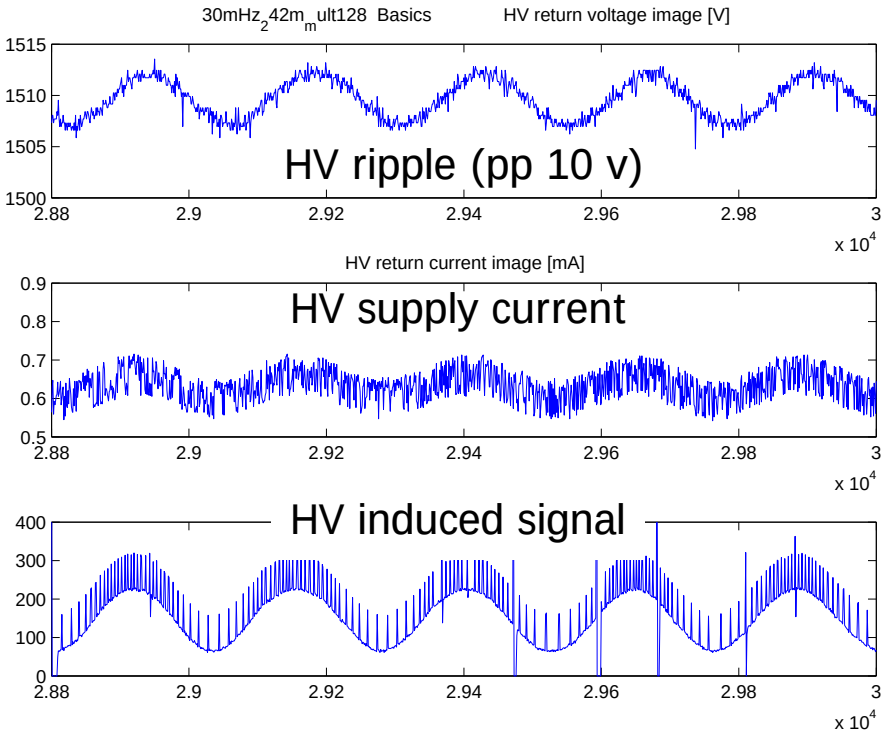
Installation and yearly maintenance

Before (each) fill

Parallel with beam

Test Procedure of Analog Signal Chain

Modulation Example



Basic concept:

Automatic test measurements in between of two fills

- Modulation of high voltage supply of chambers
  - Check of cabling
  - Check of components, R- C filter
  - Check of chamber capacity
  - Check of stability of signal, pA to nA (quench level region)
- Measurement of dark current
- Not checked: gas gain of chamber (only once a year with source)

Functional checks – Monitoring of drifts

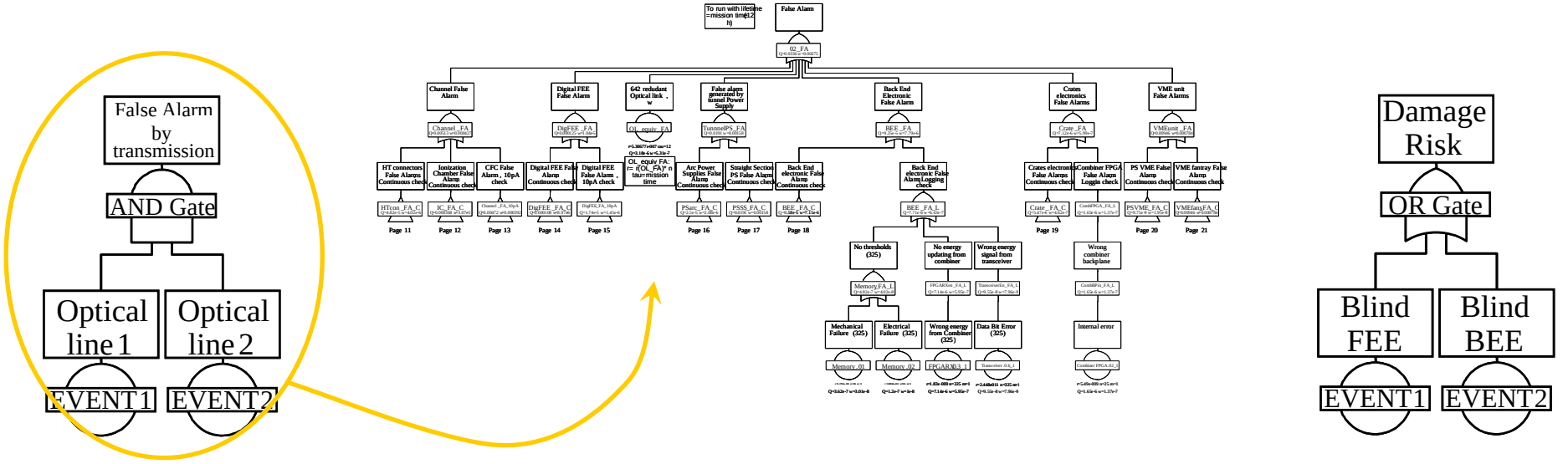
Fault Tree Analysis

- Almost 160 Failure Modes have been defined for the BLMS using the FMD-97 standard.

Three Ends Effects:

1. Damage Risk: probability not to be ready in case of dangerous loss.
2. False Alarm: probability to generate a false alarm.
3. Warning: probability to generate a maintenance request following a failure of a redundant component.

- The probability to have an Failure Mode A, Pr{A}, is calculated per each Failure Modes of the FMECA, given the hazard rate, the repair rate and the inspection period .



Fault Trees Results

- The probabilities to fail (unavailability) for the BLMS have been calculated.
- Per each End Effects, the major contributors to such probabilities have been pointed out too.

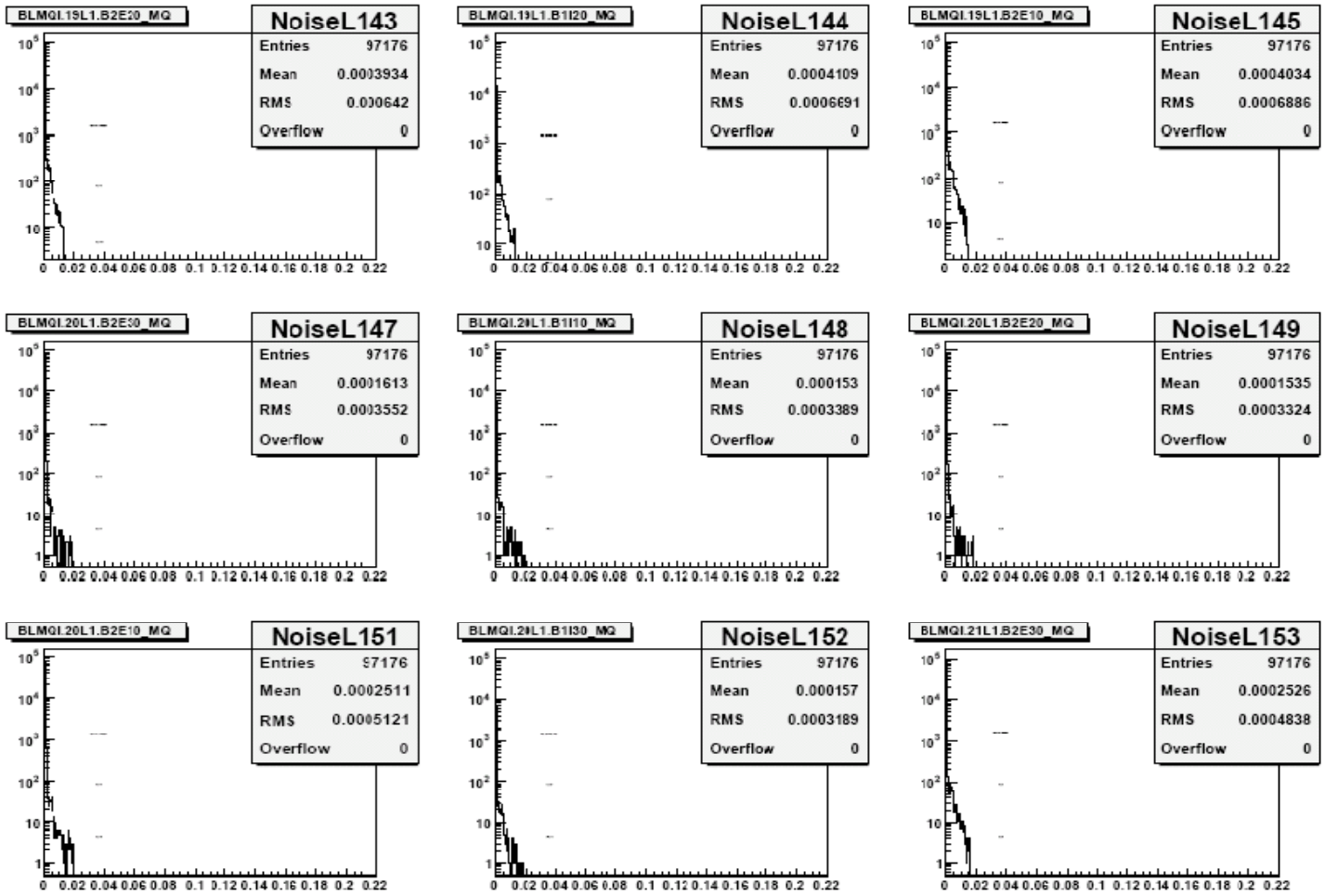
	Consequences per year	Weakest components	Notes
Damage Risk	$5 \cdot 10^{-4}$ (100 dangerous losses)	Detector (88%) Analogue electronics (11%)	Detector likely overestimated (60% CL of no failure after $1.5\ 10^{6}$ h).
False Alarm	13 ± 4	Tunnel power supplies (57%) VME fans (28%)	Tunnel power supplies likely underestimated (see sensitivity example).
Warning	35 ± 6	Optical line (98%) VME PS (1%)	LASER hazard rate likely overestimated by MIL.

Hardware Failures

- 1 VME fan-tray; hardware, microcontroller to be identified
- 1 VME (BLETC) card; printed circuit board failure. 1 year of operation. The card was in the crate that the fan-tray failed
- 1 VME crate power supply. Voltage outside the range (other PS showed same problem).
- 1 VME crate CPU, hardware failure caused by continuously rebooting due to 'persistent data' caused by the timing process (called LTIM).

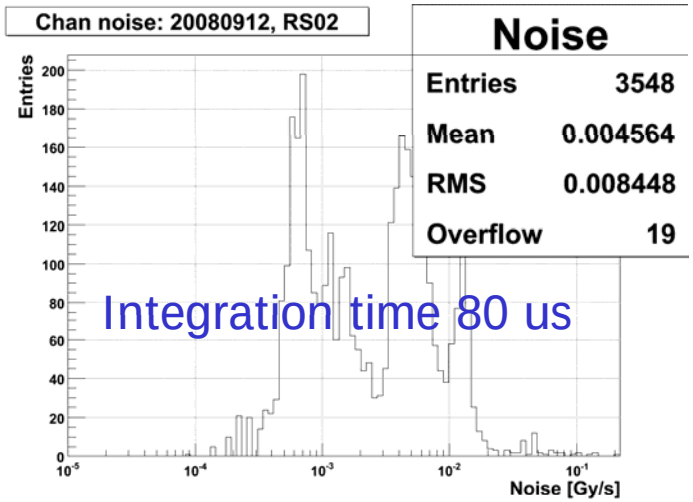
VME crate failure are under investigation

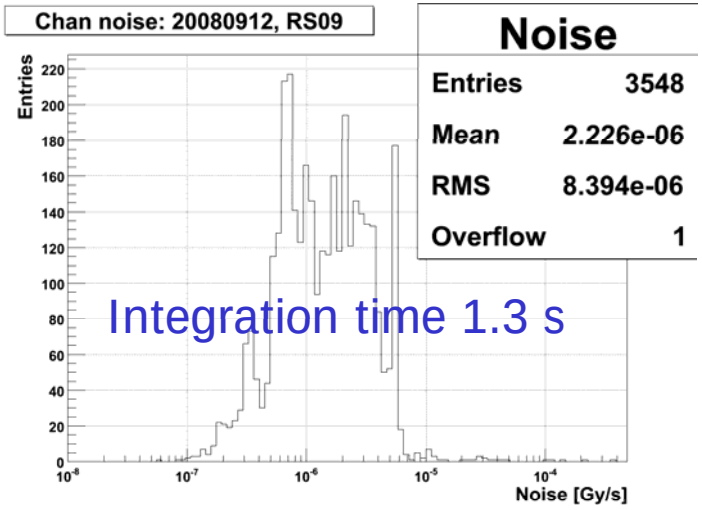
Noise Level Distributions

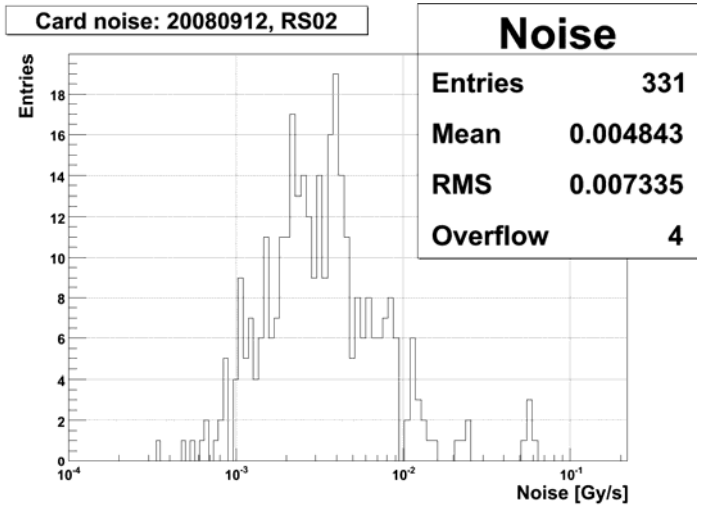


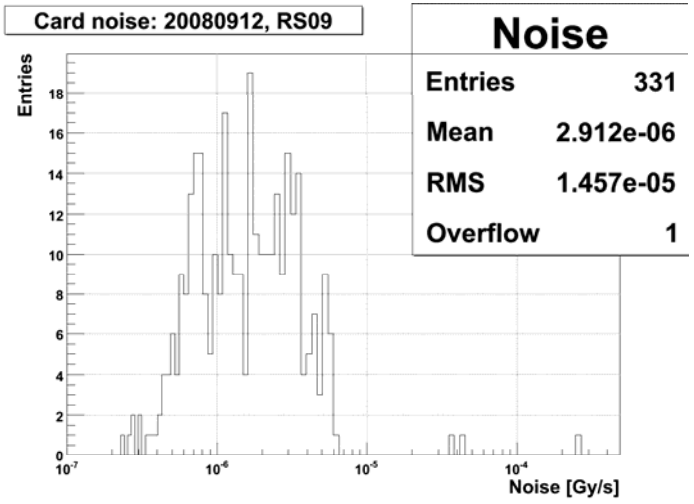
- Procedure:
  - require data during nominal operation conditions of LHC
  - Choose most sensitive integration intervals
  - Set histogram max value to lowest quench threshold level (MB-magnet)
- Overflows are interpreted as false signals

Noise Signal Distribution of LHC 12. September 2008









- Checked:

  15 hours in the nights between 12 to 16 September 2008
- Results:

  19 channels would have given false signals located on 4 electronics cards
- Conclusion:

  It is assumed that this channels could have been repaired
- 2009 checks are foreseen after reinstallation of BLM system

Conclusion

- System constructed aiming for a damage risk of SIL 3 (1 10^{-8} to 1 10^{-7} 1/h, 5 10^{-5} to 5 10^{-4} 1/year)
  - Audit endorsed system design
  - Audit follow up planed for June 2009 (combined with audit follow up for interlock system and dump)
- Full implementation of foreseen system test procedures to keep SIL level during operation
- False signal generation limited to few channels (<0.5 %), which are assumed to be repairable

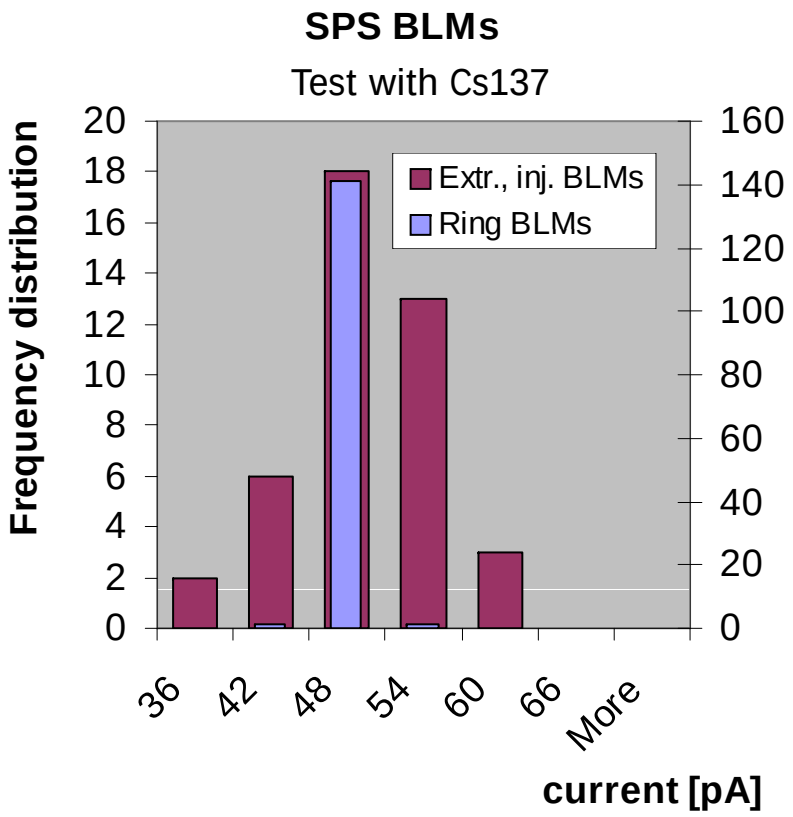
Literature

- General Information: http://cern.ch/blm
- Audit
- Talks and papers:
  - Reliability issues, thesis, G. Guaglio
  - Reliability issues, R. Filippini et al., PAC 05
  - Front end electronics, analog, thesis, W. Friesenbichler
  - Front end electronics, analog-digital, E. Effinger et al.
  - Ionisataion chamber, thesis, M. Stocker
  - Secondary emission monitor, thesis, D. Kramer
  - Digital signal treatment, thesis, C. Zamantzas
  - Balancing Safety and Availability for an Electronic Protection System, S. Wagner et al., to be published, ESREL 2008

Threshold & database functional tests

- version 2 threshold table
  - change the master threshold for one, given family:
    - generation of new master
    - sending new master to LSA (hopefully with new application by Javier)
    - we end up with a new version of master (call it 2.01)
  - split existing family into two families with different masters
    - create new family in LSA
    - create new master thresholds for the new family
    - move chosen monitors to new family
    - we end up with a new version of master: 2.02 3.
  - exchange a card (really):
    - stop a crate, change physically exchange one card
    - reconnect channels - change of channel structure
    - introduce changes to MTF (Slava)
    - propagate changes to Layout
    - update LSA from Layout
    - master version 2.03 4.
  - roll-back all the changes in LSA to version 2.00. (eventually changing back the card)
    - measure the time it takes us to perform all the operations

Gain Variation of SPS Chambers



Total received dose:

ring 0.1 to 1 kGy/year

extr 0.1 to 10 MGy/year

- 30 years of operation
- Measurements done with installed electronic
- Relative accuracy
  - $\Delta\sigma/\sigma$ < 0.01 (for ring BLMs)
  - $\Delta\sigma/\sigma$ < 0.05 (for Extr., inj. BLMs)
- Gain variation only observed in high radiation areas
- Consequences for LHC:
  - No gain variation expected in the straight section and ARC of LHC
  - Variation of gain in collimation possible for ionisation chambers

Reliable component

System Failures

To avoid loss of data

- Frame ID
  - Surface FPGA checks for missing frames
  - Incrementing number included at every transmission
- Optical link is always active
  - 8b/10b encoding sends “commas” when no data
  - Disconnection is detected in max 25ns

To ensure recognition of system failures
and beam dump requests

- FPGA Outputs (Beam Dump signals) as frequency
  - At a dump request, reset, or failure the transmitted frequency will be altered
- Beam Permit lines are daisy-chained between cards
  - Custom VME backplane
  - Dummy cards on empty slots to close circuit