Monitoring Vibrations with an FPGA

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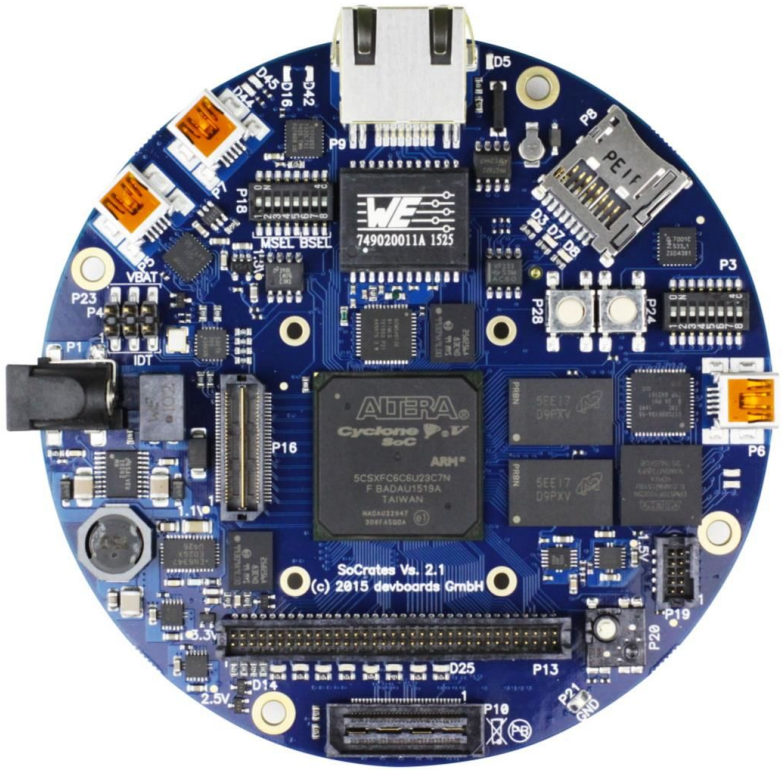
LHCb



Develop a vibration monitoring system for the hard-disks using vibration sensors, ADCs and a SoC FPGA

Progress

- Communicate with ADC chip via Verilog SPI
  - Visual indications with LEDs
- Interface between ARM processor and FPGA fabric
- Communicate with accelerometer using Verilog I^2C

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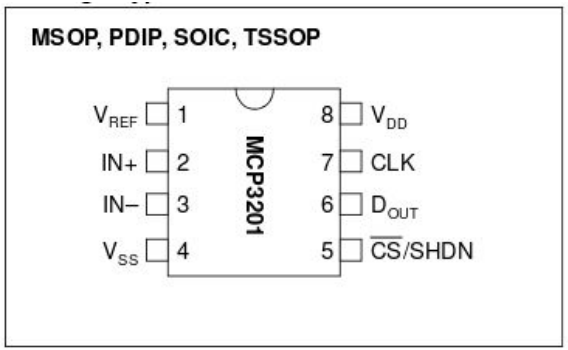
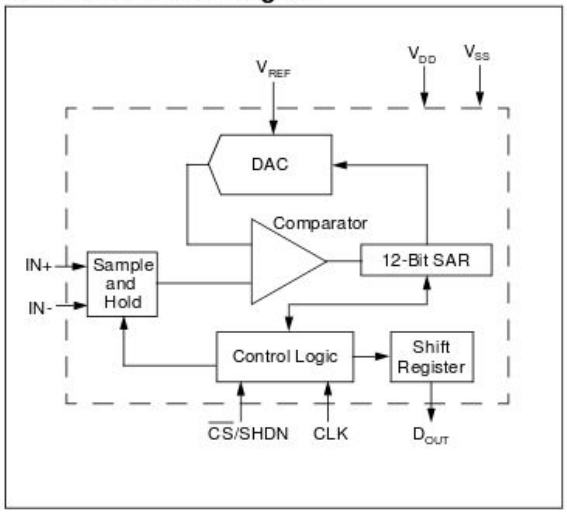


Functional Block Diagram



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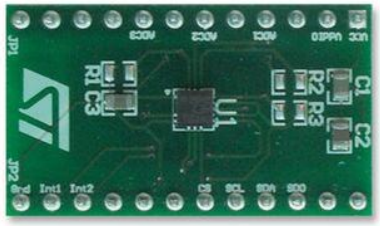
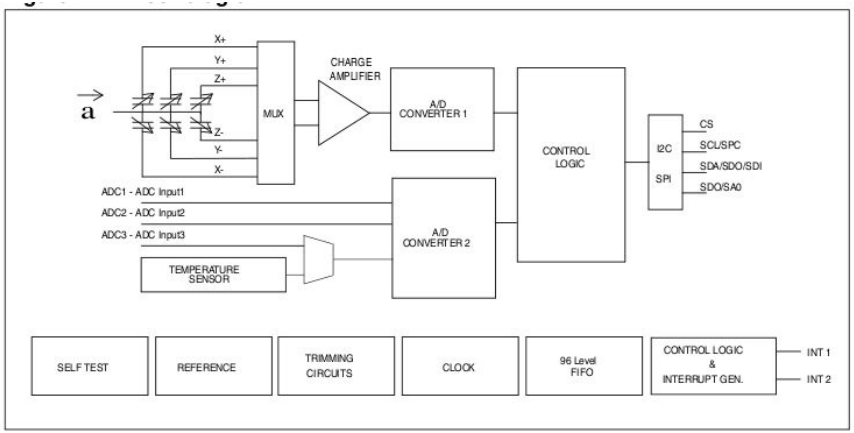
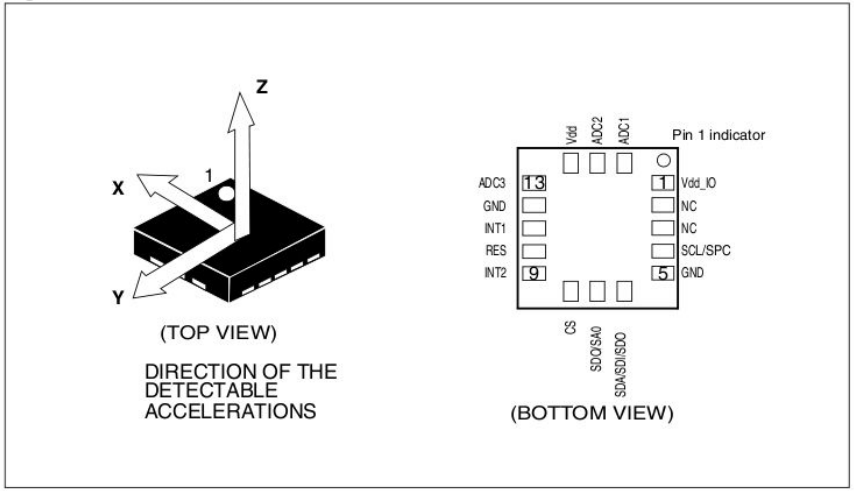
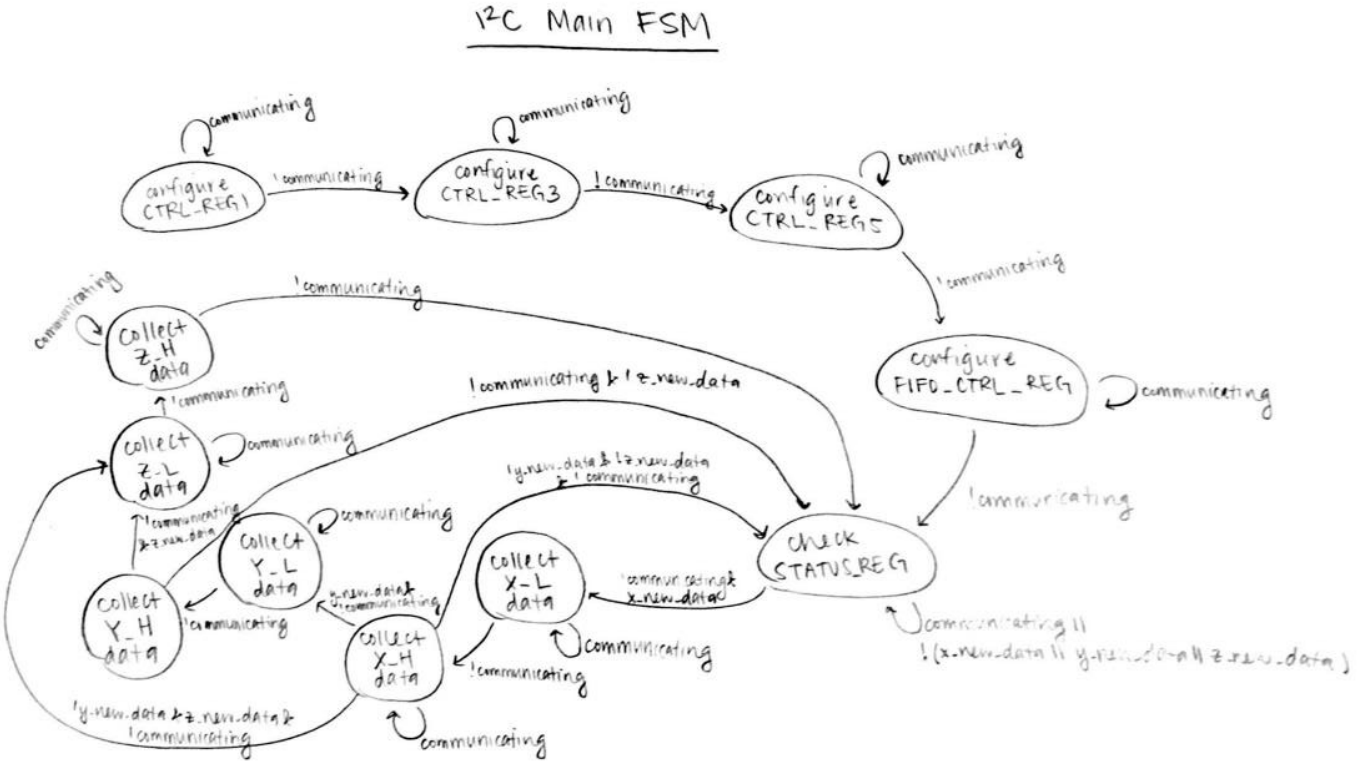
- Implementing a sequential communication interface using parallel logic
- Time communications at the right clock cycles
- Testing modules (ModelSim & SignalTap)







FSM Diagrams - Main



I^2C - Inter-integrated Circuit Protocol

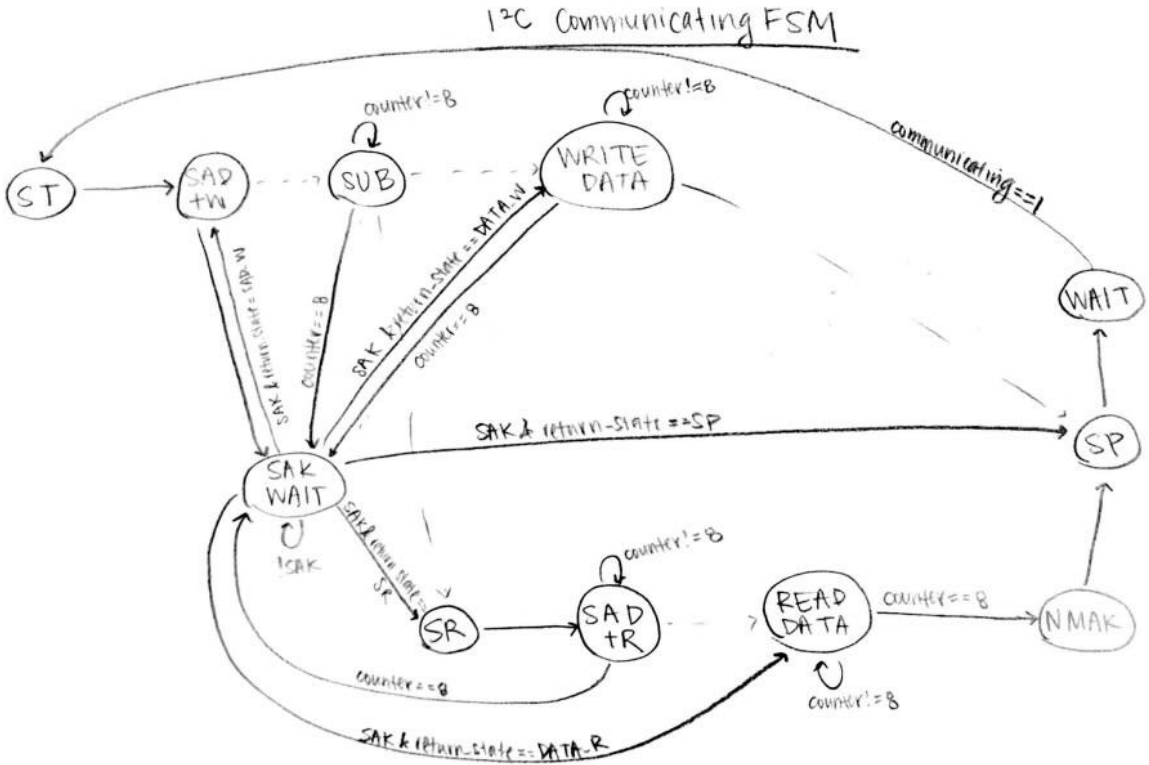
Table 15. Transfer when master is receiving (reading) one byte of data from slave:

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 13. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

FSM Diagrams - Communication



Questions?