Monitoring Vibrations with an FPGA

Sharon Tseng
Supervisor: Christian Faerber

UM CERN REU
10 August 2016

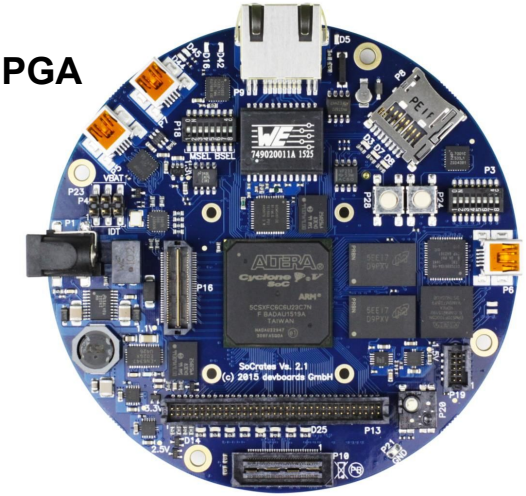
LHCb

Event Filter Farm hard disks

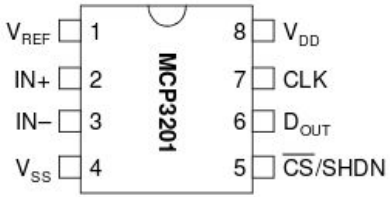
Develop a vibration monitoring system for the hard-disks using vibration sensors, ADCs and a SoC FPGA

Components

FPGA

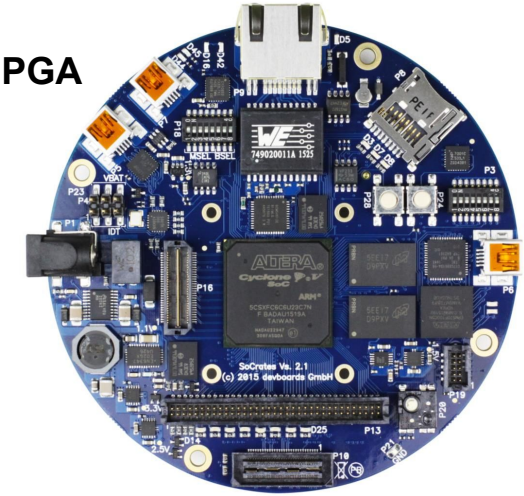


Components

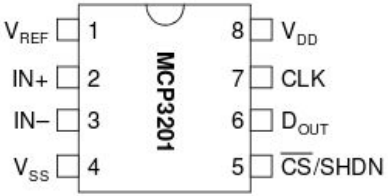


ADC chip

FPGA

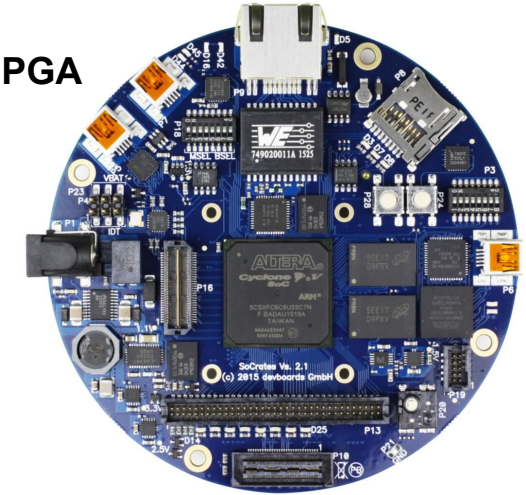


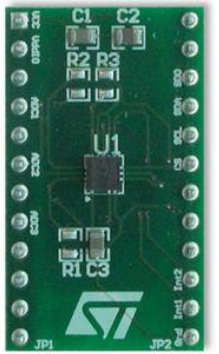
Components



ADC chip

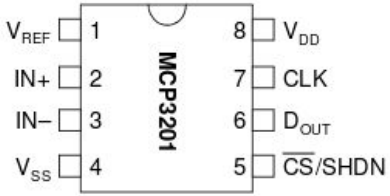
FPGA





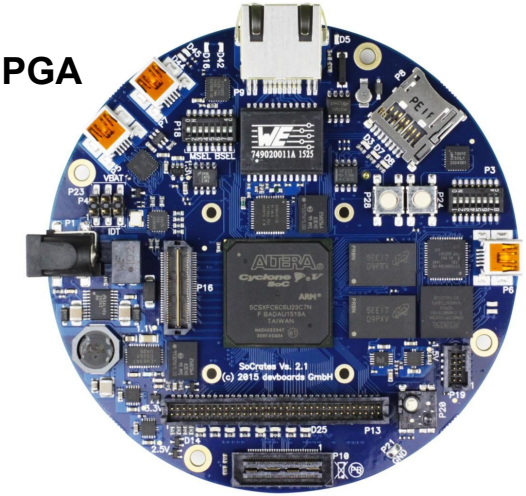
Accelerometer

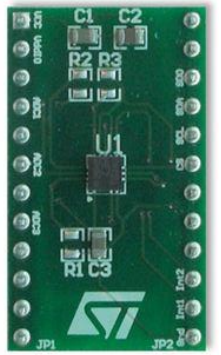
Components



ADC chip

FPGA





Accelerometer

ALTERA

QUARTUS® II

Qsys

eclipse

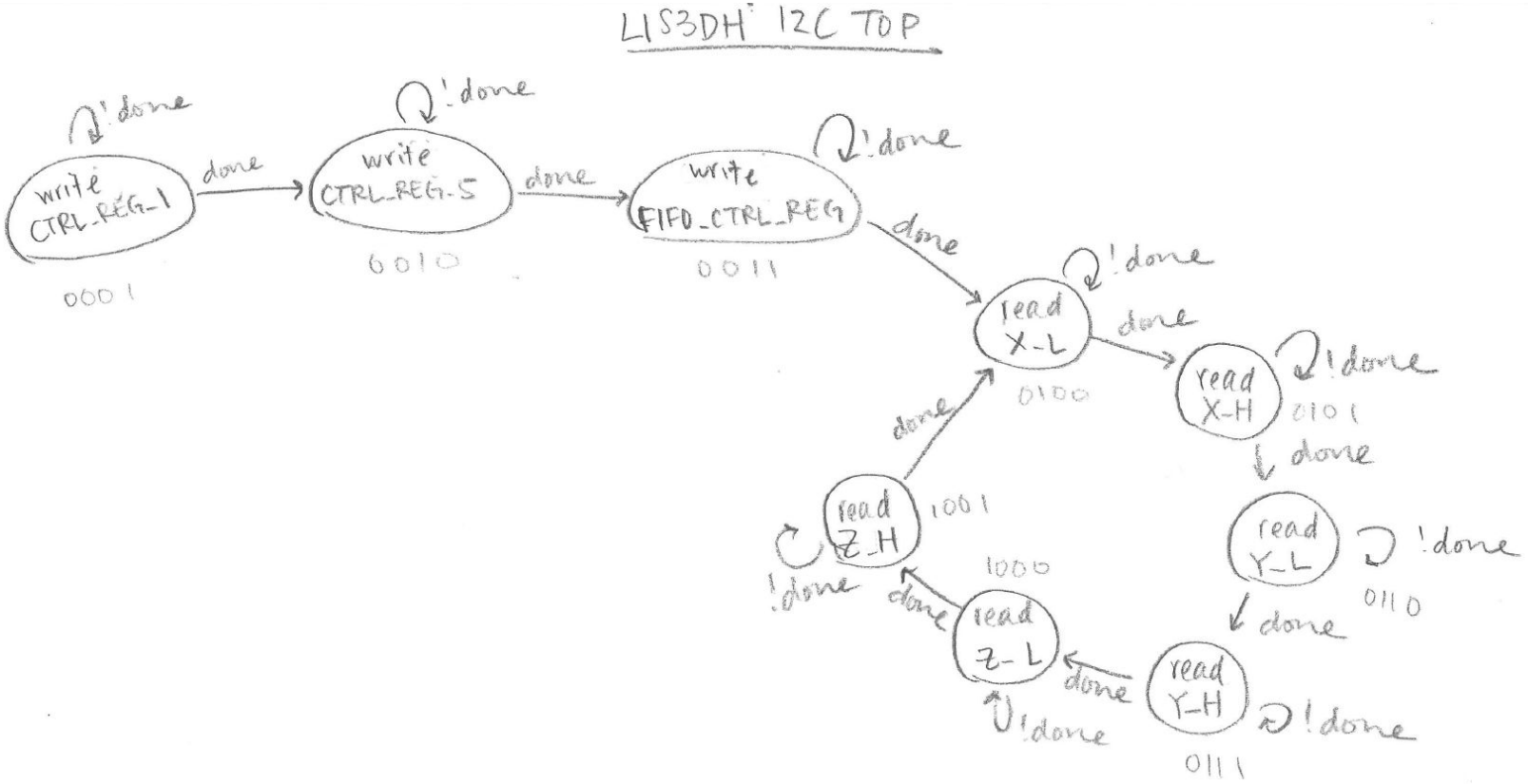
Software

Communication Protocols

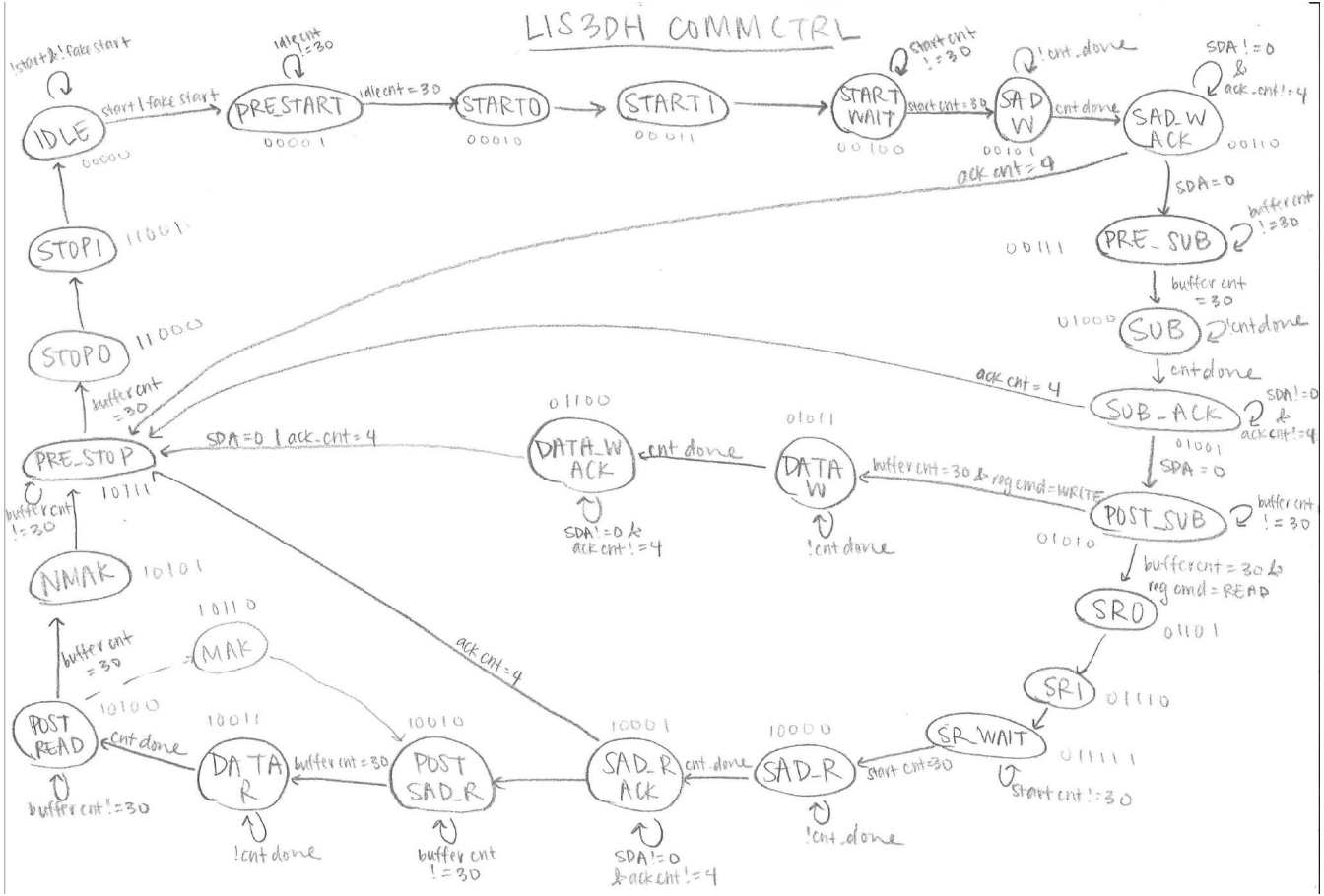
- Designing protocols for a microcontroller to communicate with other integrated circuits
  - SPI - Serial Peripheral Interface
  - I^2C - Inter-integrated Circuits Protocol

- Implemented primarily with finite state machines in Verilog

I²C Finite State Machines - Top Level

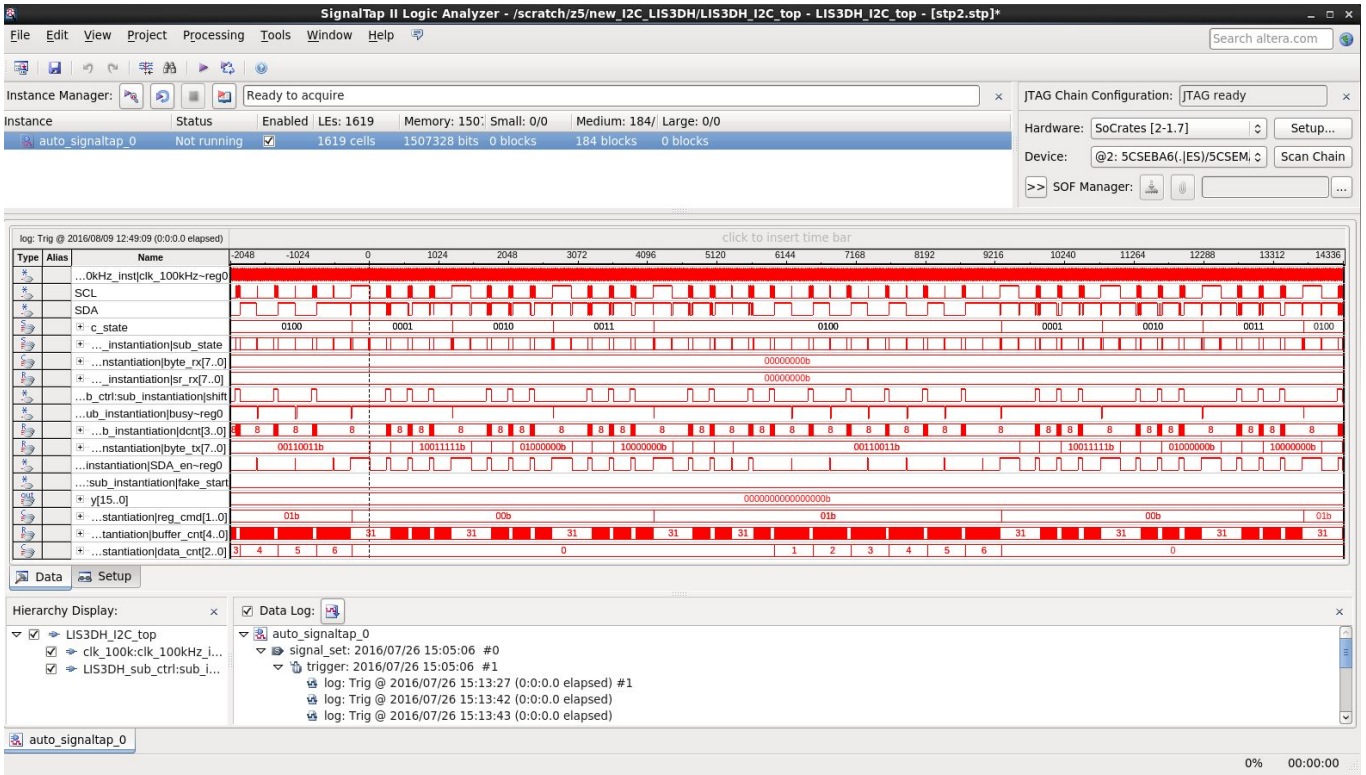


I²C FSM - Bit Level Communications



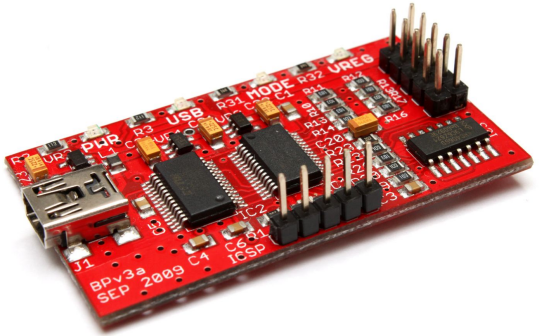
SignalTap Logic Analyzer

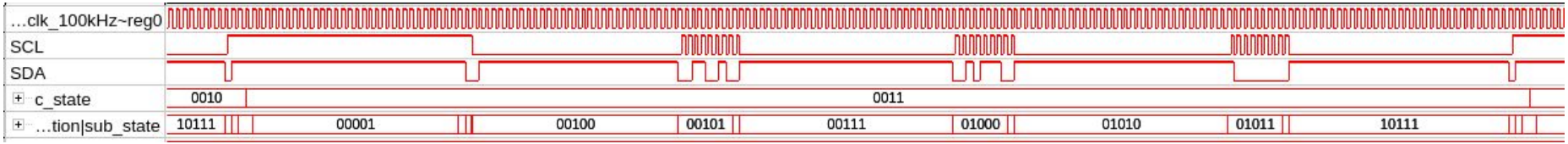
Debugging FPGA design is a different challenge because everything operates in real time and all signals are hardware.



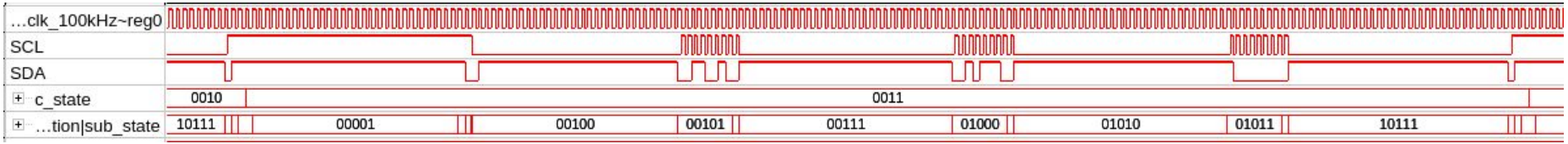
Troubleshooting

- Testing and implementing in increments
- Bus Pirate - open source hacker multi-tool to confirm protocol
- Biggest errors:
  - Timing: transmit and receive bits one clock cycle after command
  - Longer hold times between issuing commands

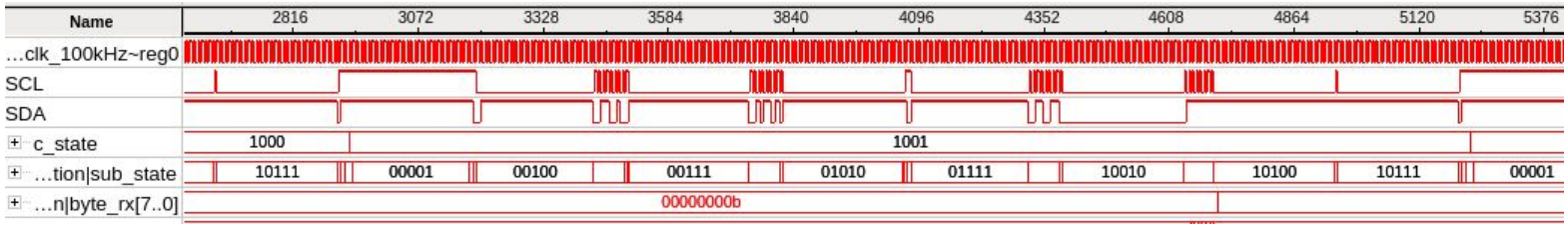




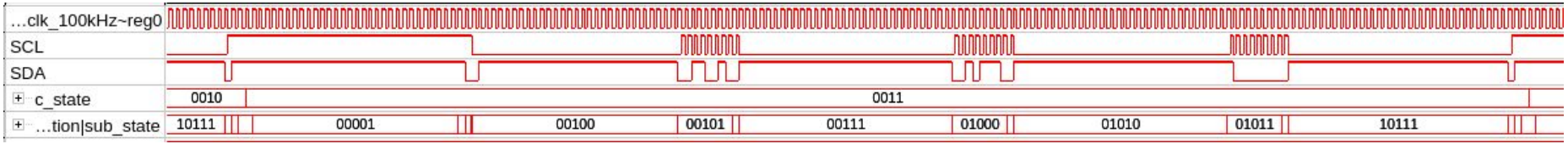
Configure FIFO_CTRL_REG (0010110b) to 10000000b



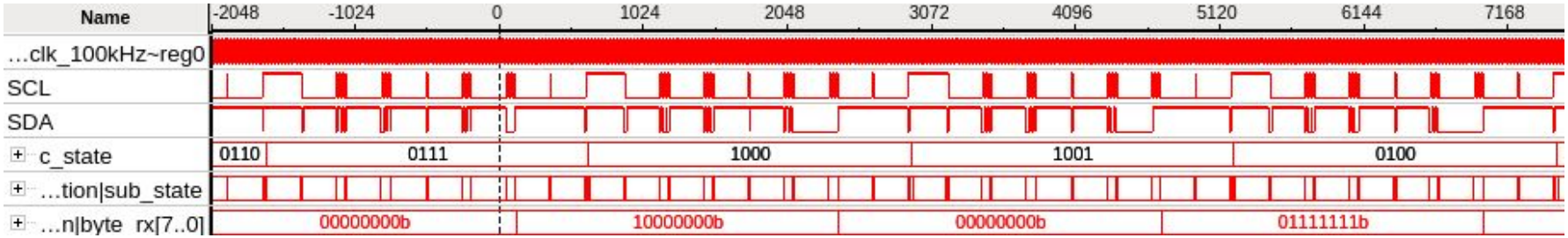
Configure FIFO_CTRL_REG (0010110b) to 10000000b

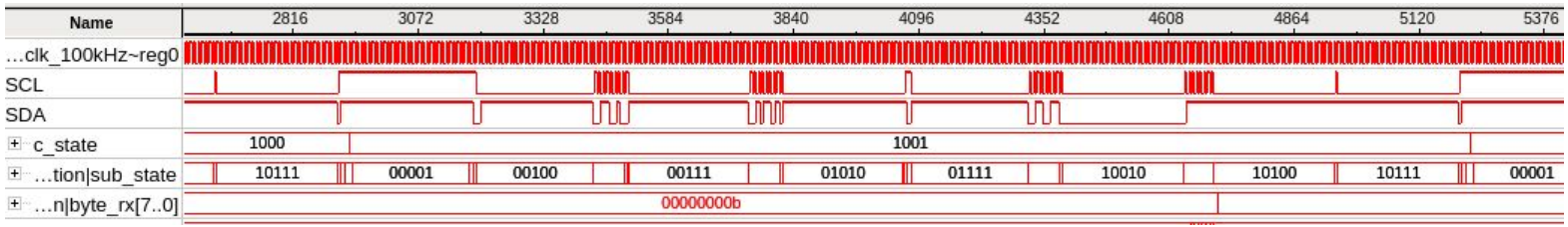


Reading output registers



Configure FIFO_CTRL_REG (0010110b) to 10000000b





Reading output registers

Next Steps

- Apply Fourier transforms to data
- Seperately analyze frequency, timing and amplitude of vibrations
- Install in the EFF and compare with data failing rate

Thank You’s

- Christian Faerber
- EP-LBC group & LHCb
- Steve Goldfarb & Jennifer Roloff
- Emanuel Gull, Junjie Zhu & Elise Bodei
- National Science Foundation & University of Michigan

Thank you for your time!

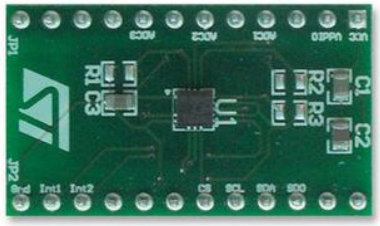
Questions?

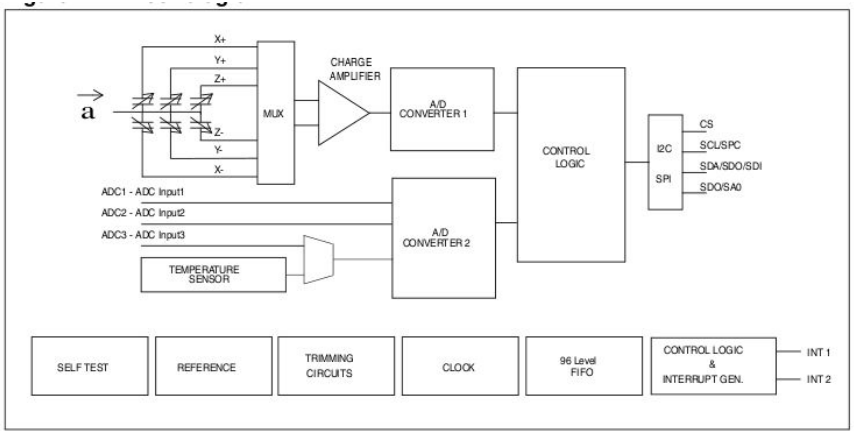
Timing

- Operate on a 100kHz clock
- Response time of 10µs
- Start-up configuration time of 7.5ms
- Read each register every 610µs

LIS3DH Accelerometer

- 3-axes linear accelerometer
- I^2C & SPI digital output interface
- 96 level FIFO register with 16 bit data output





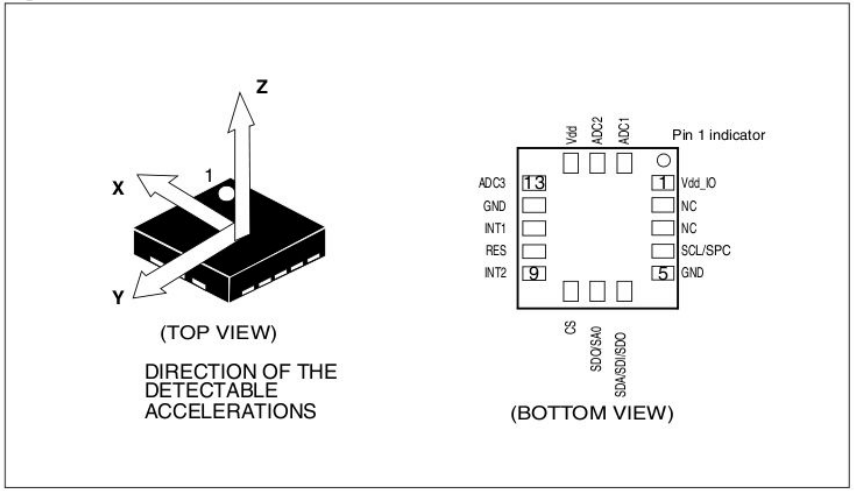


Photo Citations

https://products.avnet.com/opasdata/d120001/medias/docus/120/Product_EBV-NPI-9956_otherdoc2_en.pdf

http://www.rfduino.com/product/rfduino-3-axis-lis3dh-accelerometer-demo/

http://binarycodec.blogspot.ch/2016/01/instalacao-via-shell-do-altera-quartus.html

http://www.digikey.com/en/product-highlight/a/altera/28nm-technology

http://kevinpelgrims.com/blog/files/images/2012/05/eclipse.png

https://en.wikipedia.org/wiki/Bus_Pirate

https://en.wikipedia.org/wiki/CERN

http://lhcb.web.cern.ch/lhcb/