

# Monitoring Vibrations with an FPGA

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UM CERN REU

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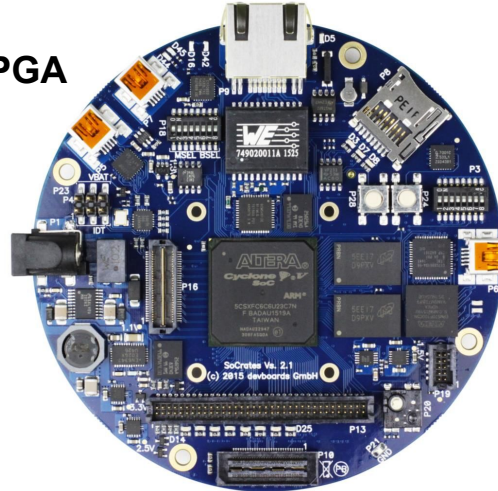
# LHCb

Event Filter Farm hard disks

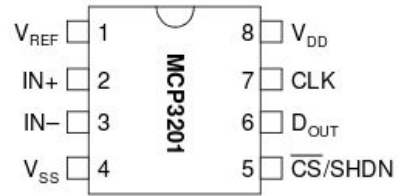
Develop a vibration monitoring system for the hard-disks using vibration sensors, ADCs and a SoC FPGA

# Components

FPGA

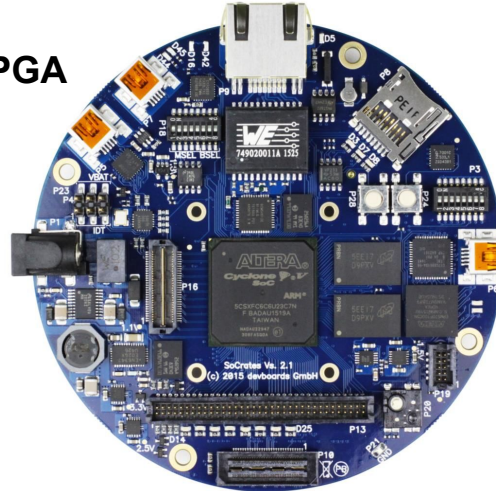


# Components

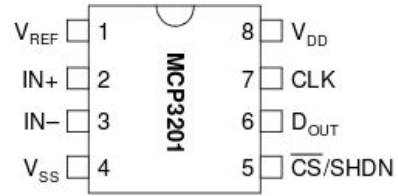


**ADC chip**

**FPGA**

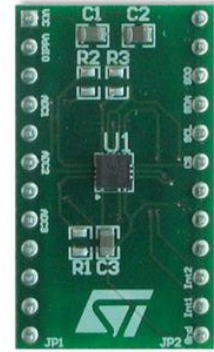
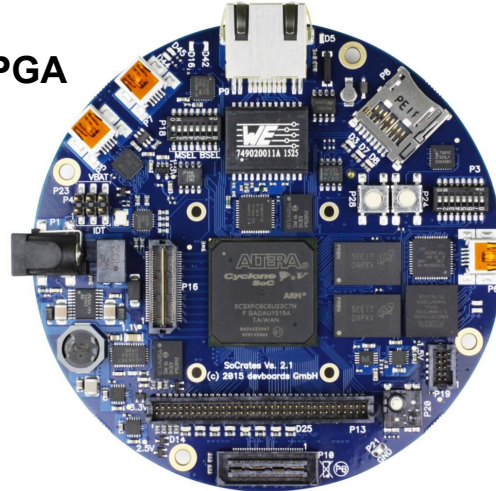


# Components



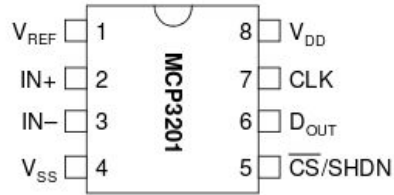
ADC chip

FPGA



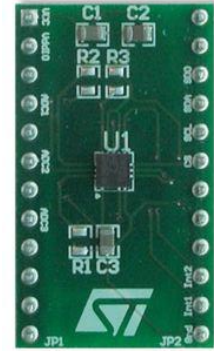
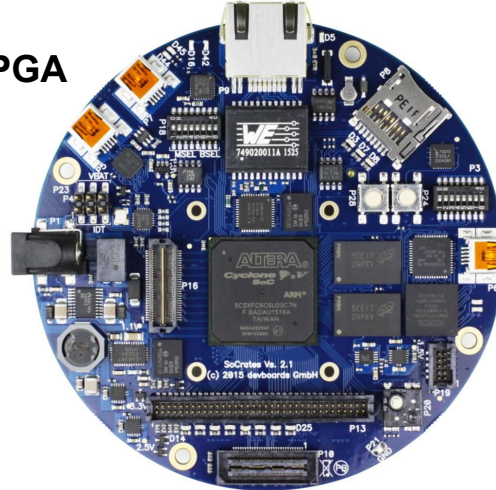
Accelerometer

# Components



ADC chip

FPGA



Accelerometer



Software

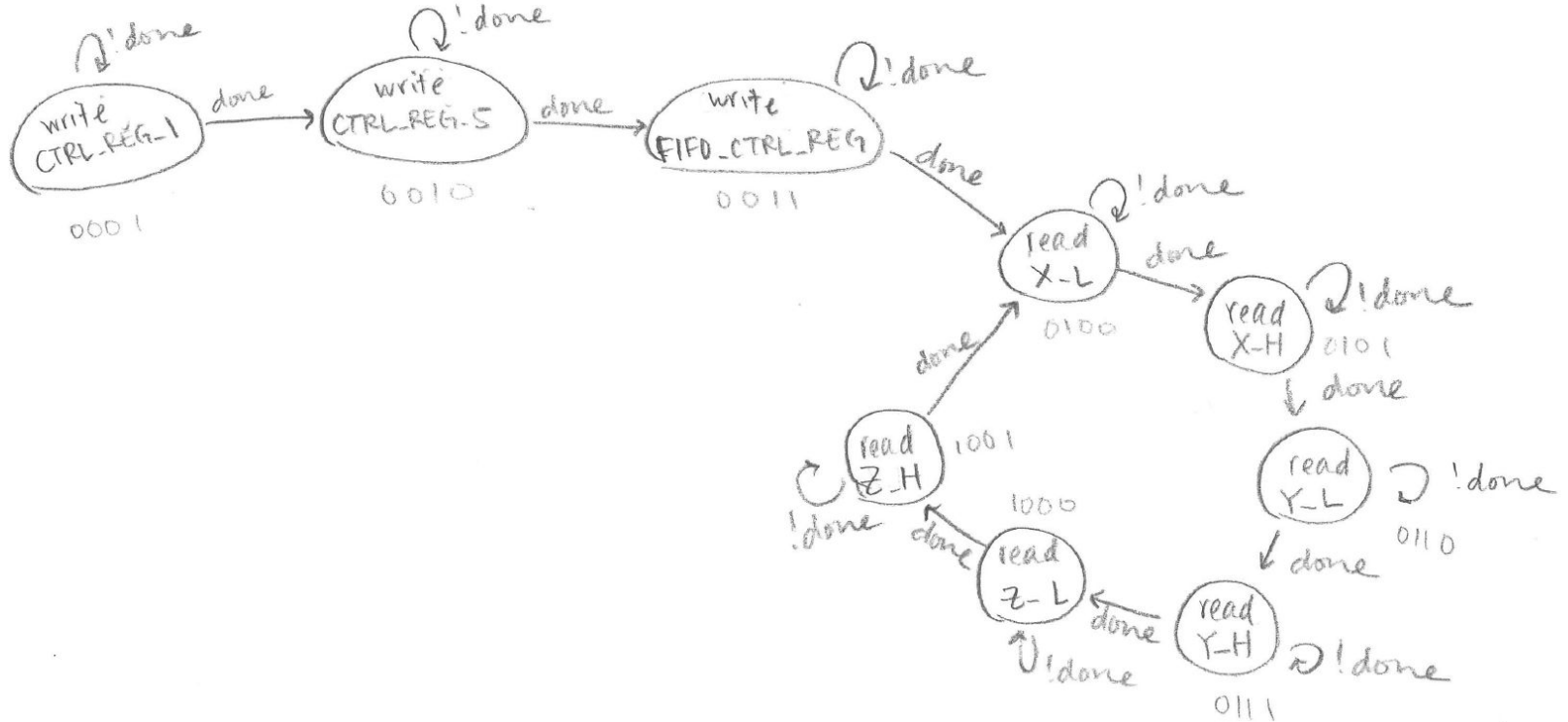


# Communication Protocols

- Designing protocols for a microcontroller to communicate with other integrated circuits
  - SPI - Serial Peripheral Interface
  - I<sup>2</sup>C - Inter-integrated Circuits Protocol
- Implemented primarily with finite state machines in Verilog

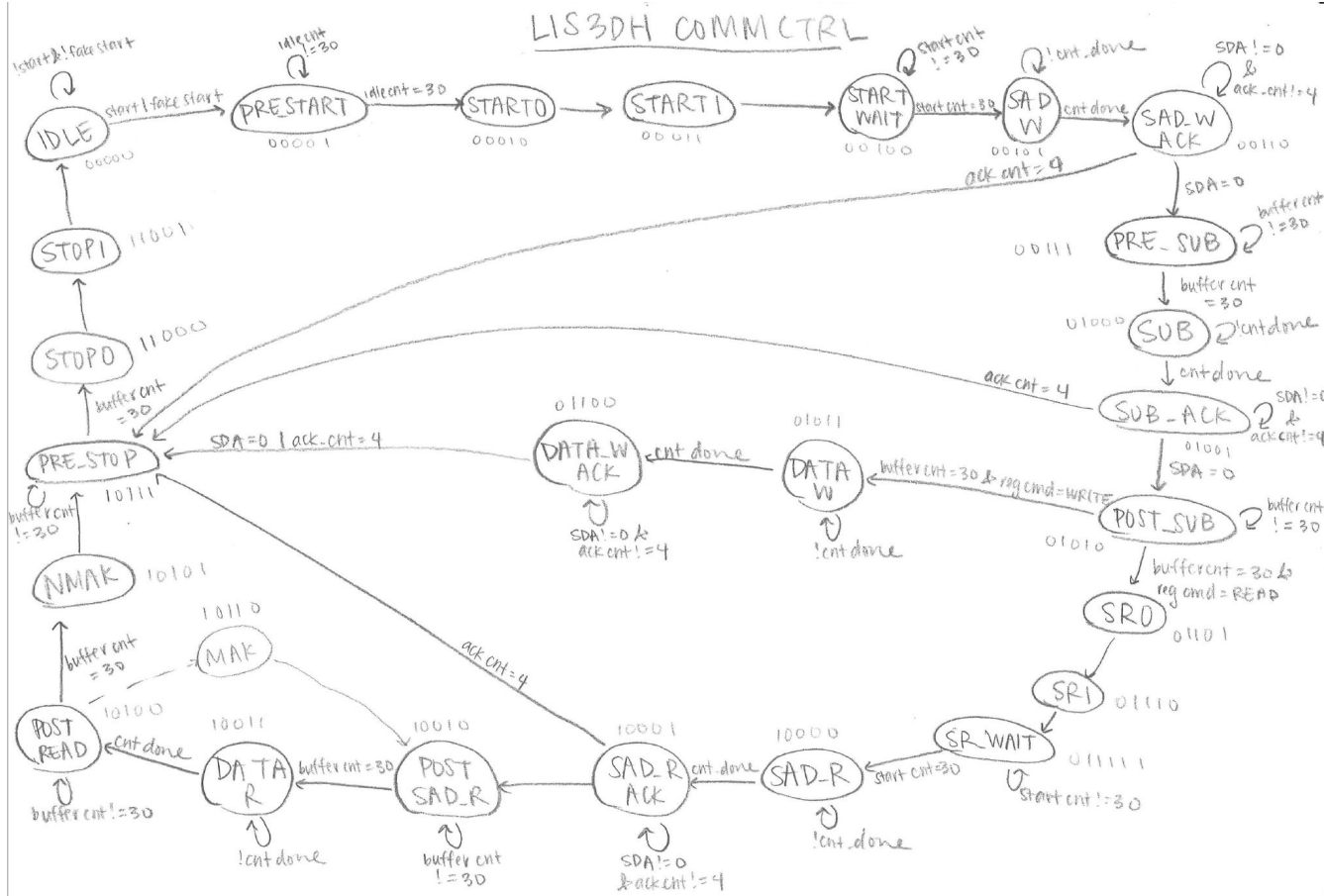
# I<sup>2</sup>C Finite State Machines - Top Level

LIS3DH I2C TOP





# I<sup>2</sup>C FSM - Bit Level Communications



# SignalTap Logic Analyzer

Debugging FPGA design is a different challenge because everything operates in real time and all signals are hardware.

The screenshot displays the SignalTap II Logic Analyzer software interface. The main window shows a digital signal trace with a time axis ranging from -2048 to 14336. The trace includes several signals: SCL, SDA, c\_state, instantiation sub\_state, instantiation byte rx[7..0], instantiation sr rx[7..0], b\_cnt1 sub instantiation shift, sub instantiation busy-reg0, instantiation dcnt[3..0], instantiation SDA\_en-reg0, sub instantiation fake\_start, y[15..0], instantiation reg\_cmd[1..0], instantiation buffer\_cnt[4..0], and instantiation data\_cnt[2..0]. The trace shows a sequence of digital signals, with a vertical dashed line indicating the trigger point. The data log at the bottom shows the trigger event and subsequent log messages.

Instance Manager: Ready to acquire

Instance: auto\_sigtap\_0 Not running 1619 cells 1507328 bits 0 blocks 184 blocks 0 blocks

JTAG Chain Configuration: JTAG ready

Hardware: SoCrates [2-1.7] Setup...

Device: @2: 5CSEBA6(.JES)/SCSEM. Scan Chain

SOF Manager: ...

log: Trig @ 2016/08/09 12:49:09 (0:0:0.0 elapsed)

click to insert time bar

Hierarchy Display:

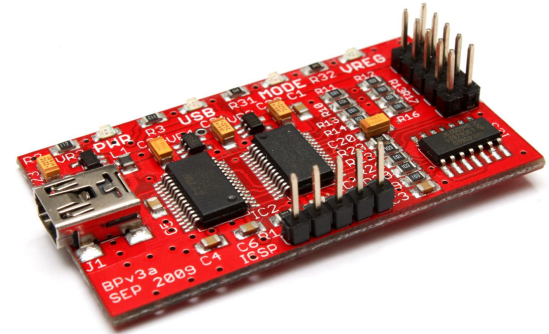
- LIS3DH\_I2C\_top
  - clk\_100k:clk\_100kHz\_i...
  - LIS3DH\_sub\_ctr1:sub\_i...

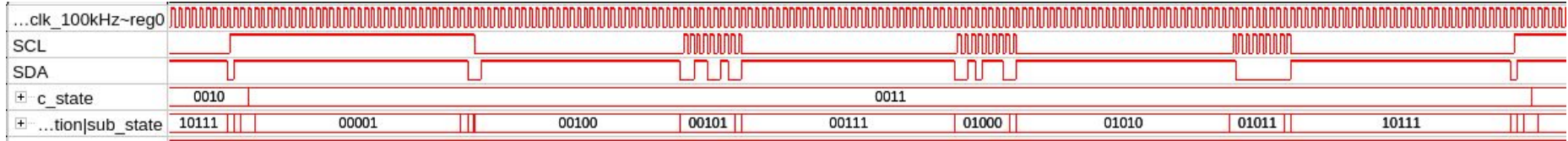
Data Log:

- auto\_sigtap\_0
  - signal\_set: 2016/07/26 15:05:06 #0
  - trigger: 2016/07/26 15:05:06 #1
    - log: Trig @ 2016/07/26 15:13:27 (0:0:0.0 elapsed) #1
    - log: Trig @ 2016/07/26 15:13:42 (0:0:0.0 elapsed)
    - log: Trig @ 2016/07/26 15:13:43 (0:0:0.0 elapsed)

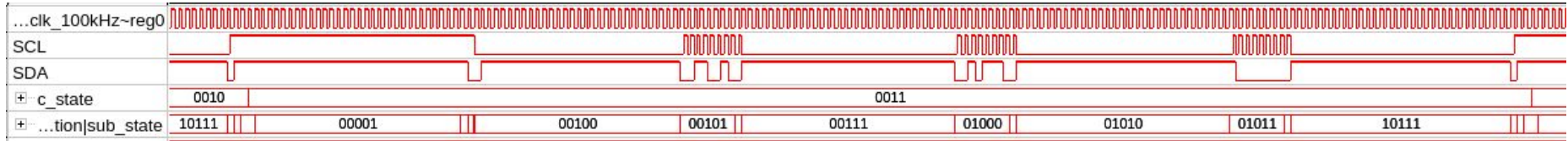
# Troubleshooting

- Testing and implementing in increments
- Bus Pirate - open source hacker multi-tool to confirm protocol
- Biggest errors:
  - Timing: transmit and receive bits one clock cycle after command
  - Longer hold times between issuing commands

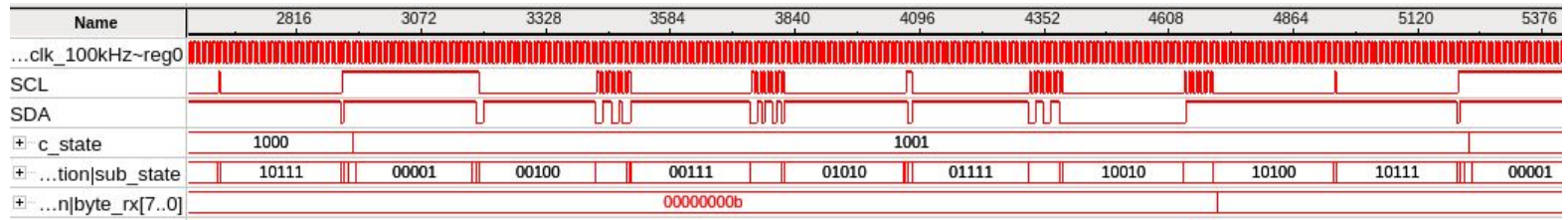




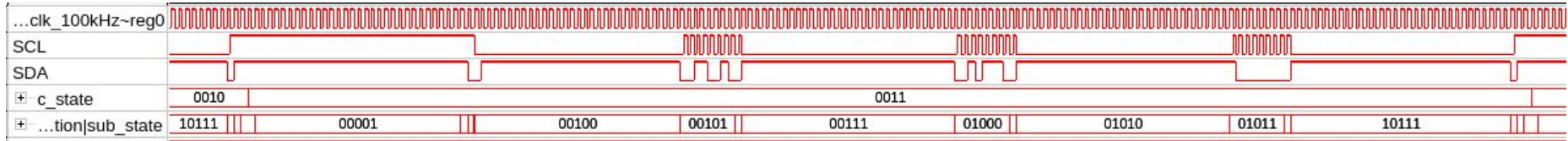
Configure FIFO\_CTRL\_REG (0010110b) to 10000000b



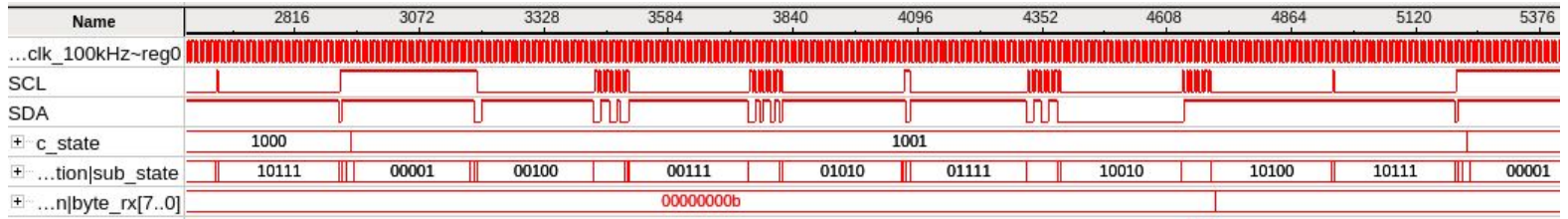
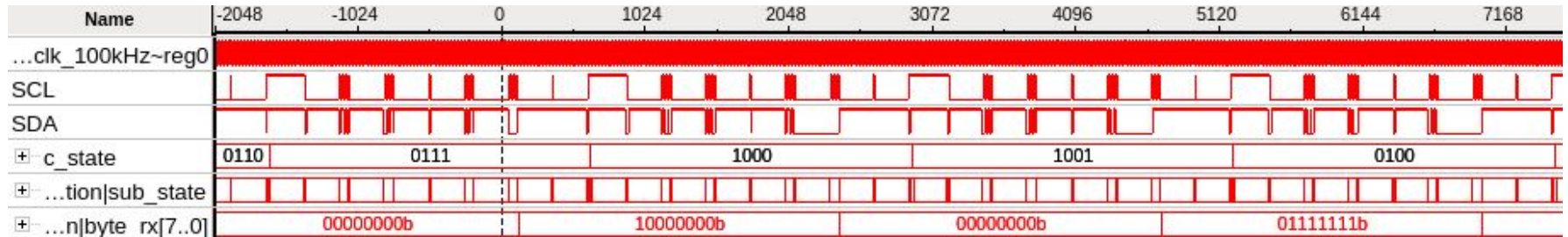
Configure FIFO\_CTRL\_REG (0010110b) to 10000000b



Reading output registers



Configure FIFO\_CTRL\_REG (0010110b) to 10000000b



Reading output registers

# Next Steps

- Apply Fourier transforms to data
- Separately analyze frequency, timing and amplitude of vibrations
- Install in the EFF and compare with data failing rate

# Thank You's

- Christian Faerber
- EP-LBC group & LHCb
- Steve Goldfarb & Jennifer Roloff
- Emanuel Gull, Junjie Zhu & Elise Bodei
- National Science Foundation & University of Michigan



Thank you for your time!

Questions?

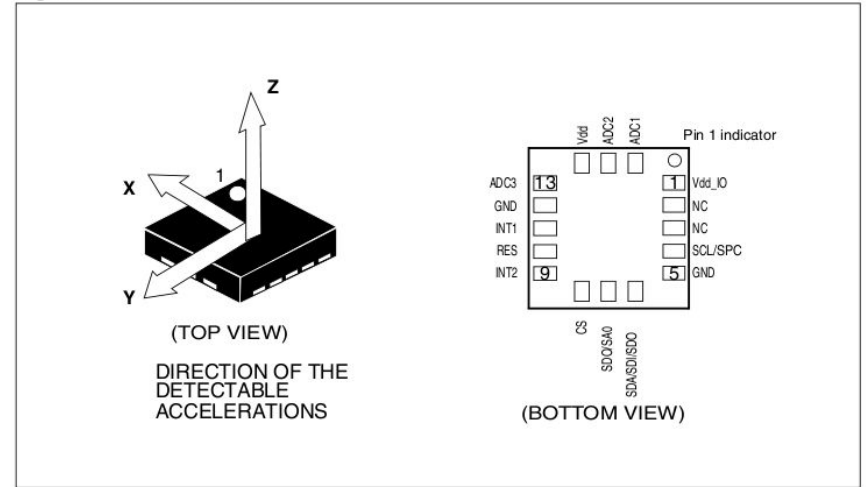
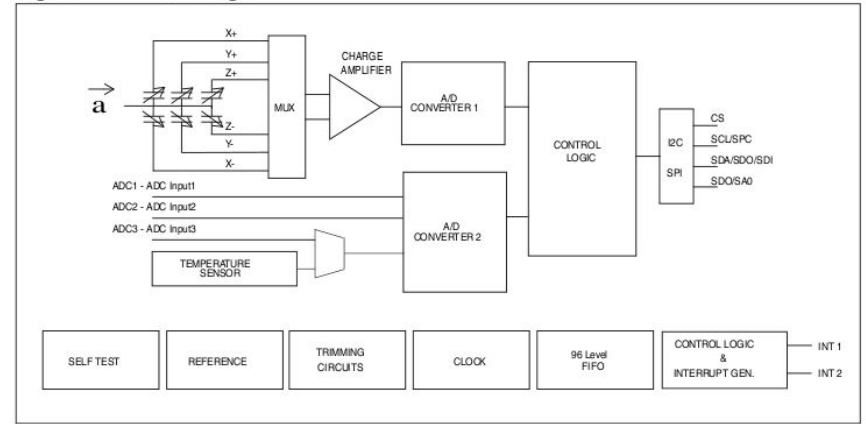
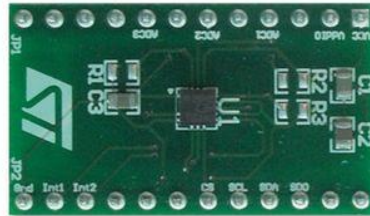


# Timing

- Operate on a 100kHz clock
- Response time of  $10\mu\text{s}$
- Start-up configuration time of 7.5ms
- Read each register every  $610\mu\text{s}$

# LIS3DH Accelerometer

- 3-axes linear accelerometer
- I<sup>2</sup>C & SPI digital output interface
- 96 level FIFO register with 16 bit data output



# Photo Citations

[https://products.avnet.com/opasdata/d120001/medias/docus/120/Product\\_EBV-NPI-9956\\_otherdoc2\\_en.pdf](https://products.avnet.com/opasdata/d120001/medias/docus/120/Product_EBV-NPI-9956_otherdoc2_en.pdf)

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